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A new balancing three level three dimensional space vector modulation strategy for three level neutral point clamped four leg inverter based shunt active power filter controlling by nonlinear back stepping controllers

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ABSTRACT

In this paper is proposed a new balancing three-level three dimensional space vector modulation (B3L-3DSVM) strategy which uses a redundant voltage vectors to realize precise control and high-performance for a three phase three-level four-leg neutral point clamped (NPC) inverter based Shunt Active Power Filter (SAPF) for eliminate the source currents harmonics, reduce the magnitude of neutral wire current (eliminate the zero-sequence current produced by single-phase nonlinear loads), and to compensate the reactive power in the three-phase four-wire electrical networks. This strategy is proposed in order to gate switching pulses generation, dc bus voltage capacitors balancing (conserve equal voltage of the two dc bus capacitors), and to switching frequency reduced and fixed of inverter switches in same times. A Nonlinear Back Stepping Controllers (NBSC) are used for regulated the dc bus voltage capacitors and the SAPF injected currents to robustness, stabilizing the system and to improve the response and to eliminate the overshoot and undershoot of traditional PI (Proportional-Integral). Conventional three-level three dimensional space vector modulation (C3L-3DSVM) and B3L-3DSVM are calculated and compared in terms of error between the two dc bus voltage capacitors, SAPF output voltages and THDv, THDi of source currents, magnitude of source neutral wire current, and the reactive power compensation under unbalanced single phase nonlinear loads. The success, robustness, and the effectiveness of the proposed control strategies are demonstrated through simulation using Sim Power Systems and S-Function of MATLAB/SIMULINK.

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1. Introduction

Recently, about the world the industrial and domestic equipment are progressively use the single and three phase unbalanced non-linear loads, such as rectifiers, power supplies and speed drivers, include nonlinear dynamics that entail the generation in four wire distribution networks the current harmonics, zero sequence current, and consumption of reactive power, these harmonics, zero sequence current, and reactive power causing harmful effects, such as the distortion of loads and waveform of line voltages, boosted ageing of loads and disturbing the other electronic equipments connected to the four wire distribution networks [1–4].

The modern filtering solutions to eliminate these harmonics and zero sequence current, and to improve the quality of electric power are, the four leg shunt active power filters (SAPFs), they can extensively studied and effectively solution for improve the mainly power factor by the elimination of harmonic currents and zero sequence current, and the compensation of reactive power into the point of common coupling (PCC) in three phase four wire electrical networks [3,5–7]. The most powerful converters used in four leg shunt active power filter have been the two-level four leg inverters. However, due to power handling capabilities of power semiconductors, these inverters configurations with a very high switching frequency of the switches incur additional losses in the switches and are limited for low and medium power applications.

To remedy these problems and to reach higher compensation levels, the researchers have been providing other configurations based on the series or parallel switches connection. These configurations are the parallel of multiple inverters in the case of

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parallel switches connection [8,9], and the multilevel inverter in the case of series switches connection [10]. The parallel of multiple inverters configurations offers an interesting alternative for reducing the switches constraints and the fractionation of the loads power [9]. The drawback of these configurations is the circulation currents between these paralleling inverters.

Various multilevel inverters configurations are proposed and used in the harmonics elimination and reactive power compensation, such as the multilevel Cascade H-bridge Inverter [11–14], Flying Capacitor Multilevel Inverter [15–17], and the multilevel neutral-point-clamped (NPC) Inverter [18–23]. The NPC inverters are the most widely used topology and successfully employed in medium and high power applications in the harmonics elimination and reactive power compensation for electrical networks [18]. The advantages of these inverters are; lower harmonics in the inverter output voltages, lower source current harmonics, lower switching losses, lower voltage stress of power semiconductors and circumvent the problems associated with two-level inverters based SAPF. The performances of four leg NPC inverters based SAPF depends on the strategies selected for better tracking quality and dynamic of reference harmonic currents generation, good robustness and stabilization of SAPF injected currents and dc bus voltages regulation, and the accuracy gate switching pulses generation. Several researchers described the effect of switching frequency and gate switching pulses on the performance of four leg NPC inverters. Benaissa et al. [24] have explicated the PWM based on Fuzzy logic controller to generate the gate switching pulses of the five level NPC four leg inverter used in SAPF for improved performance. Authors [25,26] have used the hysteresis controller for generate the gate switching pulses of three-level NPC inverter based SAPF. Switches inverter based SAPF suffers from variation switching frequency problem of hysteresis controller and it is also not fully effective in the application of SAPF due to the weak quality of SAPF output voltages and the unbalanced of dc bus voltage capacitors. Two modifications in the three-level NPC inverter based Distribution Static Compensator (DSTATCOM) are

suggested by Gawande et al. [21] to developed an news configurations of three-level NPC inverter based on hysteresis controller for circumvent the unbalance dc bus voltage capacitors problem, in these works not take into account the problem of variation switching frequency.

In the described works [27,28], Yaramasu et al., have also proposed a finite control-set model predictive control (FCS-MPC) strategy which uses a two-sample-ahead prediction horizon to achieve high performance operation for a four-leg NPC inverter. Some other works use a conventional three-level three dimensional space vector modulation strategy (C3L-3DSVM) for a four-leg NPC inverter [29–32], this strategy have been widely used in generation of gate switching pulses for three-level four leg NPC inverter based SAPF and DSTATCOM, as this strategy can fixed switching frequency, reduce commutation losses and harmonic contents of output voltage [14,15], and can obtain higher amplitude modulation indexes and high quality of output SAPF voltages waveforms. The drawback of these strategies is the unbalance of dc bus voltage capacitors for three-level four leg NPC inverters, this unbalanced is affected the loading of certain capacitor and unloading the other capacitor and causing harmful effects, such as the inverter output voltages distorted and from deteriorating any further in the level of inverter is increase, because of the proliferation midpoints between the capacitors. This unbalance of dc bus voltage capacitors problem is extensively studied by the researchers [33,34]. Zabalza et al. [33] have proposed a novel technique using triangular carrier pulse width modulation and [34] have described the level-shifted PWM and SVM to balance the neutral point voltage or the voltage of the two dc capacitors of a three-leg NPC inverter.

Several others researchers described the effects of reference currents generation theories on the performance of SAPFs [3,17]. For improvement the SAPF performances, in [35] have explicated the Synchronous Reference Frame theory (SRF) for reference currents generation based SAPF. Thirumoorthi et al. [36] have described the pq theory on the performance of SAPF to reduce
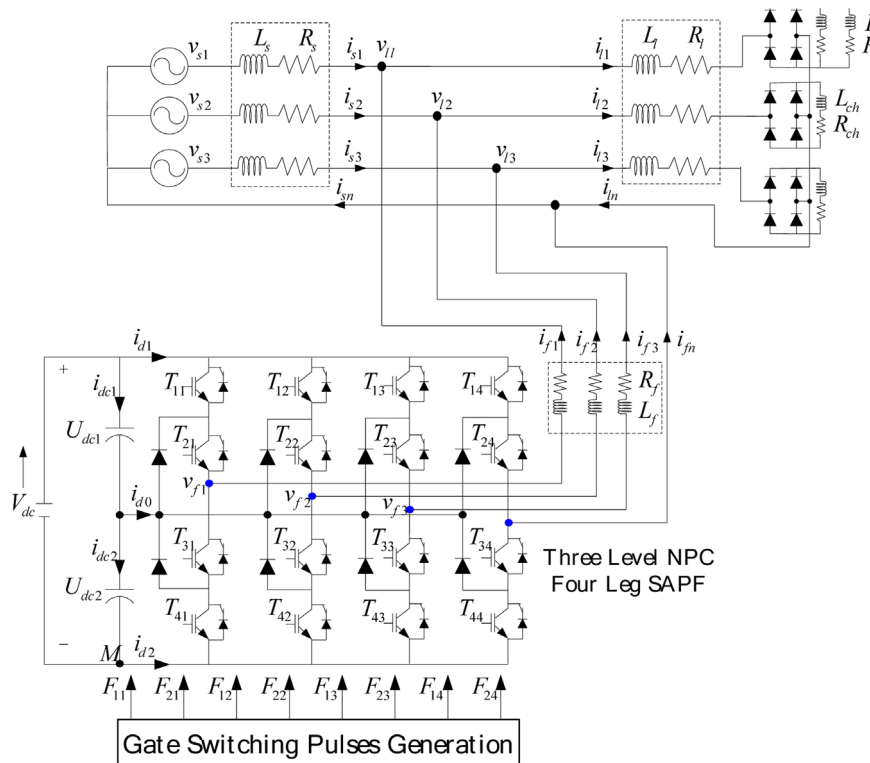

Fig. 1. Schematic block diagram of three phase three level NPC four leg shunt active power filter.

Table 1
Possible switching states of the three level NPC four-leg inverter and corresponding output voltages.
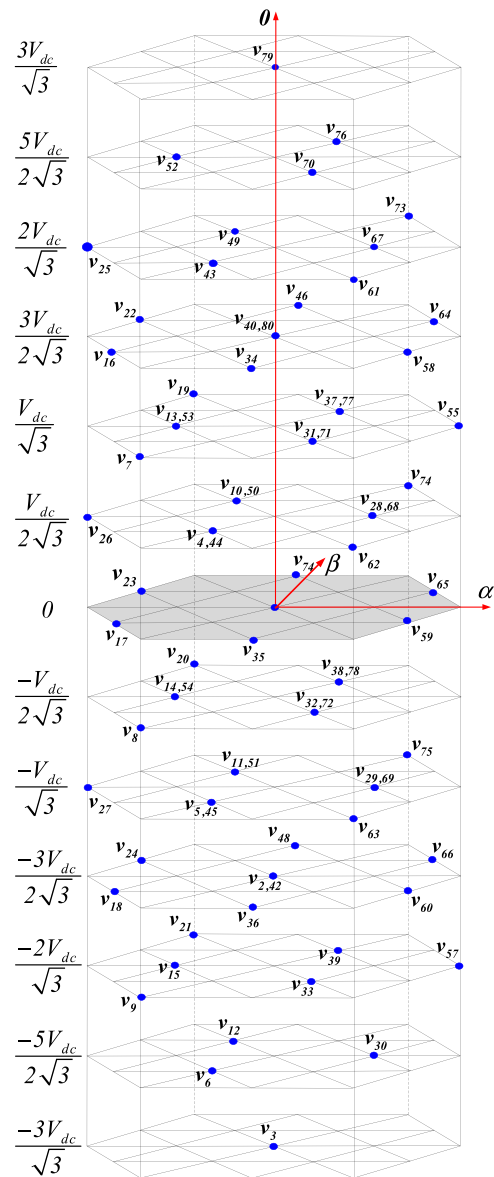
States F_j of the leg j	States of i switches of the j leg				Output voltages v_{jo}
	F_{1j}	F_{2j}	F_{3j}	F_{4j}	
P	1	1	0	0	$U_{dc1} + U_{dc2}$
O	0	1	1	0	U_{dc2}
N	0	0	1	1	0

Table 2
Voltage vectors of three level NPC four leg inverter and corresponding switching states.

voltage vectors	switching states	voltage vectors	switching states	voltage vectors	switching states
v_1	NNNN	v_{28}	ONNN	v_{55}	PNNN
v_2	NNNO	v_{29}	ONNO	v_{56}	PNNO
v_3	NNNP	v_{30}	ONNP	v_{57}	PNNP
v_4	NNON	v_{31}	ONON	v_{58}	PNON
v_5	NNOO	v_{32}	ONOO	v_{59}	PNOO
v_6	NNOP	v_{33}	ONOP	v_{60}	PNOP
v_7	NNPN	v_{34}	ONPN	v_{61}	PNPN
v_8	NNPO	v_{35}	ONPO	v_{62}	PNPO
v_9	NNPP	v_{36}	ONPP	v_{63}	PNPP
v_{10}	NONN	v_{37}	OONN	v_{64}	PONN
v_{11}	NONO	v_{38}	OONO	v_{65}	PONO
v_{12}	NONP	v_{39}	OONP	v_{66}	PONP
v_{13}	NOON	v_{40}	OOON	v_{67}	POON
v_{14}	NOOO	v_{41}	OOOO	v_{68}	POOO
v_{15}	NOOP	v_{42}	OOOP	v_{69}	POOP
v_{16}	NOPN	v_{43}	OOPN	v_{70}	POPN
v_{17}	NOPO	v_{44}	OOPO	v_{71}	POPO
v_{18}	NOPP	v_{45}	OOPP	v_{72}	POPP
v_{19}	NPNN	v_{46}	OPNN	v_{73}	PPNN
v_{20}	NPNO	v_{47}	OPNO	v_{74}	PPNO
v_{21}	NPNP	v_{48}	OPNP	v_{75}	PPNP
v_{22}	NPON	v_{49}	OPON	v_{76}	PPON
v_{23}	NPOO	v_{50}	OPOO	v_{77}	PPOO
v_{24}	NPOP	v_{51}	OPOP	v_{78}	PPOP
v_{25}	NPPN	v_{52}	OPPN	v_{79}	PPPN
v_{26}	NPPO	v_{53}	OPPO	v_{80}	PPPO
v_{27}	NPPP	v_{54}	OPPP	v_{81}	PPPP

**Fig. 2.** 3D space vector diagram ($\alpha\beta0$ frame) of three level NPC four leg inverter.

these problems. In all of them publications, have confirmed that the SAPF with SRF theory has simple structure, easy to realized and good harmonics extracting than others theories. The Synchronous Reference Frame theory is analyzed for three leg two level SAPF, Shunt Hybrid Active Power Filter (SHAPF) [35,37], and the DSTATCOM [38,39], and in four leg two level SAPF and DSTATCOM [3,14]. This concept has been extended by simulation studies to three-level NPC three and four leg SAPFs [30,40] using the same loads model presented in [3]. The Synchronous Reference Frame theory is extracted the reference harmonic currents directly after Park Transformation of distorted loads currents using low pass filter (LPF).

Also others researchers have demonstrated the effects of dc bus voltages and SAPF injected currents regulation on the performance of SAPF. Yi et al. [12] demonstrated the good performances gives in the application of linear PI regulators. Nevertheless, during the loads unbalanced and parameter variations, the linear PI regulators caused in the dc bus voltage capacitors the overshoot and undershoot which affects the SAPF performances and caused the breakdown of capacitors dielectric [36]. Therefore, the dynamic performance of linear PI regulators uses in dc bus voltage capacitors and reference currents regulation are not robustness and not stabilization due to loads unbalanced and parameter variations. The Nonlinear Back Stepping Controller (NBSC) (BSRs) possibly will be used for improving the dynamics of linear PI regulators to

have increase the robustness, the stabilization, gives good regulation on the dc bus voltage and the SAPF injected currents by the elimination of overshoot and undershoot in the dc bus voltage capacitors and the elimination of the error between the SAPF injected currents and there references [3]. The Nonlinear Back Stepping Controller (NBSC) is a systematic and flexible technique, newly developed and can be effectively used to linearize a nonlinear system in the presence of uncertainties. The Nonlinear Back Stepping Controller (NBSC) is used for controlled the three leg two level SAPF [41-43] and has been extended to four leg two level SAPF [3]. The Nonlinear Back Stepping Controller (NBSC) laws are based in the derived easy step by step across an appropriate Lyapunov. In this paper, Nonlinear Back Stepping Controllers are used for controlling the three level NPC four-leg SAPF and compared with linear PI regulators in terms of robustness, references tracking for the total dc bus voltage and SAPF injected currents under unbalanced loads, harmonics and switching ripple in source currents, reactive power compensation, overshoot and undershoot in the dc bus voltage capacitors, and the error between the SAPF injected currents and there references under unbalanced loads.
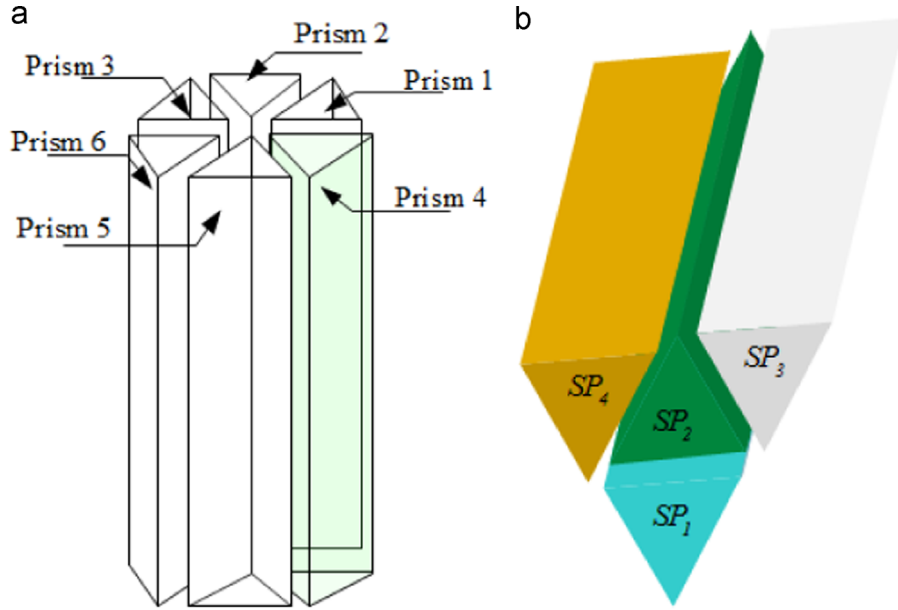
Fig. 3. Representation of prisms in the vector diagram of the three level NPC four legs inverter, and the sub-prisms in the first prism. (a) The prisms, (b) the four sub-prisms in first prism.

In this paper, a new balancing three level three dimensional space vector modulation (B3L-3DSVM) is proposed which based on the incessant measurement of output current and difference between dc bus voltages for selected the voltage vector for both redundant voltage vectors in three level NPC four-leg inverter based SAPF under unbalanced loads with an Nonlinear Back Stepping Controllers for controlling the dc bus voltage capacitors and SAPF injected currents, and the Synchronous Reference Frame theory for reference currents generation. The proposed new B3L-3DSVM strategy used for gate switching pulses generation and dc bus voltage capacitors balancing of three level NPC four-leg SAPF, it has dc bus voltage capacitors balancing, fixed switching frequency and lower power losses of the inverter switches, high quality of output SAPF voltages waveforms and lower THDv, lower THDi of source currents, lower ripple in neutral wire current and reactive power source. It also improves the operations of three level NPC four-leg SAPF due to conventional three level 3D SVM. This paper is organized as follows: Section II gives the controller configuration and mathematical model of the three level NPC four-leg SAPF. In Section III, the conventional three level 3D SVM is introduced, with their detail calculations. The new balancing three level 3D SVM with its basic calculations in detail is proposed in Section IV. Section V gives feature comparisons between the proposed balancing three level 3D SVM and the conventional three level 3D SVM. Finally, in Section VI, related the conclusions obtained in this paper.

2. Three level NPC four-leg sapf system configuration

Fig. 1 shows a schematic diagram of a three phase three level neutral point clamped (NPC) four leg inverter based SAPF, this is connected in a Point of Common Coupling (PCC) to a three phase four-wire electrical network with a source inductors and resistors (L_s and R_s) feeding three single-phase nonlinear loads. Three level NPC four leg SAPF is connected in the PCC of electrical network by an L-R_f coupling filter for reducing the ripple in SAPF injected currents (i_{f123n}). The three level NPC four leg SAPF currents are injected in the electrical network at the PCC to compensating the harmonics of the loads currents and cancel the reactive power components in the network.

The variables for three level NPC four leg SAPF control are PCC voltages (v_{l123}), source currents (i_{s123n}), loads currents (i_{l123n}) and dc bus voltage capacitors (U_{dc1} and U_{dc2}) of three level NPC four leg inverter used in SAPF.

$i_{c1,2}$: the currents of the capacitors,
$i_{d1,2}$: inverter inputs currents,
i_{d0}: output current from the neutral point voltage between the two capacitors,

The three level NPC four leg inverter detail concepts are extended in [18,30], this three level NPC four leg inverter topology is generate at the outputs three voltage levels according to the switching states of each leg F_{ij}. These three voltage levels and corresponding switching states are summarized in Table 1 [11,12]:

v_{jN} are the output voltages of each phase to the negative point of the dc bus capacitors (M). These voltages are expressed in terms of the dc bus voltage capacitors (U_{dc1} and U_{dc2}) and the switching states of each leg as follows [11,12]:

$$v_{jM} = U_{dc1}F_{1j} + U_{dc2}F_{2j}, \quad j = 1, 2, 3, n \tag{1}$$

The phases to neutral output voltages are defined as:

$$v_{jn} = v_{jM} - v_{nM} \tag{2}$$

According to the possible switching states combinations of each leg, in the three level NPC four leg inverter topology there are $3^4 = 81$ voltage vectors combinations; 79 active voltage vectors and 3 null. These 81 voltage vectors of three level NPC four leg inverter and corresponding switching states are summarized in Table 2 [11,12]:

The mathematical model of the three level NPC four leg SAPF is defined in dq0-axes as follows:

$$\begin{cases} \frac{di_{fd}}{dt} = -\frac{R_f}{L_f}i_{fd} + \omega i_{fq} + \frac{1}{L_f}v_{fd} - \frac{1}{L_f}v_{ld} \\ \frac{di_{fq}}{dt} = -\frac{R_f}{L_f}i_{fq} - \omega i_{fd} + \frac{1}{L_f}v_{fq} - \frac{1}{L_f}v_{lq} \\ \frac{di_{fo}}{dt} = -\frac{R_f}{L_f}i_{fo} + \frac{1}{L_f}v_{fo} - \frac{1}{L_f}v_{lo} \\ \frac{dV_{dc}}{dt} = -\frac{1}{C}i_{dc}^* \end{cases} \tag{3}$$

Fig. 2 shows the distribution of the three level NPC four leg inverter voltage vectors in the 3D space vector diagram (αβ0

frame) [18] corresponding the inverter output voltages in the αβ0 frame.

3. Balancing three-level three dimensional space vector modulation (B3L-3DSVM)

The B3L-3DSVM in the αβ0 frame has been developed and employed for the gate switching pulses generation of three level NPC four-leg inverter based SAPF. As in the 2L-3DSVM for 2-level four leg inverter control [3], in order to realizing the B3L-3DSVM for three level NPC four-leg inverter control, it is necessary to proceed by the following four steps:

- Identification of prisms and sub-prisms,
- Identification of tetrahedrons,
- Calculation the times duration of selected voltage vectors,
- Generation of gate switching pulses for three level NPC four-leg inverter.

3.1. Identification of prisms and sub-prisms

The detail concepts of C3L-3DSVM strategy and all steps are presented and described in [29,30]. The vector diagram of three level NPC four leg inverter shown in Fig. 2 is composed of six prisms Fig. 3-a are so-called Prisms 1 through 6, each prism is decomposed into four sub-prism Fig. 3b are so-called SP$_1$ to SP$_4$.

The four sub-prism of each prism are detected by using the equations of the eight straights (d$_1$, d$_2$,…, d$_8$) delimitation of each sub-prism as shown in Fig. 4, these eight straights are gives as follows.

$$
\begin{cases}
d_1 : v_{f\beta}^* = -\sqrt{3}v_{f\alpha}^* + \sqrt{\tfrac{1}{2}}V_{dc} \\
d_2 : v_{f\beta}^* = \sqrt{\tfrac{1}{8}}V_{dc} \\
d_3 : v_{f\beta}^* = \sqrt{3}v_{f\alpha}^* - \sqrt{\tfrac{1}{2}}V_{dc} \\
d_4 : v_{f\beta}^* = \sqrt{3}v_{f\alpha}^* \\
d_5 : v_{f\beta}^* = \sqrt{3}v_{f\alpha}^* + \sqrt{\tfrac{1}{2}}V_{dc} \\
d_6 : v_{f\beta}^* = -\sqrt{3}v_{f\alpha}^* \\
d_7 : v_{f\beta}^* = -\sqrt{3}v_{f\alpha}^* - \sqrt{\tfrac{1}{2}}V_{dc} \\
d_8 : v_{f\beta}^* = -\sqrt{\tfrac{1}{8}}V_{dc}
\end{cases}
\tag{4}
$$

3.2. Identification of tetrahedrons

As in two level four leg inverter case [3], each sub-prism is decomposed into m tetrahedrons, the tetrahedrons can be constructed by the combination of three voltage vectors non-null and two null. Fig. 4 shows the separated images in 3 dimensions from the tetrahedrons for each sub-prism. In each sub-prism, the tetrahedrons are distributed as follows:

- in the first Sub-prism SP1, we discovers 10 tetrahedrons ($m=10$)
- in the second Sub-prism SP2, we discovers 8 tetrahedrons ($m=8$)
- in the third and fourth Sub-prism SP3 and SP4, we discovers 7 tetrahedrons ($m=7$)

Fig. 5. Representation of the tetrahedrons in each sub-prism in the first prism.

Fig. 6. Representation of first tetrahedron in first sub-prism in the first prism and there extremity façades.

Table 3
Three active voltage vectors and the corresponding inverter output voltages.

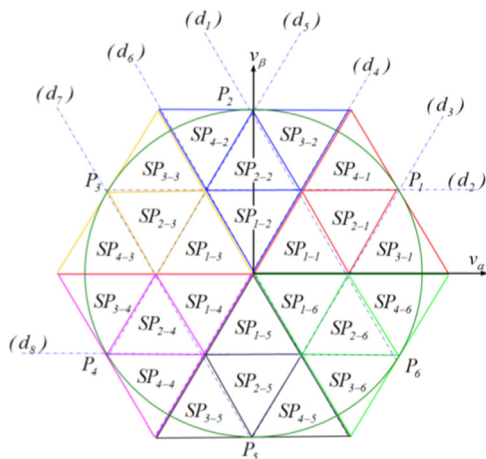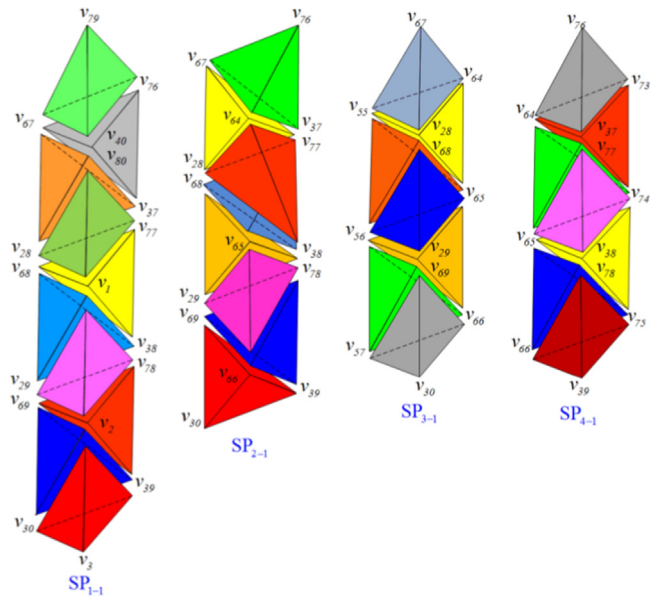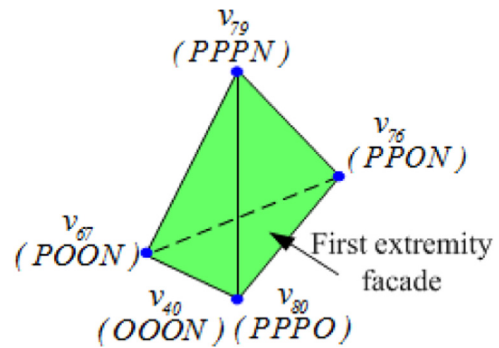| Voltage vectors	$\frac{v}{f\alpha}$	$\frac{v}{f\beta}$	$\frac{v}{f0}$
v_{40}	0	0	$3V_{dc}/2\sqrt{3}$
v_{67}	$V_{dc}/\sqrt{6}$	0	$2V_{dc}/\sqrt{3}$
v_{76}	$V_{dc}/\sqrt{24}$	$\sqrt{2}V_{dc}/4$	$5V_{dc}/2\sqrt{3}$

Fig. 4. Representation of prisms in the vector diagram of the three level NPC four leg inverter, and the sub-prisms in the prism 1. (a) The prisms. (b) The four sub-prisms in prism 1.

Table 4
Relation between the currents of the capacitors and SAPF injected currents for all voltage vectors redundant.

Redundant vectors	the redundant (red)		Stat vector	i_{f1}	i_{f2}	i_{f3}	i_{fn}	i_{dc1}	i_{dc2}	
Redon1	A	v_2	NNNO	0	0	0	1	$-I$	I	$I=i_{fn}$
	B	v_{42}	OOOP	1	1	1	0	I	$-I$	
Redon2	A	v_4	NNON	0	0	1	0	I	$-I$	$I=i_{f3}$
	B	v_{44}	OOPO	1	1	0	1	$-I$	I	
Redon3	A	v_5	NNOO	0	0	1	1	$-I$	I	$I=i_{fn}-i_{f3}$
	B	v_{45}	OOPP	1	1	0	0	I	$-I$	
Redon4	A	v_{10}	NONN	0	1	0	0	I	$-I$	$I=i_{f2}$
	B	v_{50}	OPOO	1	0	1	1	$-I$	I	
Redon5	A	v_{11}	NONO	0	1	0	1	I	$-I$	$I=i_{f2}-i_{fn}$
	B	v_{51}	OPOP	1	0	1	1	$-I$	I	
Redon6	A	v_{13}	NOON	0	1	1	0	$-I$	I	$I=i_{f1}-i_{fn}$
	B	v_{53}	OPPO	1	0	0	1	I	$-I$	
Redon7	A	v_{14}	NOOO	0	1	1	1	$-I$	I	$I=i_{f1}$
	B	v_{54}	OPPP	1	0	0	0	I	$-I$	
Redon8	A	v_{28}	ONNN	1	0	0	0	I	$-I$	$I=i_{f1}$
	B	v_{68}	POOO	0	1	1	1	$-I$	I	
Redon9	A	v_{29}	ONNO	1	0	0	1	I	$-I$	$I=i_{f1}-i_{fn}$
	B	v_{69}	POOP	0	1	1	0	$-I$	I	
Redon10	A	v_{31}	ONON	1	0	1	0	$-I$	I	$I=i_{f2}-i_{fn}$
	B	v_{71}	POPO	0	1	0	1	I	$-I$	
Redon11	A	v_{32}	ONOO	1	0	1	1	$-I$	I	$I=i_{f2}$
	B	v_{72}	POPN	0	1	0	0	I	$-I$	
Redon12	A	v_{37}	OONN	1	1	0	0	$-I$	I	$I=i_{f3}-i_{fn}$
	B	v_{77}	PPOO	0	0	1	1	I	$-I$	
Redon13	A	v_{38}	OONO	1	1	0	1	$-I$	I	$I=i_{f3}$
	B	v_{78}	PPOP	0	0	1	0	I	$-I$	
Redon14	A	v_{40}	OOON	1	1	1	0	I	$-I$	$I=i_{fn}$
	B	v_{80}	PPPO	0	0	0	1	$-I$	I	

Table 5
Effect of each voltage vector redundancy on the two voltage capacitors.

G	Redon-i A		Redon-i B	
	U_{dc1}	U_{dc2}	U_{dc1}	U_{dc2}
1	+	−	−	+
0	−	+	+	−

Table 6
The stats of the error between the two voltage capacitors.

M	$U_{dc1}-U_{dc2} > 0$	$U_{dc1}-U_{dc2} < 0$
1	x	
0		x

Table 7
The voltage vector redundancy to be applied for each redundant vectors.

G	M	
	1	0
1	Red A	Red B
0	Red B	Red A

What discovered 32 tetrahedrons in each prism and a total of 192 tetrahedrons in the vector diagram of three level NPC four leg inverter in three dimensions space (αβ0 plan) (Fig. 5).

To detect which tetrahedron is the reference voltage vector, it is necessary to detect the location of each tetrahedron by the calculation of the equations defined the three extremity facades of each tetrahedron using the $(v^*_{f\alpha}, v^*_{f\beta}, v^*_{f0})$ coordinates. For example, the first tetrahedron of the first sub-prism of first prism is constructed by the combination of five voltage vectors ($v_{40}, v_{67}, v_{76}, v_{79}, v_{80}$) as shown in Fig. 6, the first extremity façade of this tetrahedron is constructed by the three voltage vectors (v_{40}, v_{67}, v_{76}), these voltage vectors and the corresponding inverter output voltages in the αβ0 frame are summarized in Table 3.

Referring to Table 3, we are calculating the equation defined the first extremity façade of this tetrahedron as follow.

$$\begin{cases} a.0+b.0+c=\frac{3}{2\sqrt{3}}V_{dc} \rightarrow v_{40} \\ a.\frac{V_{dc}}{\sqrt{6}}+b.0+c=\frac{2}{\sqrt{3}}V_{dc} \rightarrow v_{67} \\ a\frac{V_{dc}}{\sqrt{24}}+b\frac{\sqrt{2}}{4}V_{dc}+c=\frac{5}{2\sqrt{3}}V_{dc} \rightarrow v_{76} \end{cases} \tag{5}$$

Which give:

$$a=\frac{\sqrt{2}}{2}, \quad b=\sqrt{\frac{3}{2}} \quad and \quad c=\frac{3}{2\sqrt{3}}V_{dc}$$

The equation defined the location of the first tetrahedron for the first sub-prism of first prism is:

$$v^*_{f0} > \frac{\sqrt{2}}{2}v^*_{f\alpha}+\sqrt{\frac{3}{2}}v^*_{f\beta}+\frac{3}{2\sqrt{3}}V_{dc} \tag{6}$$

In like manner, we determine the equations defined the locations of other tetrahedrons to the different sub-prisms of different prisms.

3.3. Calculation the times duration of selected voltage vectors

We recall that the calculation of times duration in 3L-3DSVM are a great similar for the 2L-3DSVM. Therefore, the determination of the times duration of the projection of each voltage vectors applications in each tetrahedron will be done in a manner similar to that described in [3], these times duration of the projection of
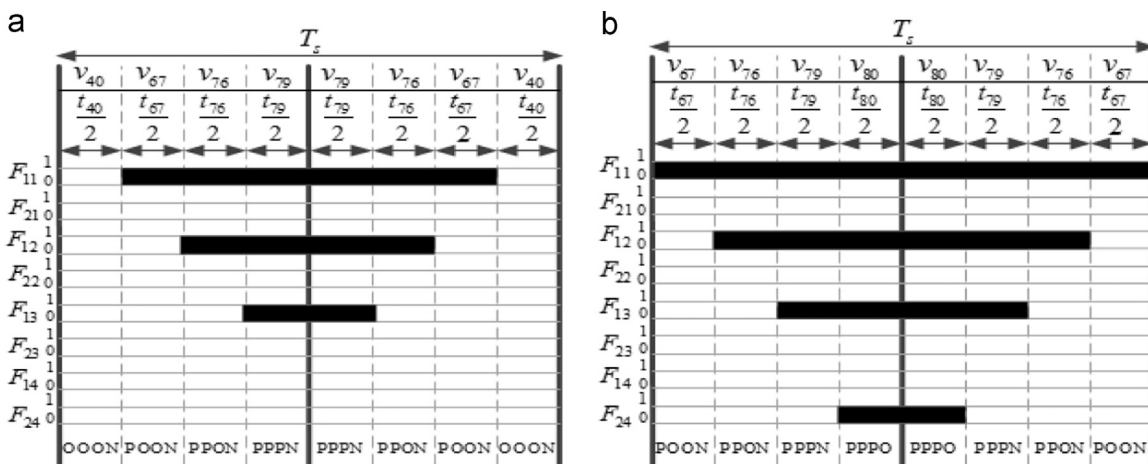
a

b

Fig. 7. The gate switching pulses in the first tetrahedron of the first sub-prism of first prism; (a) case of voltage vector v_{40} is selected; (b) case of voltage vector v_{80} is selected.
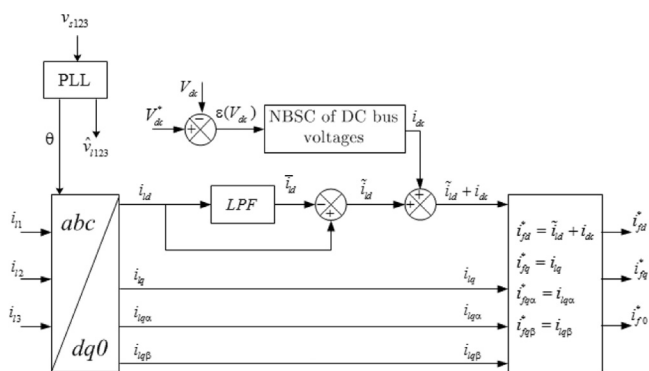

Fig. 8. Blok diagram of the SRF theory using PLL based three-level NPC four leg SAPF.

each voltage vectors are gives as:

$$
\begin{bmatrix} t_{v1} \\ t_{v2} \\ t_{v3} \\ t_{v4} \end{bmatrix} = \frac{T_s}{V_{dc}}[A]^{-1} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \\ v_0^* \\ 1 \end{bmatrix}
\tag{7}
$$

We denote by t_{v1}, t_{v2}, t_{v3} and t_{v4} the times application of voltage vectors that belong to each tetrahedron during the half of switching period (T_s), and $[A]^{-1}$ is the projection matric of the voltage vectors. For example, the voltage vectors ($v_{40}, v_{67}, v_{76}, v_{79}$) in the first tetrahedron of the first sub-prism of first prism, the projection matrix $[A]$ is given as follow.

$$
[A]^{-1} = \begin{bmatrix} 0 & 1/\sqrt{6} & 1/\sqrt{24} & 0 \\ 0 & 0 & \sqrt{2}/4 & 0 \\ 3/2\sqrt{3} & 2/\sqrt{3} & 5/2\sqrt{3} & 3/\sqrt{3} \\ 1 & 1 & 1 & 1 \end{bmatrix}
\tag{8}
$$

3.4. Generation of gate switching pulses for three level NPC four-leg inverter

The basic idea for control the neutral point voltage of three level NPC four leg inverter is based significant on the incessant measurement of output current (i_{d0}) from the neutral point of this inverter and the error between the two dc bus voltage capacitors to select the voltage vector in both redundant voltage vectors in each tetrahedron, to inject in the neutral point a positive or negative current. These two dc bus voltages and the inverter

inputs currents (i_{dc1} and i_{dc2}) are given by the following equations.

$$
\begin{cases} V_{dc} = U_{dc1} + U_{dc2} \\ i_{d0} = i_{dc1} - i_{dc2} \\ C\frac{dV_{dc}}{dt} = C_1\frac{dU_{dc1}}{dt} + C_2\frac{dU_{dc2}}{dt} \\ \qquad = (i_{dc1} - i_{d1}) + (i_{dc2} + i_{d2}) \end{cases}
\tag{9}
$$

$$
\begin{cases} i_{d0} = -(i_{d1} + i_{d2}) \\ i_{d1} = F_{11}.F_{12}.i_{f1} + F_{21}.F_{22}.i_{f2} + F_{31}.F_{32}.i_{f3} - F_{41}.F_{42}.i_{fn} \\ i_{d2} = F_{13}.F_{14}.i_{f1} + F_{23}.F_{24}.i_{f2} + F_{33}.F_{34}.i_{f3} - F_{43}.F_{44}.i_{fn} \end{cases}
\tag{10}
$$

In order to eliminate the error between the two dc bus voltage capacitors, we supposing the total dc bus voltage V_{dc} is constant, it follows that:

$$
i_{dc1} + i_{dc2} = 0
\tag{11}
$$

From the Eqs. (9)–(11) we deduce the following expression:

$$
\begin{aligned} i_{d0} = &-((F_{11}.F_{12} + F_{13}.F_{14}).i_{f1} + (F_{21}.F_{22} + F_{23}.F_{24}).i_{f2} \\ &+ (F_{31}.F_{32} + F_{33}.F_{34}).i_{f3} - (F_{41}.F_{42} + F_{43}.F_{44}).i_{fn}) \end{aligned}
\tag{12}
$$

Eq. (6) shows that relationship among the output current (i_{d0}) from the neutral point voltage and SAPF injected currents depend on the function of switching vector states (F_{ji}).

The sign of three level NPC four leg inverter inputs currents depends on two factors: voltage vectors in each tetrahedron and inverter injected currents. The three level NPC four leg inverter has 14 redundant voltage vectors shown on the vector diagram of Fig. 2, which produce the same inverter output voltages, which is the same currents injected by three level NPC four leg inverter, but have opposite effects on the two capacitors. Table 4 gives, for both voltage vectors redundant in each tetrahedron the explicit association among the currents of the capacitors and SAPF injected currents.

3.4.1. Elaboration of the balancing capacitors voltages table

To illustrate the synthesis of truth table necessary for balancing the dc bus capacitor voltages of three level NPC four leg inverter it is interesting for the choice of voltage vector redundant for each tetrahedron applying to increase or decrease both the voltage of each capacitor.

3.4.1.1. Truth table of capacitors currents. In each voltage vector application for both redundant vectors in each tetrahedron, the state of capacitor voltages (increase or decrease) depends on the value of two currents i_{c1} and i_{c2}, i.e. value of i_{d0}. We define a

function G dependent on polarity of i_{d0}:

$$G = \begin{cases} 1 & si \quad i_{d0} \geq 0 \\ 0 & si \quad i_{d0} \leq 0 \end{cases} \qquad (13)$$

Table 5 summarizes the effect of each voltage vector redundancy on the two voltage capacitors U_{dc1} and U_{dc2}. The sign ($+$) indicates the increase in voltage, and the sign (-) indicates a decrease.

Table 5 shows that:

In case $G=1$: the redundancy A of each redundant voltage vectors causes an increase of voltage U_{dc1} and decrease of voltage U_{dc2}, while the redundancy B causes an decrease of U_{dc1} and increase U_{dc2}.

In case $G=0$: the redundancy A of each redundant voltage vectors causes decrease of voltage U_{dc1} and increase of voltage U_{dc2}, while the redundancy B causes the increase of U_{dc1} and decrease of U_{dc2}.
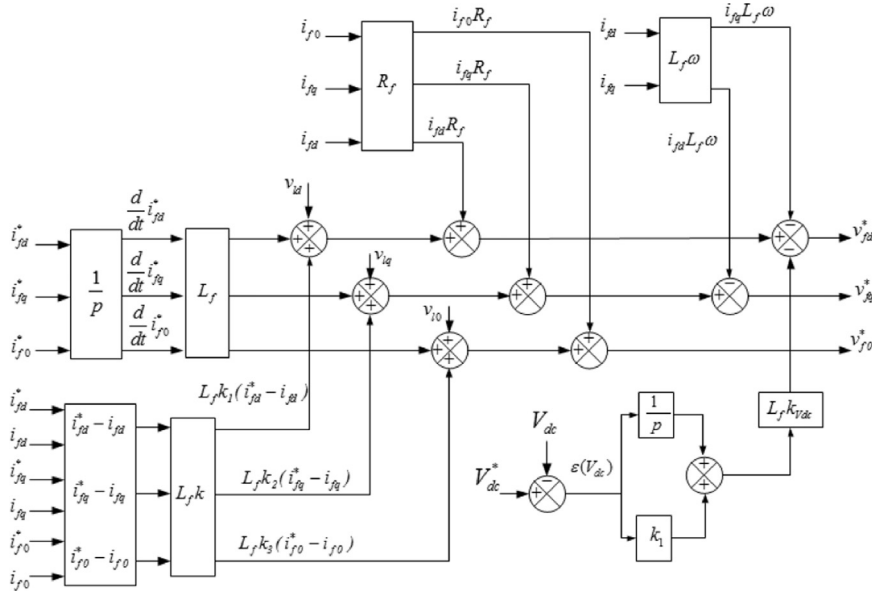

Fig. 9. block diagram of Nonlinear Back Stepping Controllers (NBSC) based three-level NPC four leg SAPF.
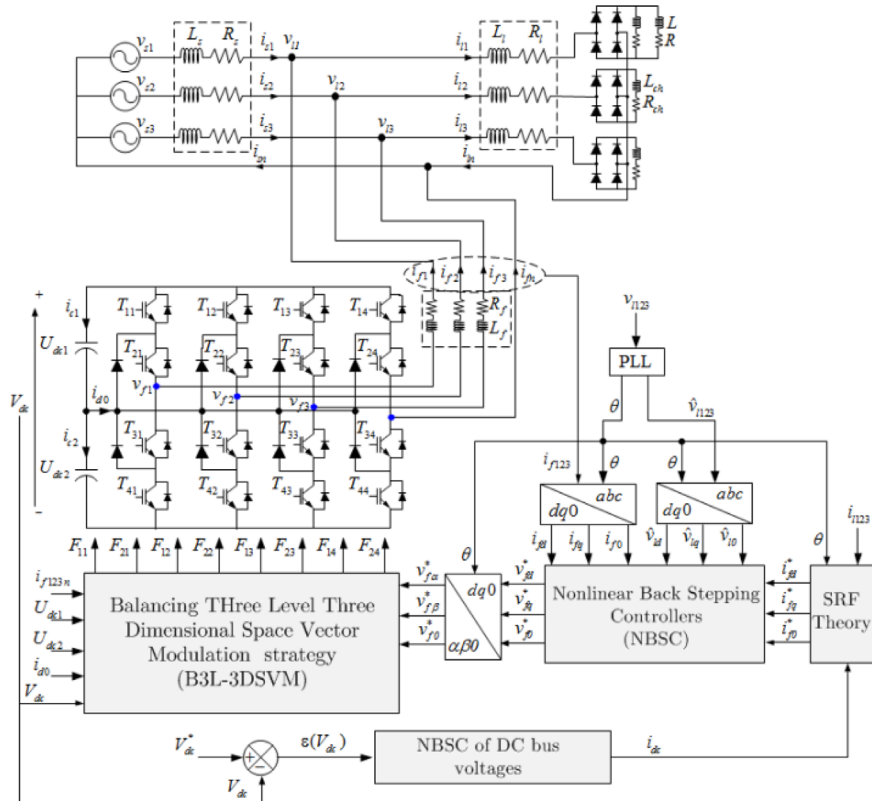

Fig. 10. Schematic diagram of three-level NPC four leg SAPF controlled by proposed B3L-3DSVM using SRF theory and Nonlinear Back Stepping Controllers (NBSC).

3.4.1.2. Voltage truth table at the capacitor terminals. To select the voltage vector in both redundant vectors to be applied to each redundant state, apply redundancy that tends to eliminate the unbalanced or the error between the capacitors voltages (U_{dc1} and U_{dc2}). For this, we defined the stats of the error between the two voltage capacitors ($U_{dc1} - U_{dc2}$) by the logic function M as follow.

$$M = \begin{cases} 1 & si & U_{dc1} - U_{dc2} \geq 0 \\ 0 & si & U_{dc1} - U_{dc2} \leq 0 \end{cases} \tag{14}$$

Table 6 summarizes the stats M of the error between the two voltage capacitors ($U_{dc1} - U_{dc2}$).

Finally the association of two truth Tables 5 and 6 allows the final synthesis of the balancing table of dc bus capacitor voltages. Table 7 summarizes the choice of redundancy voltage vector applying in all possible tetrahedrons in the different sub-prisms of different prisms to balancing the dc bus capacitor voltages.

Referring to Table 7, we can express the redundancy (Red) to apply by the following logical formula:

$$Red = [M.G + (1-M).(1-G)].A + [M.(1-G) + G.(1-M)].B \tag{15}$$

After the redundancy voltage vector for both redundant voltage vectors is selected, we are presented in Fig. 7 the switching pulses and the distribution of voltage vectors to be applied in the first tetrahedron of the first sub-prism of first prism for a one switching period. This tetrahedron is constructed by the combination of the five voltage vectors ($v_{40}, v_{67}, v_{76}, v_{79}, v_{80}$) and we are the two redundant voltage vectors v_{40} and v_{80}.

Fig. 7a shows the gate switching pulses in the case of voltage vector v_{40} is selected and Fig. 7b shows the gate switching pulses in the case of voltage vector v_{80} is selected.

4. Reference harmonic currents generation

Fig. 8 shows a block diagram of synchronous reference frame (SRF) theory based on PLL for generate the reference harmonic currents through the extraction of fundamental loads active and reactive currents. This theory and all steps are presented and described in detail in our previous work [3,30].

The three phase loads currents are converted in the dq0-axes by a rotational frame synchronous with the Eq. (16).

$$\begin{bmatrix} i_{ld} \\ i_{lq} \\ i_{l0} \end{bmatrix} = \begin{bmatrix} \sin(\hat{\theta}) & \sin\left(\hat{\theta} - \frac{2\pi}{3}\right) & \sin\left(\hat{\theta} + \frac{2\pi}{3}\right) \\ \cos(\hat{\theta}) & \cos\left(\hat{\theta} - \frac{2\pi}{3}\right) & \cos\left(\hat{\theta} - \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_{l1} \\ i_{l2} \\ i_{l3} \end{bmatrix} \tag{16}$$

$\hat{\theta}$ is the source voltages phase angle and it is determine and delivered by the Phase Lock Loop (PLL).

After the loads currents i_{ld} and i_{lq} in the *dq0-axes* (active component i_{ld} and oscillating component i_{lq}) are determined, it is necessary to pass the active component i_{ld} for a low pass filter to extract the ac or alternative current component ($\tilde{i}_{ld}$) and dc or direct current ($\bar{i}_{ld}$) component from Eq. (17).

$$i_{ld} = \bar{i}_{ld} + \tilde{i}_{ld} \tag{17}$$

The dc current component $\left(\bar{i}_{ld}\right)$ is associated with the responsibility for fundamental current and the ac current component $\left(\tilde{i}_{ld}\right)$ is associated with the responsibility for harmonics and reactive power compensation. The filter used in the circuit of conventional SRF theory is the 2nd order low pass filter and their cut-off frequency is equal to one half of the fundamental frequency (25 Hz). For harmonic currents and reactive power compensated

in the same time, the reference currents in the *dq0-axes* are given by:

$$i_{fd}^* = \tilde{i}_{ld} + i_{dc}, i_{fq}^* = i_{lq}, i_{fq\alpha}^* = i_{lq\alpha} \ \ and \ \ i_{fq\beta}^* = i_{lq\beta} \tag{18}$$

Table 8
Values of system and simulation parameters.

Parameter	Value
The source voltage and frequency	220 V, 50 Hz
Capacitance of the capacitor $C_{1,2}$	$5*10^{-3}$F, 400 V
Source impedance R_s, L_s	1 mΩ, 1 mH
Line impedance R_l, L_l	1 mΩ, 1 mH
Coupling filter R_f, L_f	0.1 mΩ, 0.1 mH
Loads impedance R_{ch}, L_{ch}	5 Ω, 10 mH
Unbalanced load R, L	5 Ω, 10 mH
Sampling time	10^{-6} s
Switching frequency fs	7000 Hz

Table 9
Values of regulators parameters.

PI	Back Stepping
$f_c = 10 \ kHz$	$K_1 = k_2 = k_3 = 8e^6$.
$f_{ds} = 4 \ Hz$	$K_{Vdc} = 100$.
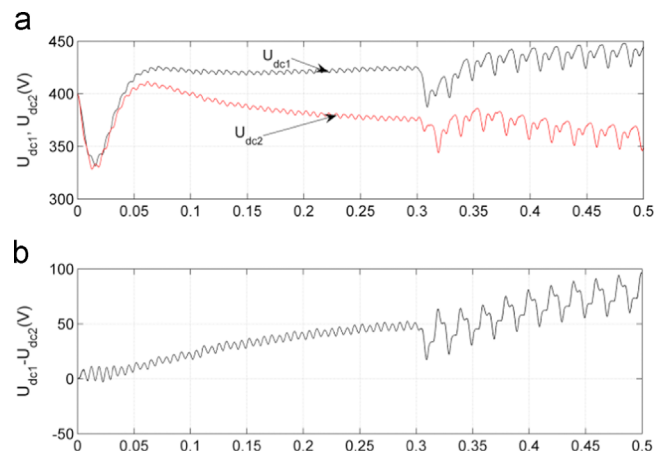
Fig. 11. Performance of three-level NPC four leg inverter controlled by C3L-3DSVM under unbalanced loads, (a) dc bus voltage capacitors (U_{dc1} and U_{dc2}), (b) error between the two dc bus voltage capacitors.
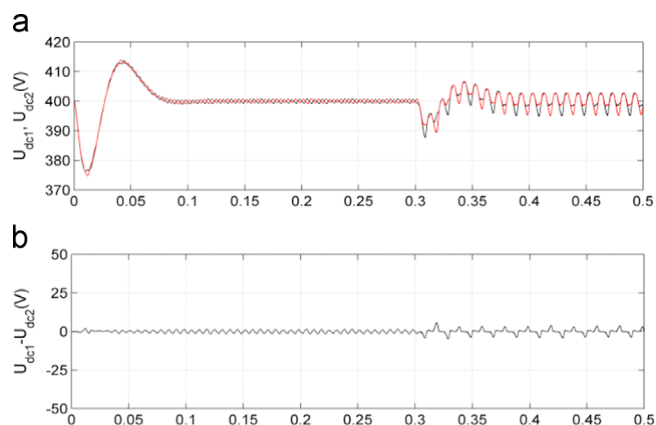
Fig. 12. Performance of three-level NPC four leg inverter controlled by proposed B3L-3DSVM under unbalanced loads, (a) dc bus voltage capacitors (U_{dc1} and U_{dc2}), (b) error between the two dc bus voltage capacitors.

5. SAPF injected currents and DC bus voltages regulation

For an effective operation of SAPF, it is necessary to minimize the error between the SAPF injected currents and there references, and maintain constant the two dc bus voltage capacitors of three-level NPC four leg inverter of SAPF. It is realized using a Nonlinear Back-Stepping Controllers (NBSC), the detail concepts of this technique is extended in [3]. The NBSC laws of SAPF injected currents and total dc bus voltage regulation is given by. (Figs. 9 and 10)

$$v_{fd}^* = L_f k_1 (i_{fd}^* - i_{fd}) + L_f \frac{d}{dt} i_{fd}^* + R_f i_{fd} - L_f \omega i_{fq}$$
$$- L_f k_1 k_{V_{dc}} (V_{dc}^* - V_{dc}) - L_f k_{V_{dc}} \frac{d}{dt} (V_{dc}^* - V_{dc}) + v_{ld}$$
$$v_{fq}^* = L_f \frac{d}{dt} i_{fq}^* + R_f i_{fq} + L_f \omega i_{fd} + L_f k_2 (i_{fq}^* - i_{fq}) + v_{lq}$$
$$v_{fo}^* = L_f \frac{d}{dt} i_{fo}^* + R_f i_{fo} + L_f k_3 (i_{fo}^* - i_{fo}) + v_{lo} \qquad (19)$$

Fig. 4 shows a block diagram of Nonlinear Back Stepping Controllers (NBSC) for SAPF injected currents and dc bus voltages regulation.

6. Simulation results

In order to confirm the viability of the proposed B3L-3DSVM strategy, a simulation model as shown in Fig. 4 has been developed using Sim Power Systems and S-Function of MATLAB. The objectives of these simulation are the study of two different aspects: (a) The unbalance of dc bus voltage capacitors and the improvement of output voltages quality for three-level four leg NPC inverter rating in comparison with three-level NPC four leg SAPF controlled by conventional three-level 3D SVM due to three-level NPC four leg SAPF controlled by new balancing three-level 3D SVM. (b) The effects of NBSC for the stabilization of dc bus voltages and the elimination of the overshoot, the elimination of the error between the SAPF injected currents and their references, compensation of harmonics and reactive power, zero sequence current elimination under unbalanced loads at $t = 0.4$ s. The values of system and simulation parameters are presented in Table 8 and the values of regulators parameters are presented in Table 9.

6.1. Performance of B3L-3DSVM based control strategy of 3 L NPC 4L inverter under unbalanced loads

We present in these simulations of the two strategies for gate switching pulses generation (C3L-3DSVM and B3L-3DSVM), the dc bus voltage capacitors and the error between the two dc bus voltage capacitors Figs. 11 and 12(a and b), the switching frequency of both strategies is 7000 Hz. It can be observed from these Figs that in case of C3L-3DSVM strategy Fig. 11, the dc bus voltage capacitors (U_{dc1} and U_{dc2}) are rapidly diverge and the error between the two dc bus voltage capacitors is vary increasing but in B3L-3DSVM strategy gives very good balancing for dc bus voltage capacitors (Udc1 and Udc2) with an zero error between these dc bus voltage capacitors before and after unbalanced loads Fig. 12 which verifies the effectiveness of B3L-3DSVM for controlling the

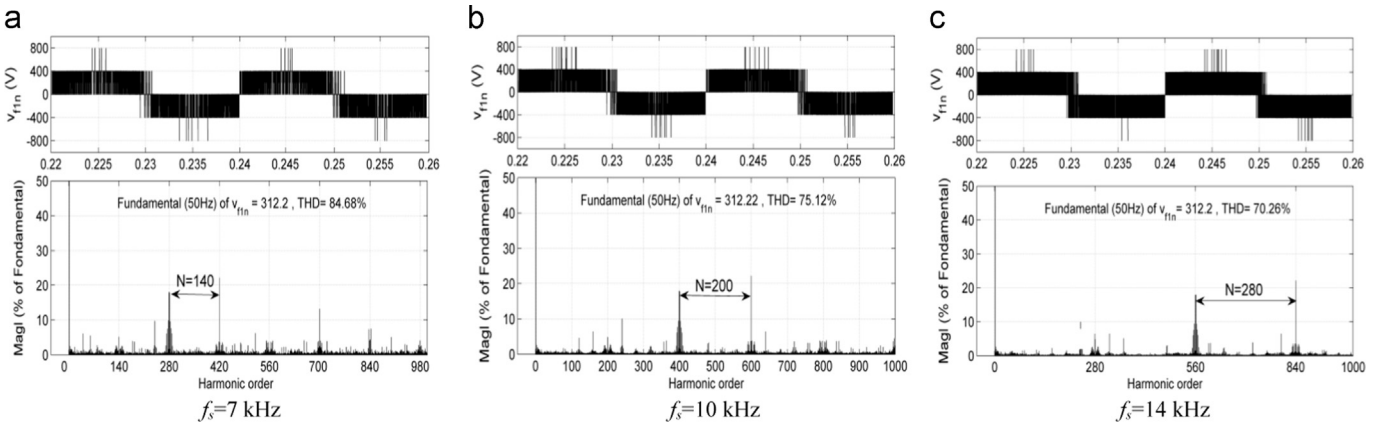**Fig. 13.** Output voltages phase-to-neutral v_{f1n} and their THDv of three-level NPC four leg inverter controlled by C3L-3DSVM. (a): $f_s = 7$ kHz, (b): $f_s = 10$ kHz, (c): $f_s = 14$ kHz.
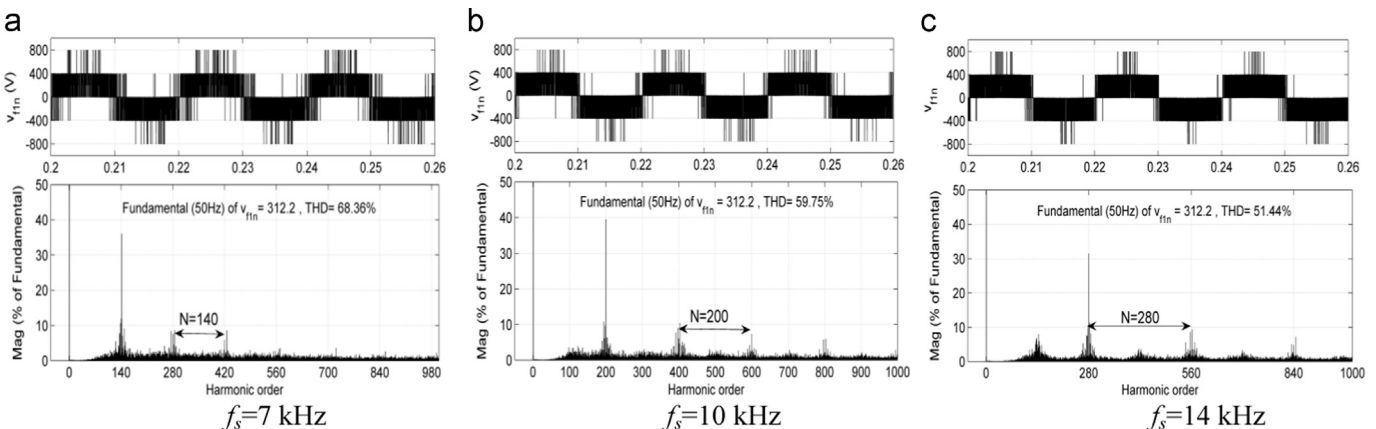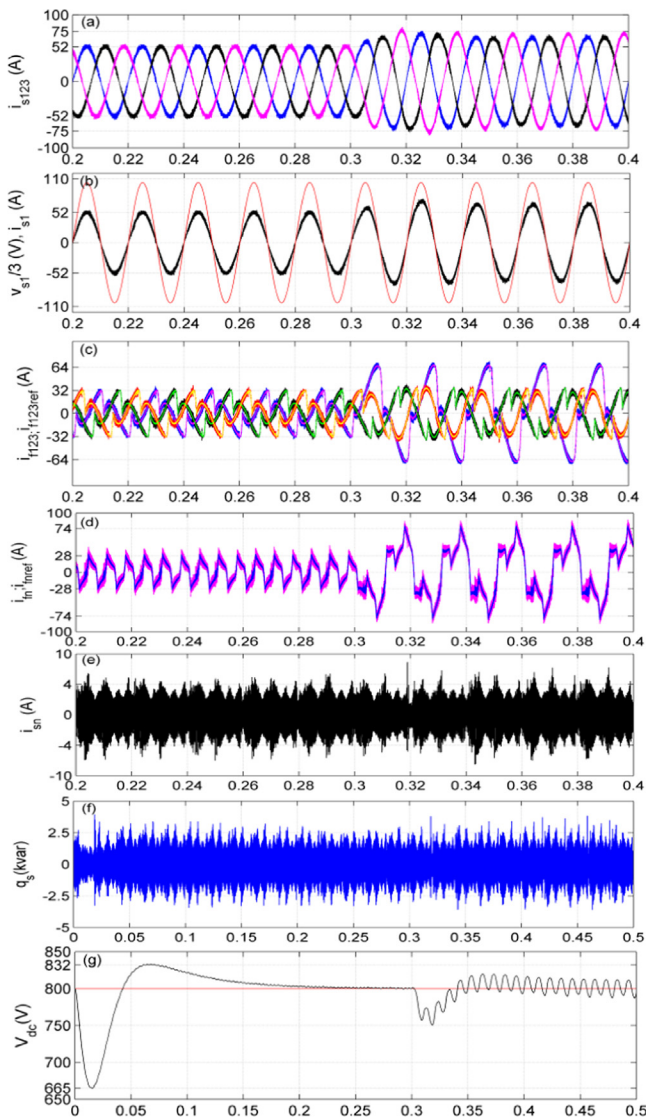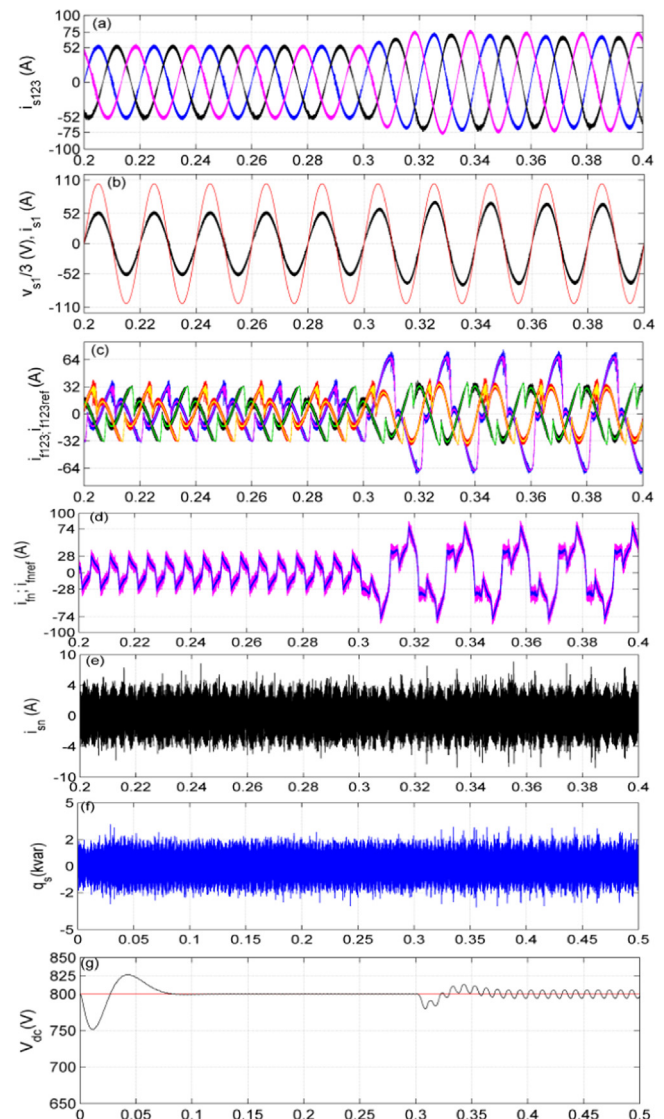

Fig. 14. Output voltages phase-to-neutral v_{f1n} and their THDv of three-level NPC four leg inverter controlled by proposed B3L-3DSVM. (a): $f_s = 7$ kHz, (b): $f_s = 10$ kHz, (c): $f_s = 14$ kHz.

Fig. 15. Performance of three-level NPC four leg SAPF controlled by C3L-3DSVM using conventional PI under unbalanced loads.

Fig. 16. Performance of three-level NPC four leg SAPF controlled by B3L-3DSVM using conventional PI under unbalanced loads.

three-level NPC four-leg inverter in terms of balancing for dc bus voltage capacitors.

Figs. 13 and 14(a, b and c) show the waveform of three-level NPC four leg inverter output phase-to-neutral voltage v_{f1n} and their analysis harmonics of the three-level NPC four leg inverter controlled by the two strategies of gate switching pulses generation with three various switching frequency values (7, 10 and 14 KHz). Through the harmonics analysis 3 cycles of three-level NPC four leg inverter output phase-to-neutral voltage has been selected for every analysis, these results demonstrate that for same conditions, the output voltage distortion harmonics values (THDv) are decreased significantly even though the switching frequency is increase, and the distribution of output phase-to-neutral voltage harmonics for both strategies are approximately centered around the multiples of report N between the period of switching frequency Ts and the period of output voltage T=0.02 s as follows.

For the case of $f_s=7\,kHz$, $T_s=1/7000\,s$ and $N=0.02*7000$ thus $N=140$ period, Figs. 13 and 14a.
For the case of $f_s=10\,kHz$, $T_s=1/10000\,s$ and $N=0.02*10000$ thus $N=200$ period, Figs. 13 and 14b.

For the case of $f_s=14\,kHz$, $T_s=1/14000\,s$ and $N=0.02*14000$ thus $N=280$ period, Figs. 13 and 14c.

According to THDv obtained in both strategies (C3L-3DSVM and B3L-3DSVM) under same switching frequency, it can be observed that the output phase-to-neutral voltage harmonics are greatly reduced in the case of three-level NPC four leg inverter controlled by B3L-3DSVM compared to C3L-3DSVM which also verifies the effectiveness of B3L-3DSVM for controlling the three-level NPC four-leg inverter in terms of output voltages quality.

6.2. Performance of B3L-3DSVM based control strategy of 3 L NPC 4L SAPF under unbalanced loads

Figs. 15 and 16 show the performances of three-level NPC four leg SAPF controlled by the two gate switching pulses generation strategies (C3L-3DSVM and B3L-3DSVM) using the conventional PI for SAPF injected currents and the dc bus voltage capacitors regulation, the switching frequency of both strategies is 7000 Hz. Each figure is divided into seven groups: (a) source currents (i_{s123}); (b) first phase source current and corresponding voltage; (c) SAPF
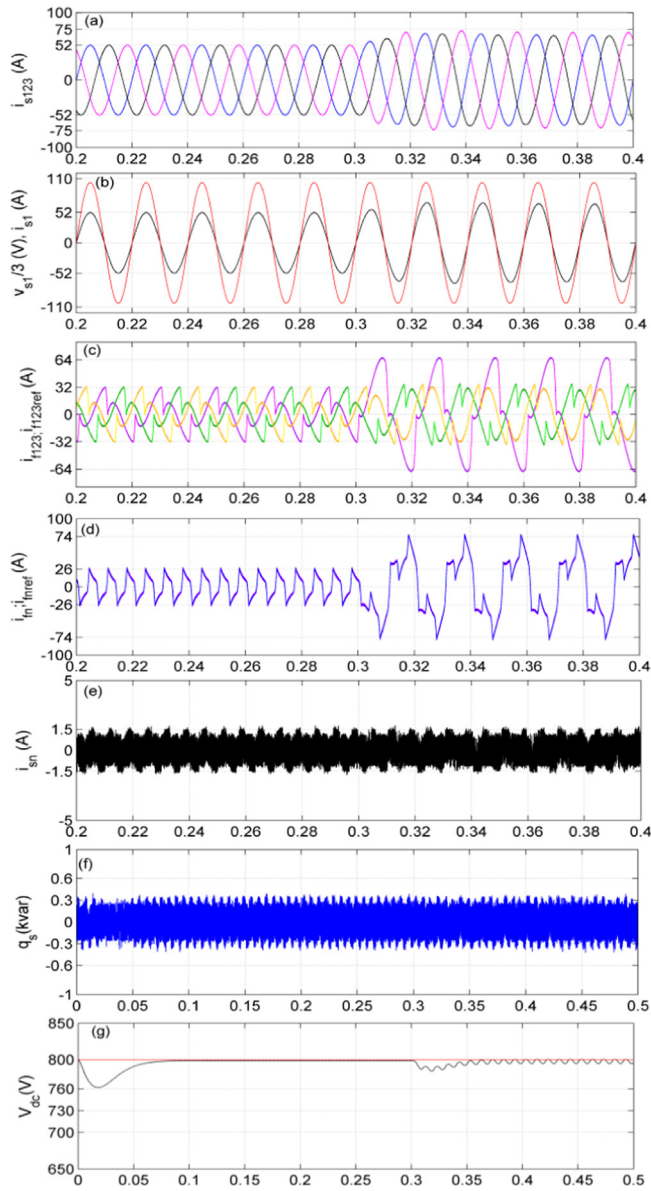
Fig. 17. Performance of three-level NPC four leg SAPF controlled by B3L-3DSVM using Nonlinear Back Stepping Controllers (NBSC) under unbalanced loads.

injected currents (i_{f123}) and there harmonic references ($i_{f123ref}$); (d) the current (i_{fn}) injected by the SAPF through the fourth leg of the inverter and its reference (i_{fnref}) that is supposed to eliminate the current circulating in the neutral wire source (i_{sn}); (e) neutral wire source current (i_{sn}); (f) source reactive power (q_s); and (g) total dc bus voltage (V_{dc}). In both the cases of gate switching pulses generation before and after unbalanced loads at $t=0.3$ s, The three-level NPC four leg SAPF with conventional PI is operate correctly to eliminate the harmonic currents and zero sequence current, and to compensate the reactive power. It can be observed from Figs. 15 and 16 that the source currents are sinusoidal with a unity power factor operation in the two strategies C3L-3DSVM and B3L-3DSVM Figs. 15 and 16(a and b), the SAPF injected currents have been tracked their harmonic references with zero error in the two strategies Figs. 15 and 16(c and d), the neutral wire source current is reduced in the two strategies, as well as less oscillations in the case of B3L-3DSVM then the C3L-3DSVM application before and after unbalanced loads Figs. 15 and 16(e), the reactive power in the source is oscillated around the zero before and after unbalanced loads, as well as smaller magnitude in the case of B3L-3DSVM (2 kvar) Figs. 15 and 16(f), it can be also observed from Figs. 15 and 16(g) that in case of C3L-3DSVM Fig. 15(g), the total dc bus voltage has an undershoot of 135 V and an overshoot of 32 V at the engagement of the SAPF but in B3L-3DSVM an undershoot of 50 V and an overshoot of 25 V at the engagement of the SAPF Fig. 16(g) and also in case of C3L-3DSVM, the total dc bus voltage has taken 2 s to established after the engagement of the SAPF at $t=0$ s and 1 s after the unbalanced loads at $t=0.3$ s but in B3L-3DSVM has taken only 1 s to established after the engagement of the SAPF and 0.5 s after the unbalanced loads which verifies the robustness and the effectiveness of B3L-3DSVM for controlling the three-level NPC four-leg inverter based SAPF in terms of source currents ripple, magnitude of neutral wire current, compensation of reactive power, and the elimination of overshoot and undershoot under unbalanced dc bus voltage capacitors and loads.

6.3. Performance of NBSC with B3L-3DSVM based control strategies of 3 L NPC 4L SAPF under unbalanced loads

Fig. 17 show the performances of three-level NPC four leg SAPF controlled by B3L-3DSVM using the Nonlinear Back Stepping Controllers (NBSC) for SAPF injected currents and the dc bus voltage capacitors regulation, the switching frequency of both strategies is 7000 Hz. In this case, the three-level NPC four leg SAPF
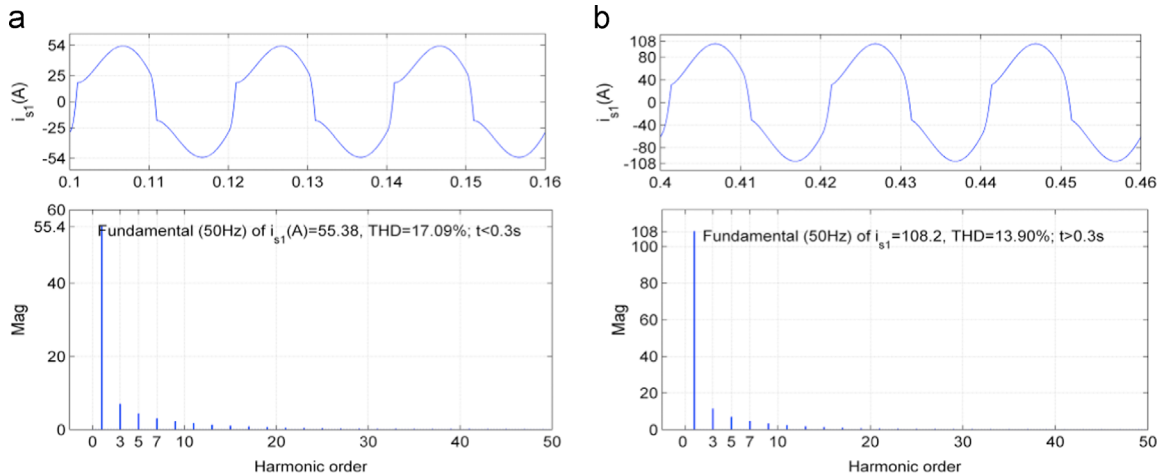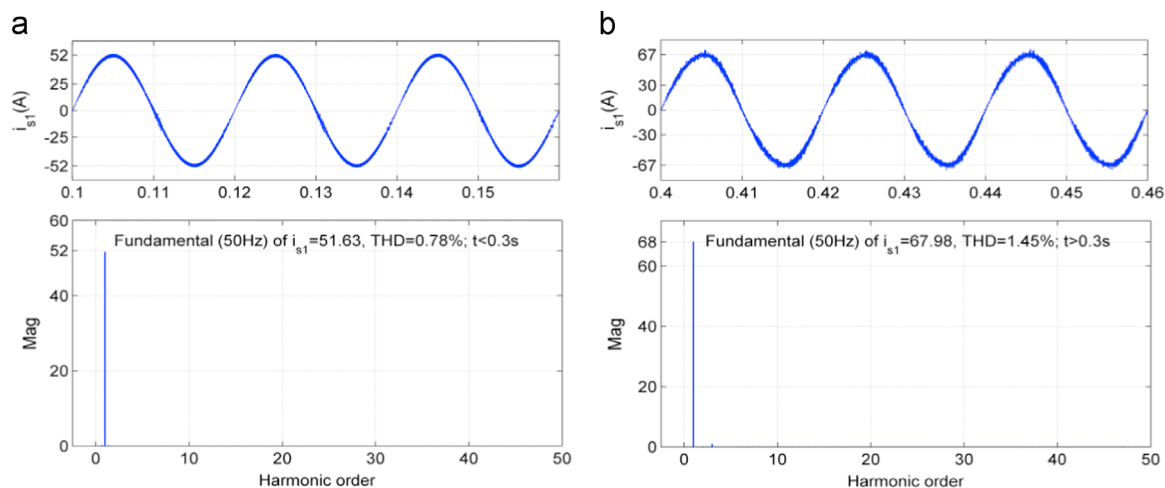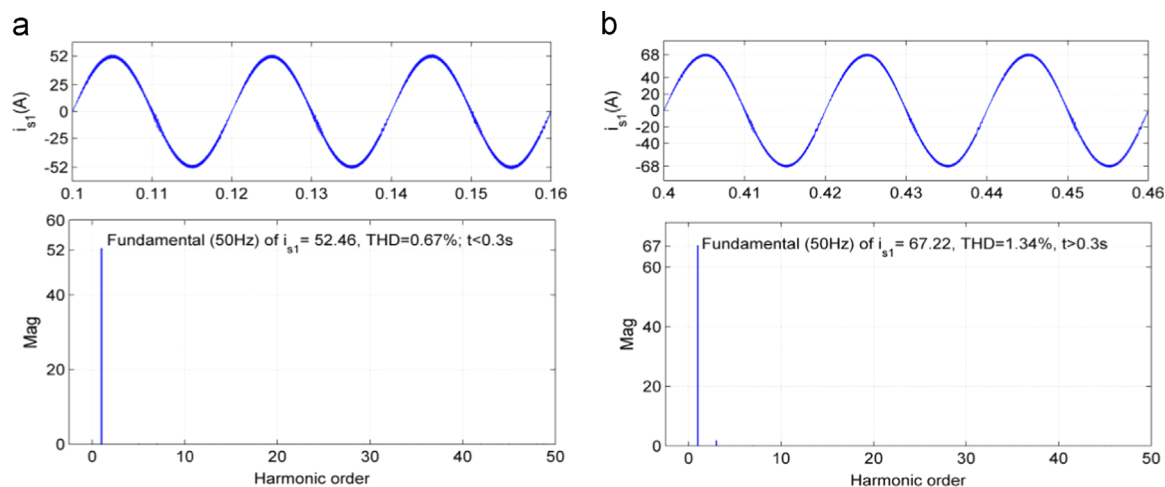

Fig. 18. Waveforms and harmonics analysis of source current without compensation: (a) Before unbalanced loads and (b) after unbalanced loads.

Fig. 19. Waveforms and harmonics analysis of source current with an three-level NPC four leg SAPF controlled by C3L-3DSVM using conventional PI: (a) before unbalanced loads and (b) after unbalanced loads.

Fig. 20. Waveforms and harmonics analysis of source current with an three-level NPC four leg SAPF controlled by B3L-3DSVM using conventional PI: (a) before unbalanced loads and (b) after unbalanced loads.

with Nonlinear Back Stepping Controllers (NBSC) is perfectly operate to eliminate the harmonic currents and zero sequence current, and to compensate the reactive power before and after unbalanced loads at $t=0.3$ s. It can be observed in this case that the source currents are perfectly sinusoidal with a unity power factor operation and less switching ripple then the conventional PI applications Fig. 17(a and b), the SAPF injected currents have been tracked their harmonic references with zero errors and also less switching ripple then the conventional PI applications Fig. 17(c and d), the neutral wire source current is perfectly reduced before and after unbalanced loads from 4A using conventional PI to 1.5A using NBSC Fig. 17(e), the reactive power in the source is also vary reduced from 2kvar using conventional PI to 0.3kvar using NBSC Fig. 17(f), the total dc bus voltage has an undershoot of 40 V and an overshoot of 0 V at the engagement of the SAPF and also has taken 0.75 s to established after the engagement of the SAPF at $t=0$ s and 0.5 s after the unbalanced loads at $t=0.3$ s Fig. 17(g) which also verifies the effectiveness and the robustness of NBSC associated with B3L-3DSVM for controlling the three-level NPC four-leg SAPF in case of unbalanced dc bus voltage capacitors and loads.

Figs. 18,19 and 21 show the waveforms and harmonics analysis of source current without and with compensation before and after unbalanced loads. The source current harmonics without compensation are create to be 17.09% before unbalanced loads and 13. 90% after unbalanced loads Fig. 18(a and b) and it reduces with

compensation by three-level NPC four leg SAPF controlled by C3L-3DSVM using conventional PI to 0.78% before unbalanced loads and 1.45% after unbalanced loads Fig. 19(a and b). The three-level NPC four leg SAPF controlled by proposed B3L-3DSVM using conventional PI gives 0.67% before unbalanced loads and 1.34% after unbalanced loads Fig. 20(a and b), and using Nonlinear Back Stepping Controllers (NBSC) gives 0.35% before unbalanced loads and 0.97% after unbalanced loads Fig. 21(a and b), which are vary less than the three-level NPC four leg SAPF controlled by proposed B3L-3DSVM using conventional PI which also verifies the effectiveness of NBSC associated with B3L-3DSVM for controlling the three-level NPC four-leg SAPF in terms of source current harmonics reduction in case of unbalanced dc bus voltage capacitors and loads. Table 10 shows the performance comparison for all simulation tests offered in this work.

7. Conclusion

A B3L-3DSVM strategy for generate the gate switching pulses and balancing the dc bus voltage capacitors in same times of a three phase three level NPC four-leg SAPF has been proposed with an Nonlinear Back-Stepping Controllers (NBSC) for regulated the dc bus voltage capacitors and the SAPF injected currents for power quality improvement in a four wire distribution network. The use
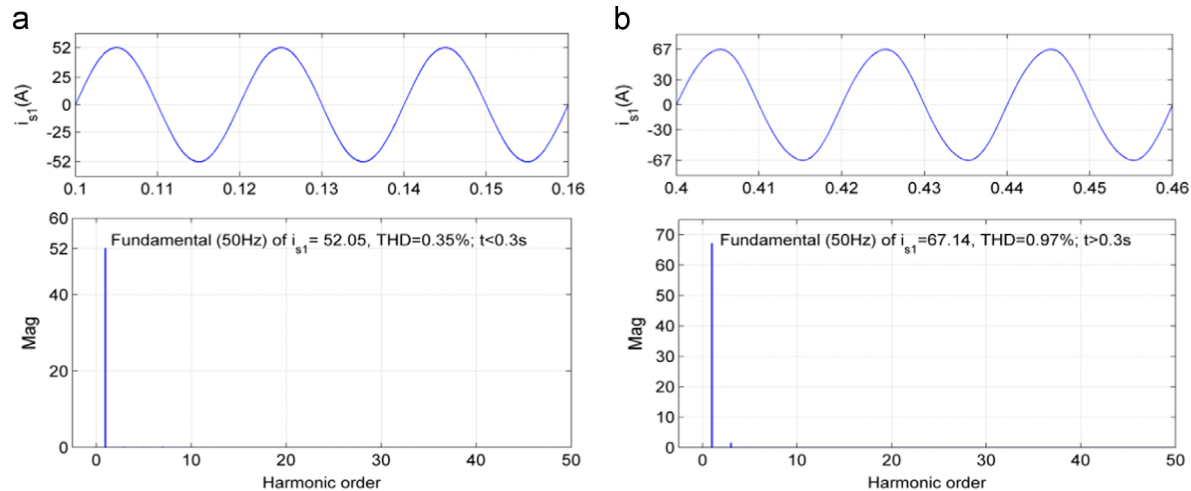
Fig. 21. Waveforms and harmonics analysis of source current with an three-level NPC four leg SAPF controlled by B3L-3DSVM using nonlinear back-stepping controllers: (a) before unbalanced loads and (b) after unbalanced loads.

Table 10
Performances comparison for all simulation tests offered in this work.

	C3L-3DSVM		B3L-3DSVM			
	PI		PI		NBSC	
	t < 0.3 s	t > 0.3 s	t < 0.3 s	t > 0.3 s	t < 0.3 s	t > 0.3 s
Source current THD (%)	0.78%	1.45%	0.67%	1.34%	0.35%	0.97%
Oscillations of neutral source current (A)	4A		4A		1.5A	
Oscillations of reactive power (kvar)	2.5 kvar		2 kvar		0.3 kvar	
Total dc bus voltage undershoot (V)	135 V	50 V	50 V	20 V	40 V	15 V
Total dc bus voltage overshoot (V)	32 V	18 V	25 V	10 V	Zero	Zero
Times of total dc bus voltage stabilization (s)	0.2 s	0.1 s	0.1 s	0.075 s	0.075 s	0.05 s

of B3L-3DSVM has a satisfactory performances of a three level four-leg NPC SAPF in terms of dc bus voltage capacitors balancing, inverter output voltages quality, and dynamic response during unbalanced loads than the C3L-3DSVM strategy application while also operating at a vary lower switching frequency which has been confirmed by simulation results, and the proposed strategy is effective for evaluated each of the 81 voltage vectors to selected a capable vector for both redundant vectors in each tetrahedron that reduced the error between the two dc bus voltage capacitors. Since it perfectly balanced and established the dc bus voltage capacitors under unbalanced loads, it has been discovered as an efficient solution to the problem of unbalanced dc bus voltage capacitors. For the dc bus voltage capacitors and the SAPF injected currents of three level NPC four-leg SAPF, the used of NBSC has given vary good performances in terms of references tracking for the total dc bus voltage and SAPF injected currents under unbalanced loads, maintain constant the total dc bus voltage, dc bus voltage overshoot and undershoot elimination, vary lower harmonics and switching ripple in source currents, and the reactive power compensation. The simulation results has also demonstrated the effectiveness and the robustness of the NBSC associated with B3L-3DSVM for controlling the three phase three level NPC four-leg SAPF.

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