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Self Tuning Filter and Fuzzy logic Control of Shunt Active Power Filter for Eliminates the Current Harmonics Constraints under Unbalanced Source Voltages and Loads Conditions

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Abstract

Shunt active power filters (SAPFs) are modern filtering technologies for source current harmonic elimination and source reactive power compensation of nonlinear loads. In the case of normally balanced source voltages, the SAPFs are controlled to eliminate a wide range of source current harmonics and compensate the source reactive power generated by non-linear loads to provide source current functions with maximum power factor. However, if source voltages are unbalanced and/or distorted, these control objectives cannot be achieved, which impacts the SAPFs performances. In the present paper, we propose a new modification to extend the stable dynamic range and to enhance the transient response of a classical phase locked loop (CPLL). An enhanced phase locked loop (EPLL) based on a self tuning filter (STF) and fuzzy logic control (FLC) associated with SRF theory are used in four leg shunt active power filter control under unbalanced source voltages and nonlinear loads. The aim is to enable the SAPFs to reach a higher compensation level of reactive power and current harmonics for all cases of source voltages and nonlinear loads for the limits specified in IEEE Std. 519. The success, robustness, and effectiveness of proposed control circuits are demonstrated through simulation, using Sim Power Systems and S-Function of MATLAB/SIMULINK.

Keywords: Four-leg Shunt Active Power Filter (4LSAPF); Enhanced Phase Locked Loop (EPLL); Self Tuning Filter (STF); Fuzzy Logic Control (FLC); Harmonics; Reactive power.

1. Introduction

Industrial and domestic equipment make widespread use of single and three phase unbalanced nonlinear loads based on power electronics, such as rectifiers and speed drivers [1]. Increases in these loads in distribution systems cause harmful effects and problems, such as increased distortion level of voltages and currents, increased harmonic currents and excessive zero sequence harmonic, unbalance and distortion in source waveform currents/voltages, increased losses, poor power factor, reduced efficiency, and disruptions to electronic equipment connected to electrical networks [2].

The three or four leg shunt active power filters (SAPFs) are modern filtering technologies and provide an effective solution to remedy and eliminate most power quality problems of harmonic currents and reactive power in three phase, three or four wire electrical networks [3, 4]. They can provide effective solutions to improve the main power factor through the compensation of reactive power and current harmonics at the point of common coupling (PCC) of the electrical network. The most powerful converter used in a four leg shunt active power filter to compensate four wire electrical networks is the four leg voltage source inverter (4LVSI) [5, 6]. The advantage of this inverter configuration is that it compensates the zero sequence current circulating in the neutral wire of four wire electrical networks [7, 8].

The good performances achieved by the four leg shunt active power filter depend on the techniques and strategies selected in the three parts of the control circuit for accuracy determination of switching signals for the 4LVSI (part 1), better robustness and stabilization of 4LVSI current harmonics and dc-link voltage capacitor controllers (part 2) and good tracking quality and dynamic of reference current harmonics identification (part 3). Several researchers have described the effect of reference current harmonics identification (part 3) on

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the performance of three or four leg shunt active power filters. To improve SAPF performances and reduce the power quality problems, researchers [9, 10] have described the pq theory on the performance of 3LSAPF aimed at reducing these problems. Patel et al. [11] proposed the Synchronous Reference Frame theory (SRF) for reference current harmonics identification based 3LSAPF, and P. Kanjiya et al. [5, 12] used the instantaneous power theory, called pq0 theory, for reference current harmonics identification with PI for dc-link voltage capacitor regulation and Hysteresis control for switching signals determination of 4LSAPF.

In the case of balanced source voltages and loads, the SAPF based on these theories delivers good performances and is able to reduce power quality problems. The SAPF based on SRF theory confirmed itself as a simple structure, easier to implement than pq0 theory and with good reference current harmonics identification. This theory is analyzed in various SAPF and DSTATCOM configurations, such as 3LSAPF and 3L DSTATCOM [13, 14]. This concept was extended by simulation studies to four leg SAPF [9, 15] and in four leg DSTATCOM [16]. The SRF theory extracted the reference current harmonics directly using a low pass filter (LPF).

There are many power quality problems and difficulties involved in utilizing this theory in the case of unbalanced source voltages and loads, such as deformation of the synchronization between the source currents/voltages and control circuit, and between the SAPF and distribution system. These in turn result in problems, such as poor identification of harmonic currents, unbalance and distortion in source waveform currents/voltages, poor power factor in three phase four wire electrical networks, and reduced efficiency of SAPF connected to distribution systems [17]. In these cases other researchers proposed numerous modifications to SRF theory, suggesting good reference current harmonics identification to remedy these problems and difficulties. Benchouia et al. [18] replaced the low pass filter (LPF) by a Self Tuning Filter (STF) to enhance the SRF Theory; Stastny et al. [19] discussed the zero cross theory based on CPLL; and Bhattacharjee et al. [13] described the association of classical phase locked loop (CPLL) with SRF theory for generating unit reference signals to achieve good harmonic currents identification through the extraction of fundamental current components of reference signals. These suggested modifications are not favorable and not fully effective in the case of distorted and unbalanced source voltages due to the limitation and non linearity of a CPLL based linear PI controller [18–21].

To remedy these limitations, to stabilize the dynamic range, and to enhance the response of a CPLL, several researchers suggested modifications to and enhancements of the CPLL based on a linear PI controller. Lanza et al. [22] used sliding mode control to improve the CPLL; Lei et al. [23] applied the injection locked synchronous oscillator to replace the conventional voltage controlled oscillator (VCO) to improve the CPLL; Qasim et al. [24] used the PLL based artificial neural network for harmonic current identification to improve SAPF performances; the present authors in [25] improved the CPLL by using an STF for harmonic current identification through the extraction of fundamental components of the unbalanced source voltages of a four leg SAPF and DSTATCOM for improved performances. This Enhanced EPLL based of linear PI gives very good performances in terms of extracting fundamental components under unbalanced source voltages. The drawbacks of this EPLL are unstable and susceptible to external disturbances, the dynamic transient response is very long, and the dynamics of loops in unstable self oscillations, and in the uncertainty of VCO parametric yield the degradation of EPLL performances. Hence, under various cases of source voltages and nonlinear loads, SAPFs with very good demonstrations and intelligent control circuit are capable of achieving a unity power factor with minimum current harmonics in four wire electrical networks.

In this paper an effective EPLL based on STF and FLC is proposed and discussed with the aim being to achieve a robust EPLL and to render the EPLL operation independent from the magnitude of unbalanced source voltages. The modification focuses on replacing the linear PI controller with a fuzzy logic controller and using STF to estimate the fundamental components. This EPLL associated with SRF theory makes the third part of the control circuit able to provide good identification of reference current harmonics with good tracking quality and dynamics. In the first part we use Three Dimensional Space Vector Modulation (3DSVM) for accuracy determination of switching signals for the 4LVSI based 4LSAPF. In the second part we use the Nonlinear Back Stepping Controllers (NBSC) of 4LVSI current harmonics and dc-link voltage capacitor controllers, these two techniques – 3DSVM and NBSC – are used and discussed in several previous works [15, 16] which demonstrate good performances in terms of THDv of 4LSAPF output voltages, power losses and switching frequency in the application of 3DSVM, and in terms of robustness, reference tracking for the dc-link voltage capacitor and 4LSAPF injected currents under unbalanced loads, harmonics and switching ripple in source currents, reactive power compensation, overshoot and undershoot in the dc-link voltage capacitor, and error between the SAPF injected currents and the references under unbalanced loads in the application NBSC. This paper is organized as follows: Section II gives the power configuration and mathematical model of the three four-leg SAPF. Section III presents the CPLL and conventional SRF theory with their detailed calculations. The proposed EPLL based on STF and FLC with their detailed calculations is presented in Section IV. Section V compares the performances of the proposed EPLL and the CPLL. Section VI compares the performances of 4LSAPF based on the proposed EPLL and the CPLL under unbalanced source voltage and load conditions. Finally, Section VII contains the conclusions drawn in this paper.

2. Power system configuration and control circuit of four leg SAPF

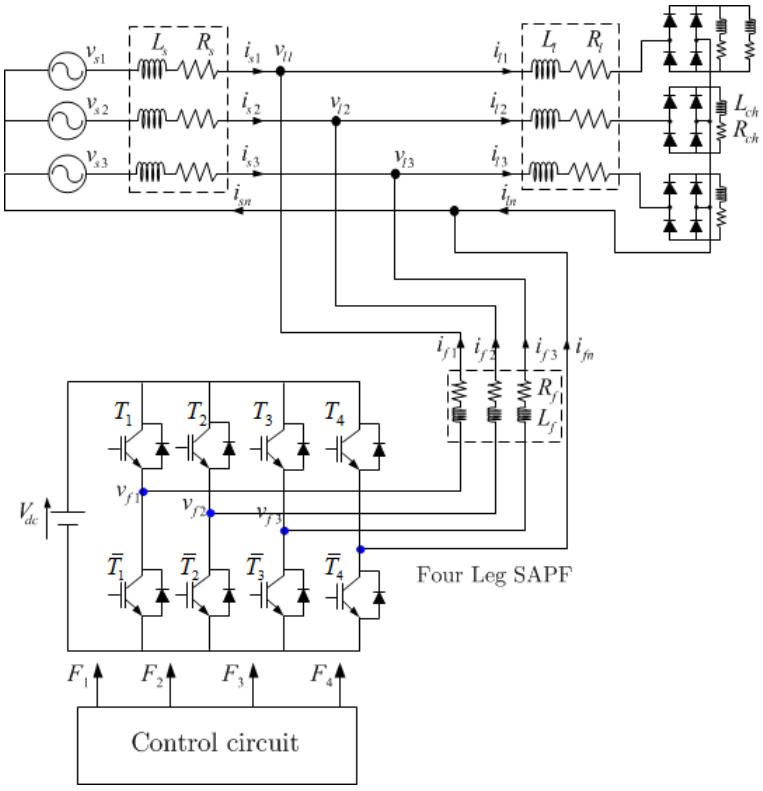

Figure 1: Schematic block of three phase four leg shunt active power filter

The schematic block of a power distribution system with 4L SAPF is illustrated in Fig. 1, the 4L SAPF is connected to a three phase four wire electrical network in a Point of Common Coupling (PCC) with source inductors and resistors (L_s and R_s) feeding three single phase nonlinear loads. The 4L SAPF is connected in the distribution system by an $L_f - R_f$ coupling filter for reducing the ripple in 4L SAPF injected currents (i_{f123n}). These currents are injected in the distribution system at the PCC to compensate the load current harmonics and the reactive power [4, 5].

The variables for the power distribution system with 4L SAPF controllers are the PCC voltages (v_{l123}), source currents (i_{s123n}), load currents (i_{l123n}) and dc-link voltage capacitor (V_{dc}) of 4L VSI used in SAPF. The 4L SAPF mathematical model is defined in dq0 frame as follows:

$$\begin{cases} \frac{di_{fd}}{dt} = -\frac{R_f}{L_f} i_{fd} + \omega i_{fq} + \frac{1}{L_f} v_{fd} - \frac{1}{L_f} v_{ld} \\ \frac{di_{fq}}{dt} = -\frac{R_f}{L_f} i_{fq} - \omega i_{fd} + \frac{1}{L_f} v_{fq} - \frac{1}{L_f} v_{lq} \\ \frac{di_{fo}}{dt} = -\frac{R_f}{L_f} i_{fo} + \frac{1}{L_f} v_{fo} - \frac{1}{L_f} v_{lo} \\ \frac{dV_{dc}}{dt} = -\frac{1}{C} i^*_{dc} \end{cases} \quad (1)$$

2.1. Control circuit of four leg SAPF

The control circuit of 4LSAPF is illustrated in Fig. 2. This circuit contains three important parts: (i) the switching signals for 4LVSI determination, (ii) 4LVSI current harmonics and dc-link voltage capacitor controllers, and (iii) reference current harmonics identification. The good performances achieved with 4LSAPF depend on the techniques and strategies selected in the three parts of the control circuit.

2.1.1. Nonlinear Back Stepping Controllers (NBSC)

We used Nonlinear Back-Stepping Control (NBSC) for greater robustness and stabilization of current harmonics and dc-link voltage capacitor of 4LVSI based 4LSAPF, to minimize the error between the 4LSAPF injected currents and the harmonic references, and to maintain constant the two dc-link voltage capacitor – the detailed concepts of these techniques are explained in [15]. The NBSC laws of SAPF injected currents and dc-link voltage regulations in the dq0 frame are given by.

$$\begin{cases} v^*_{fd} = L_f k_1 (i^*_{fd} - i_{fd}) + L_f \frac{d}{dt} i^*_{fd} + R_f i_{fd} - L_f \omega i_{fq} - \\ -L_f k_1 k_{V_{dc}} (V^*_{dc} - V_{dc}) - L_f k_{V_{dc}} \frac{d}{dt} (V^*_{dc} - V_{dc}) + v_{ld} \\ v^*_{fq} = L_f \frac{d}{dt} i^*_{fq} + R_f i_{fq} + L_f \omega i_{fd} + L_f k_2 (i^*_{fq} - i_{fq}) + v_{ld} \\ v^*_{fq} = L_f \frac{d}{dt} i^*_{fq} + R_f i_{fq} + L_f \omega i_{fd} + L_f k_2 (i^*_{fq} - i_{fq}) + v_{ld} \end{cases} \quad (2)$$

A block diagram of NBSC used for 4LSAPF injected currents and dc-link voltage capacitor regulations is illustrated in Fig. 3.

2.1.2. Three dimensional space vector modulation (3DSVM)

Many modulation techniques existing in the literature are designed to take into account the important problems of the 4LVSI associated with the switching frequency to reduce the lost power and fix the switching frequency at the same time. Mostly, the 3DSVM technique is used to accurately determine switching signals for the 4LVSI. Due to its simplicity

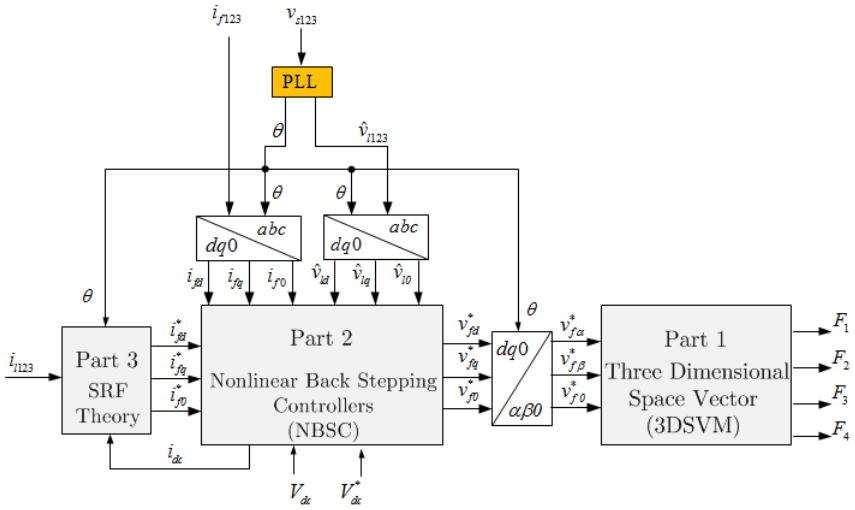

Figure 2: Block diagram control circuit based four leg shunt active power filter

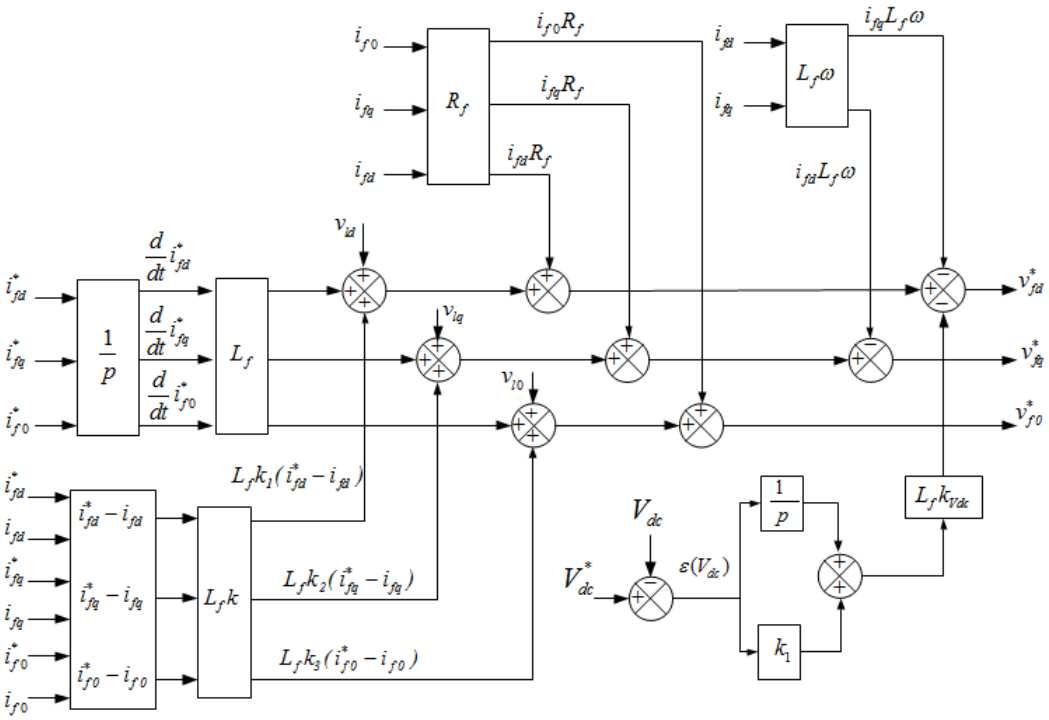

Figure 3: Block diagram of Nonlinear Back Stepping Controllers (NBSC) based 4L SAPF

and ability to fix the switching frequency at the same time, three dimensional space vector modulation in the $\alpha\beta 0$ frame has been employed to determine switching signals for the 4LVSI based 4LSAPF. The detailed concept of this technique is covered in depth in several previous works [8, 26].

2.1.3. Synchronous reference frame (SRF) theory

The synchronous reference frame (SRF) theory based on CPLL for reference harmonic currents identification through the extraction of fundamental active and reactive loads currents is shown in Fig. 4. This theory and all related steps are presented and described in detail in our previous works [15, 16].
The three phase load currents are converted in the dq0 frame by a rotational frame synchronous with the equation (3).

$$\begin{bmatrix} i_{ld} \\ i_{lq} \\ i_{l0} \end{bmatrix} = \begin{bmatrix} \sin(\hat{\theta}) & \sin(\hat{\theta}-\frac{2\pi}{3}) & \sin(\hat{\theta}+\frac{2\pi}{3}) \\ \cos(\hat{\theta}) & \cos(\hat{\theta}-\frac{2\pi}{3}) & \cos(\hat{\theta}-\frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_{l1} \\ i_{l2} \\ i_{l3} \end{bmatrix} \tag{3}$$

$\hat{\theta}$ is the estimated phase angle of source voltages and it is determined and delivered by the CPLL.

After the load currents i_{ld} and i_{lq} in the $dq0$ frame (active component i_{ld} and oscillating component i_{lq}) are determined, it is necessary to pass the active component i_{ld} to a low pass filter to extract the ac or alternative current component ($\tilde{i}_{ld}$) and dc or direct current ($\bar{i}_{ld}$) component from equation (4).

$$i_{ld} = \bar{i}_{ld} + \tilde{i}_{ld} \tag{4}$$

The dc current component ($\bar{i}_{ld}$) is associated with the responsibility for fundamental current and the ac current component ($\tilde{i}_{ld}$) is associated with the responsibility for harmonics and reactive power compensation. The filter used in the circuit of conventional SRF theory is a 2nd order low pass filter and its cut-off frequency is equal to one half of the fundamental frequency (25 Hz). For harmonic currents and reactive power compensated in the same time, the reference currents in the dq0 frame are given by:

$$\begin{cases} i^*_{fd} = \tilde{i}_{ld} + i_{dc} \\ i^*_{fq} = i_{lq} \\ i^*_{fq\alpha} = i_{lq\alpha} \\ i^*_{fq\beta} = i_{lq\beta} \end{cases} \tag{5}$$

3. Classical phase locked loop based of linear PI controller (CPLL-pi)

The classical phase-locked loop (CPLL) is a feedback configuration or controlled circuit used to synchronize the output signal with an input reference signal (phase-locked) [25, 27]. This controlled circuit contains a Concordia transformation (T_{32}) used to obtain the source voltage components in the stationary reference frame ($\alpha\beta$ axes), phase detector ($P(\hat{\theta}_s)$ or PD), a loop filter or linear PI controller (PI or LF) analogous to the low pass filter used for active source voltages component control to zero, and a voltage controlled oscillator (VCO) as shown in Fig. 5. In the present work, the CPLL is used to detect the parameters of fundamental source voltage components ($\hat{\theta}, V_{\max}$) which are given by the following equation:

$$\begin{cases} v_{s1} = V_{\max}\sin(\omega t) \\ v_{s2} = V_{\max}\sin(\omega t - \frac{2\pi}{3}) \\ v_{s3} = V_{\max}\sin(\omega t + \frac{2\pi}{3}) \end{cases} \tag{6}$$

After the transformation of Eq. (6) in the stationary reference frame ($\alpha\beta$ axes), one obtains:

$$\begin{cases} v_{s\alpha} = \sqrt{\frac{2}{3}}.V_{\max}\left[\sin(\omega t) - \frac{1}{2}\sin\left(\omega t - \frac{2\pi}{3}\right) - \frac{1}{2}\sin(\omega t + \frac{2\pi}{3})\right] \\ v_{s\beta} = \sqrt{\frac{2}{3}}.V_{\max}\left[\frac{\sqrt{3}}{2}\sin\left(\omega t - \frac{2\pi}{3}\right) - \frac{\sqrt{3}}{2}\sin\left(\omega t + \frac{2\pi}{3}\right)\right] \end{cases} \tag{7}$$

The simplification of Eq. (7) gives:

$$\begin{cases} v_{s\alpha} = 3\sqrt{\frac{2}{3}}.V_{\max}\sin(\omega t) \\ v_{s\beta} = -3\sqrt{\frac{2}{3}}.V_{\max}\cos(\omega t) \end{cases} \tag{8}$$

And in the synchronous reference frame (dq frame):

$$\begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \end{bmatrix} \tag{9}$$

With θ the position angular of three-phase source voltages. One obtains:

$$v_{sd} = 3\sqrt{\frac{3}{2}}.V_{\max}\left[\sin(\omega t)\cos(\theta) - \cos(\omega t)\sin(\theta)\right] \tag{10}$$

$$v_{sd} = 3\sqrt{\frac{3}{2}}.V_{\max}\sin(\omega t - \theta) \tag{11}$$

By supposing that$(\omega t - \theta)$ is very small, then the preceding expression can be expressed by:

$$v_{sd} = 3\sqrt{\frac{3}{2}}V_{\max}(\omega t - \theta) \tag{12}$$

The estimated angular pulsation at the output linear PI controller is given by:

$$\widehat{\omega} = H.3\sqrt{\frac{3}{2}}V_{\max}(\omega t - \theta) \tag{13}$$

$H(s)$ is the transfer function of linear PI controller, defined by:

$$H(s) = k_p + \frac{k_i}{s} \tag{14}$$

The position angular is given by:

$$\theta = \frac{\widehat{\omega}}{s} \tag{15}$$

The replacement of the relations (15) and (14) in (13) is given by:

$$\theta s = \left(k_p + \frac{k_i}{s}\right).3\sqrt{\frac{3}{2}}.V_{\max}(\omega t - \theta) \tag{16}$$

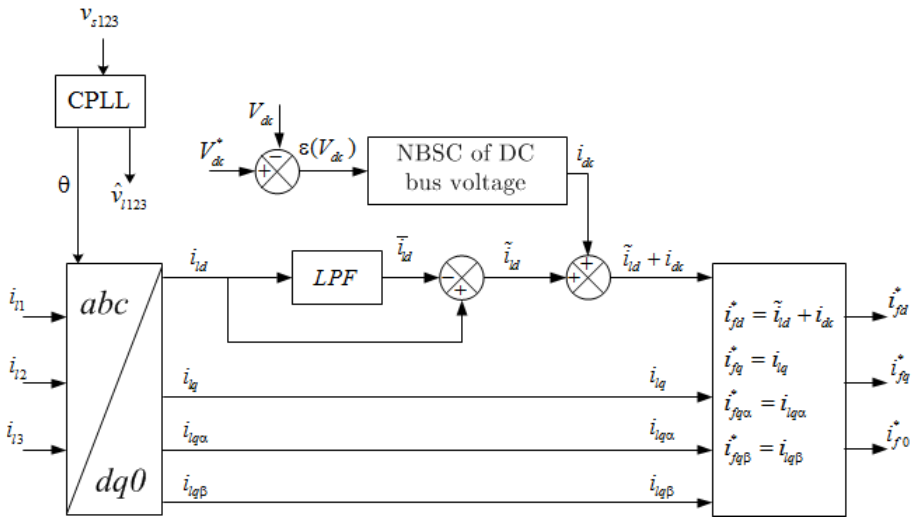

Figure 4: Block diagram of SRF theory using CPLL based four leg SAPF.

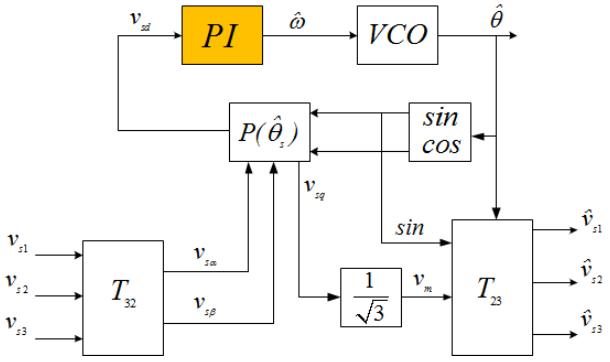

Figure 5: Block diagram of CPLL based on linear PI controller

From which one finds the transfer function of the system:

$$\frac{\theta}{\omega t} = \frac{\left(k_p s + k_i\right).3\sqrt{\frac{3}{2}}.V_{\max}}{s^2 + \left(k_p s + k_i\right).3\sqrt{\frac{3}{2}}.V_{\max}} \tag{17}$$

The gains k_p and k_i, are given by:

$$\begin{cases} k_i = \sqrt{\frac{2}{3}}\frac{(2\pi f_c)^2}{3V_{\max}} \\ k_p = \sqrt{\frac{2}{3}}\frac{4\pi f_c \xi}{3V_{\max}} \end{cases} \tag{18}$$

4. Enhanced phase locked loop based STF and PI controller (EPLL$_{\text{STF-PI}}$)

The block diagram of enhanced phase locked loop based STF and PI controller (EPLL$_{\text{STF-PI}}$) is shown in Fig. 6.

The Self Tuning Filter is a feedback nonlinear controlled circuit used to extract the fundamental components of any periodical signal [18, 25, 28]. This controlled circuit is shown in Fig. 7.

The Self Tuning Filter can be presented by the following transfer function:

$$G(s) = \frac{V_{xy}(s)}{U_{xy}(s)} = k_e \frac{(s+k) + j\omega_c}{(s+k)^2 + \omega_c^2} \tag{19}$$

In the stationary reference frame, the expressions of the continue components are given by:

$$\begin{cases} \bar{X}_\alpha(s) = \frac{k}{s}\left[X_\alpha(s) - \bar{X}_\alpha(s)\right] - \frac{\omega}{s}\bar{X}_\beta(s) \\ \bar{X}_\beta(s) = \frac{k}{s}\left[X_\beta(s) - \bar{X}_\beta(s)\right] + \frac{\omega}{s}\bar{X}_\alpha(s) \end{cases} \tag{20}$$

5. Performance analyses of the two PLL

The various performances of the two PLL under unbalanced three phase source voltages are presented in this section. For testing of the performance of the two PLL under unbalanced source voltages, the three phase unbalanced source voltages values are given as follows:

$$\begin{cases} v_{s1} = 220\sqrt{2}\sin(\omega t) \\ v_{s2} = 220\sin(\omega t - \frac{2\pi}{3}) \\ v_{s3} = 220\sqrt{2}\sin(\omega t + \frac{2\pi}{3}) \end{cases} \tag{21}$$

5.1. The performances of CPLL

Figs 8 illustrate the simulation results of the CPLL for unbalanced source voltages due to a decrease in amplitude of the second phase. The estimate position angular Titha oscillates with a pulsation of $(2w)$ about its reference, which generates deformations of the two signals sine, cosine and estimate source voltages in the outputs of PLL.

5.2. The performances of EPLL$_{STF}$

The EPLL$_{\text{STF}}$ is carried out on unbalanced source voltages due to a decrease in amplitude of phase 2. In contrast to the results found with the CPLL, the estimate position angular

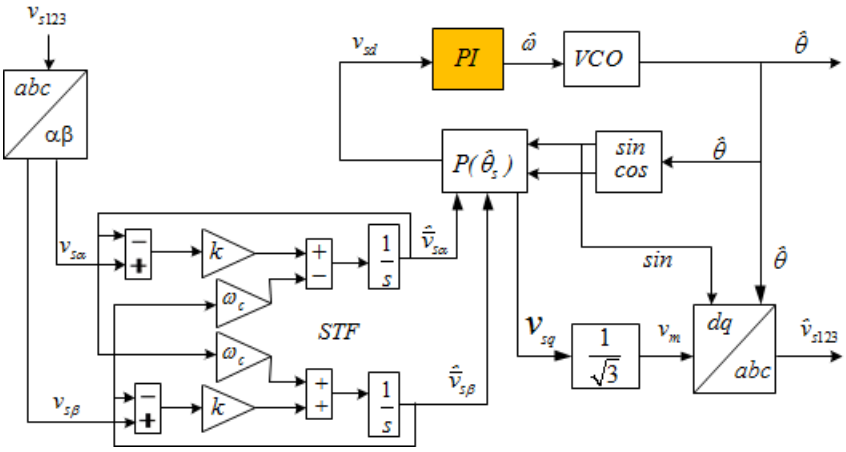

Figure 6: Block diagram of EPLL based on STF and linear PI controller or PLL$_{STF-PI}$

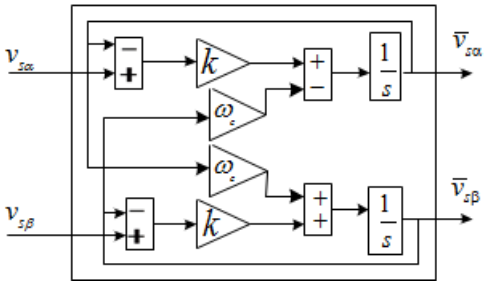

Figure 7: A Self Tuning Filter

Titha is non oscillating and periodically linear. The sin/cos waves are well filtered, and we obtain the balanced estimate source voltages and very good qualities at the outputs of EPLL$_{STF}$.

Figs 8 and 9 show that the EPLL$_{STF}$ can perform quickly for estimate position angular, sin/cos waves, and balanced estimate source voltages.

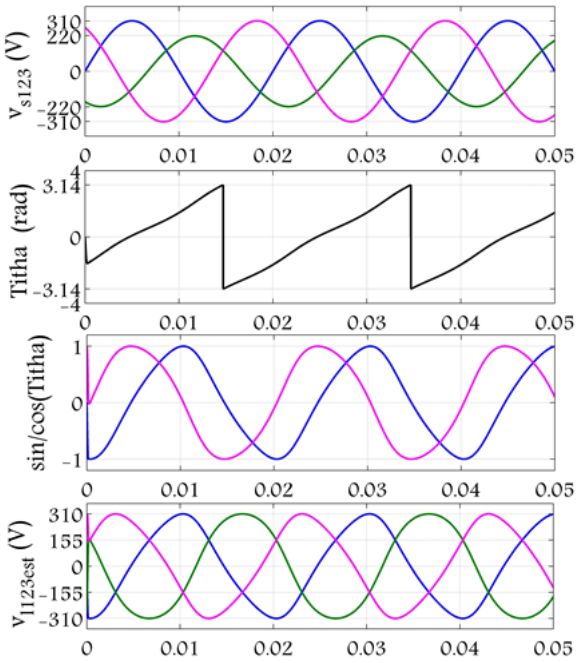

Figure 8: Performances of CPLL under unbalanced source voltages

6. Enhanced PLL based STF and FLC controller

In light of the VCO parametric uncertainties, using linear PI is not appropriate. Applying linear PI controller to this issue is non robust and results in worse EPLL performances. These problems may lead to poor performances in unbalanced source voltages and loads. FLC is intelligent control, and is an attractive regulation and control technique in several applications due to its partial association crisp membership functions nature, parallel calculating, high precision, and high robustness [27, 29, 30]. Many FLC structures based on the number of membership functions used have been proposed for control of the SAPF, such as FLC based on three membership functions and FLC based on five membership functions. Among these structures, the most frequently used FLC for control of SAPF has been the FLC based on the three membership functions structure. In this work we replaced the linear PI used in EPLL with an FLC based on the three membership functions structure for control of the active source voltages component v_{sd} to zero. The block diagram of the proposed EPLL based on STF and FLC is shown in Fig. 10 and the FLC used in this EPLL is shown in Fig 11.

The FLC contained three components: fuzzification, knowledge base and defuzzification. To fuzzify the variation of active source voltages component control, two fuzzy inputs are used. The first input is defined as the error of active source voltages component $\varepsilon(v_{sd})$ and the second fuzzy input is defined as the derivative of this error$\Delta\varepsilon(v_{sd})$. In the fuzzification of input and output variables, we used three membership functions selected from the same fuzzy sets in all variables: (N, Z, P), where N defined “Negative”, Z defined “Zero”, and

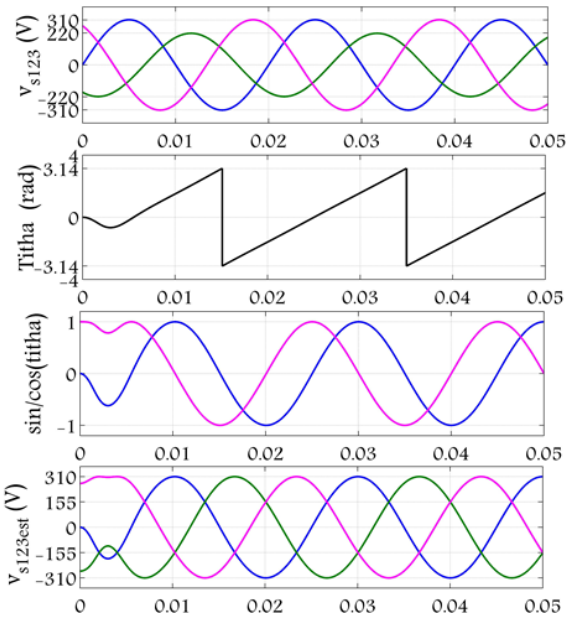

Figure 9: Simulation results of the EPLL$_{STF}$ unbalanced source voltages

Table 1: FUZZY CONTROL RULE TABLE OF THE ACTIVE SOURCE VOLTAGES COMPONENT CONTROLLER

		$\Delta\varepsilon(v_{sd})$		
		N	Z	P
$\varepsilon(v_{sd})$	N	N	N	Z
	Z	N	Z	P
	P	Z	P	P

P is “Positive”.

The output of FLC represents the estimated angular pulsation$\hat{\omega}$. The membership functions of the input and output variables are shown in Fig. 11. The knowledge base, or fuzzy rule bases with 9 rules, is given in Table 1.

Fig. 12 shows the dynamic performance of active source voltages component v_{sd} obtained in the three cases of PLL. By examining the obtained components, it is clear that there is a divergence between the component (v_{sd}) controlled by linear PI and FLC. The response time for control active source voltages component to zero in the FLC is lower and better than the PI. The undulations of the active source voltages component obtained by FLC are around zero and very small compared to those obtained by PI. This last aspect impacts the VOC operations and leads to worse EPLL performances.

7. Simulation results and discussion

A simulation model as shown in Fig. 13 was developed using Sim Power Systems and S-Function of MATLAB to verify and confirm the viability and effectiveness of the proposed Enhanced PLL based STF and FLC associated with SRF theory for good reference harmonic currents identification of 4LSAPF under unbalanced source voltages and load conditions in order to eliminate a wide range of current harmonics and compensate the reactive power generated by nonlinear loads in four wire electrical networks. The objectives of these simulations are the study of two different aspects: a) the performances of SRF theory using EPLL$_{STF\text{-}FLC}$ of reference current harmonics identification of 4LSAPF compared to SRF theory based on EPLL$_{STF\text{-}FLC}$ and SRF theory based on CPLL$_{PI}$ used in the work [15] through extensive simulation under balanced source voltages and unbalanced loads; b) the effects of SRF theory based on EPLL$_{STF\text{-}FLC}$ for the identification and stabilization of reference current harmonics under unbalanced source voltages and loads. The values of system and simulation parameters are presented in Tables 3 and 4.

7.1. Simulation results before compensation

Fig. 14 (a, b and c) shows: a) waveform of source currents (i_{s123}); b) first phase source current and corresponding voltage; and c) neutral wire source current (i_{sn}) before compensation. It can be observed from Fig. 14 (a) that the waveform of source currents are highly non sinusoidal, very deformed and not in sync with the corresponding voltage (the power factor is not unitary). Fig. 14 (b) shows the neutral wire source current is at a maximum value of 22A before unbalanced loads and 70A after unbalanced loads, see Fig. 14 (c).

Fig. 15 (a and b) shows the harmonics analysis of first phase source currents before and after unbalanced load at $t = 0.4$ s, the total harmonic distortion (THD) before unbalanced load is 13.92% and after unbalanced load is 10.51%.

7.2. Performance of 4LSAPF based on SRF theory with EPLL$_{STF-FLC}$ with balanced source voltage and unbalanced loads

We present in these simulations the three strategies for reference current harmonics identification (SRF-EPLL$_{STF\text{-}FLC}$, SRF-EPLL$_{STF\text{-}PI}$, and SRF-CPLL$_{PI}$ used in [15]) using Nonlinear Back Stepping Controllers (NBSC) for SAPF injected currents and the dc-link voltage capacitor regulation and the Three Dimensional Space Vector Modulation (3DSVM) for switching signals determination with balanced source voltages and unbalanced loads. Each figure is divided into six groups: a) waveform of source currents (i_{s123}); b) waveform of load currents (i_{l123}); c) waveform of SAPF injected currents (i_{f123}) and harmonic references ($i_{f123ref}$); d) first phase source current and corresponding voltage; e) neutral wire source current (i_{sn}); and f) source active and reactive power (p_s and q_s).

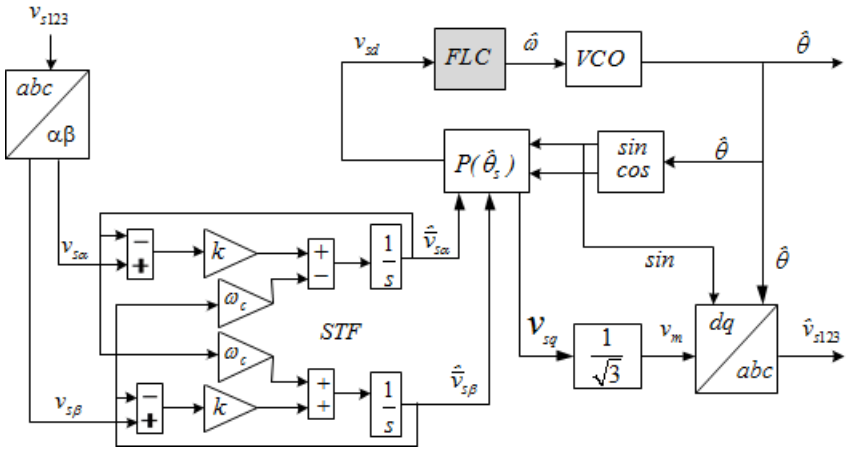

Figure 10: Block diagram of enhanced PLL based on STF and FLC controller or PLL$_{STF-FLC}$

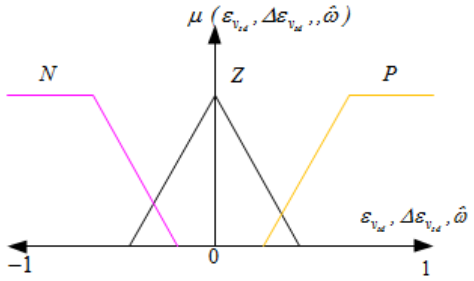

Figure 11: Membership functions for the input and output variables of active source voltages component

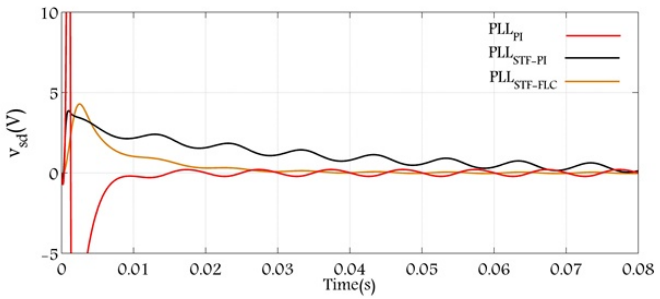

Figure 12: The dynamic performance of active source voltages component using the three PLL

In the three cases of reference current harmonics identification before and after unbalanced loads at $t = 0.4$s, the 4LSAPF operates correctly to eliminate the harmonic currents and zero sequence current, and to compensate the reactive power. It can be observed from Figs 16, 17 and 18 (a and d) that the waveforms of source currents are sinusoidal with a unity power factor operation in the three strategies SRF-EPLL$_{\text{STF-FLC}}$, SRF-EPLL$_{\text{STF-PI}}$, and SRF-CPLL$_{PI}$; the waveforms of SAPF injected currents have tracked their reference current harmonics with zero error in the three strategies: Figs 16, 17 and 18 (c), the neutral wire source current is reduced in the three strategies; there are fewer oscillations in the cases of SRF- EPLL$_{\text{STF-PI}}$ and SRF- EPLL$_{\text{STF-FLC}}$ than the SRF- CPLL$_{\text{PI}}$ application before and after unbalanced loads Figs 17 and 18 (e). It can also be observed from Figs 17 and 18 (f) that the source reactive power oscillated around zero before and after unbalanced loads, as well as small magnitudes in the case of SRF-EPLL$_{\text{STF-FLC}}$ (0.4 kvar). In the case of balanced source voltage, the THDs of the source currents are less than 5% before and after unbalanced loads, which meets the regulations of the IEEE 519 standard, as well as smaller values in the case of four leg SAPF controlled by the proposed SRF-EPLL$_{\text{STF-FLC}}$ in Figs 19, 20 and 21 (a and b). This verifies the robustness and the effectiveness of SRF-EPLL$_{\text{STF-FLC}}$ for controlling the 4LSAPF in terms of good reference harmonic currents identification, source currents ripple, magnitude of neutral wire current, and achieving reactive power compensation with balanced source voltages and unbalanced loads in the four wire electrical networks.

7.3. Performance of 4LSAPF based on SRF theory with EPLL$_{\text{STF-FLC}}$with unbalanced source voltage and loads

For testing the performance of the three PLL with unbalanced source voltages and loads, the three phase unbalanced source voltage values are given as follows:

$$\begin{cases} v_{s1} = 220\sqrt{2}\sin(\omega t) \\ v_{s2} = 220\sin(\omega t - \frac{2\pi}{3}) \\ v_{s3} = 220\sqrt{2}\sin(\omega t + \frac{2\pi}{3}) \end{cases} \quad (22)$$

The 4LSAPF configuration is tested before and after unbalanced loads at $t = 0.4$ s with unbalanced source voltages and the simulation results are presented in the following sub sections.

Figs 22 to 30shows the performances of 4LSAPF controlled by the three strategies for reference current harmonics identification (SRF-EPLL$_{\text{STF-FLC}}$, SRF-EPLL$_{\text{STF-PI}}$, and SRF-CPLL$_{\text{PI}}$ used in [15]) with unbalanced source voltages and loads.

Fig. 22 (a) and (b) shows the waveforms of unbalanced source voltages and estimate source voltages with SRF-CPLL$_{PI}$ respectively. The waveform of source currents and

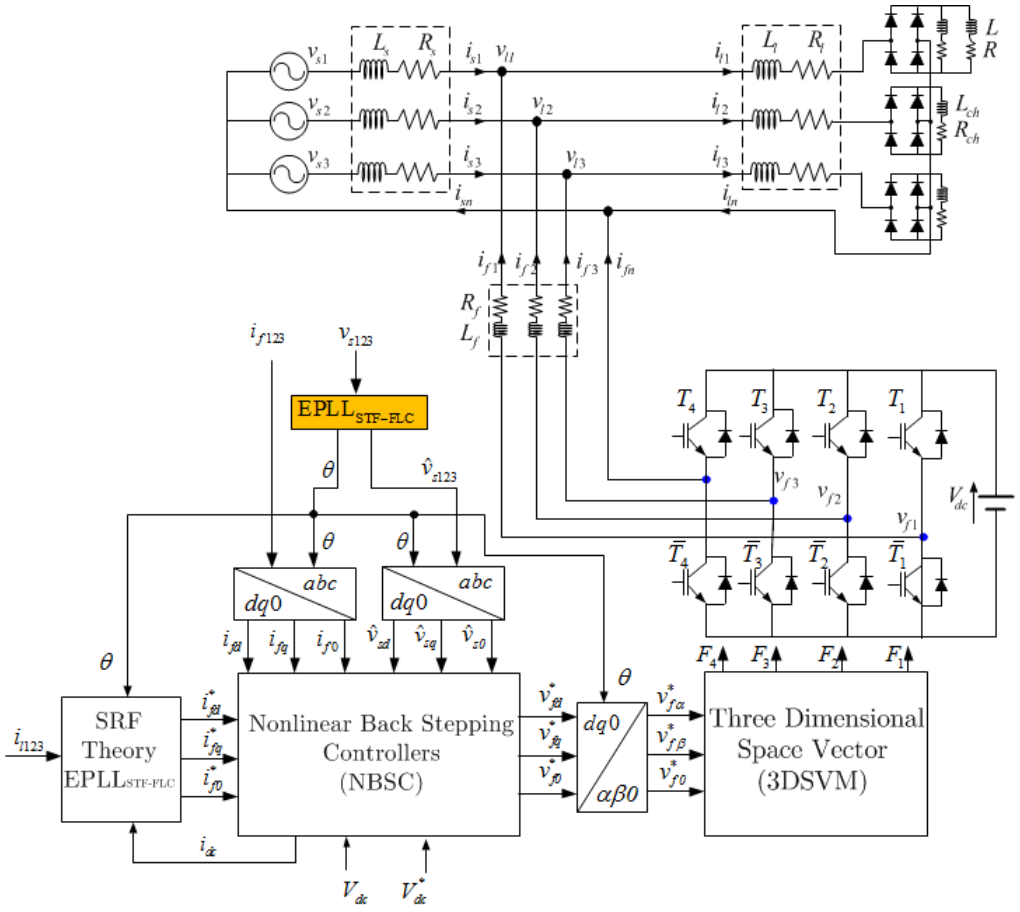

Figure 13: Schematic diagram of 4L SAPF controlled by proposed SRF theory based on $EPLL_{STF-FLC}$ using 3DSVM and Nonlinear Back Stepping Controllers (NBSC).

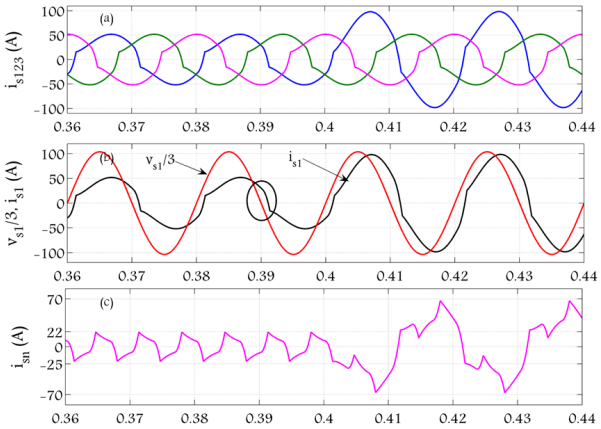

Figure 14: Simulation results before compensation of four wire electrical network

the first phase source current, and the corresponding voltage are shown in Fig. 22 (c) and (d) respectively. It is observed that due to the unbalance of source voltages, the estimate source voltages and currents are not sinusoidal and the source currents not compensated satisfactorily by the 4LSAPF, and the power factor is not unitary Fig. 22 (d).

In the two cases of reference current harmonics identification (SRF-EPLL$_{\text{STF-FLC}}$ and SRF-EPLL$_{\text{STF-PI}}$) before and after unbalanced loads at $t = 0.4$s with unbalanced source voltages, the 4LSAPF operates correctly to eliminate the harmonic currents and zero sequence current, and to compensate the reactive power. It can be observed from Figs 23 and 24 (b, c and d) that the waveforms of estimate source voltages and currents are sinusoidal with a unity power factor operation in the two strategies SRF- EPLL$_{\text{STF-FLC}}$ and SRF-EPLL$_{\text{STF-PI}}$, the SAPF injected currents tracked their harmonic references with zero error in the two strategies, see Figs 23 and 24 (f).

Figs 25 to 30 (a, b and c) shows the harmonics analysis of source currents with unbalanced source voltages before and after unbalanced loads. In the case of four leg SAPF controlled by SRF-CPLL$_{\text{PI}}$, the THDs of source currents are more than 5% before and after unbalanced loads, see Figs 25 and 26 (a, b and c) which present the poor power factor. These THDs are further reduced in the two cases of four leg SAPF controlled by SRF-EPLL$_{\text{STF-PI}}$ and SRF-EPLL$_{\text{STF-FLC}}$, see Figs 27 to 30 (a, b and c), and are less than 5% before and after unbalanced loads, which meets the regulations as per the IEEE 519 standard. There are very small values in the case of four leg SAPF controlled by proposed SRF-EPLL$_{\text{STF-FLC}}$, see Figs29 and 30 (a, b and c), which confirm the effectiveness of the proposed EPLL$_{\text{STF-FLC}}$ associated with SRF theory for controlling the four leg SAPF in terms of good reference harmonic currents identification, source current harmonics reduction, and source reactive power compensation with maximum power factor in four wire electrical networks under unbalanced source voltages and loads. The results achieved with all methods for different test cases of source voltages and loads are tabulated in Table 2.

8. Conclusion

In this paper, an effective Enhanced Phase Locked Loop based on self tuning filter (STF) and fuzzy logic control associated with SRF theory has been proposed for a four leg SAPF to eliminate a wide range of current harmonics and compensate the source reactive power generated by nonlinear loads in order to achieve the maximum power factor in four wire electrical networks under unbalanced source voltages and loads. The use of Enhanced Phase Locked Loop based on self tuning filter (STF) and fuzzy logic control associated with SRF theory delivers satisfactory performance for a four leg SAPF, which has been validated by various simulation results. The robustness analysis of the proposed SRF-EPLL$_{\text{STF-FLC}}$ strategy, tested with different source voltages and load conditions and compared with the two strategies SRF-CPLL$_{\text{PI}}$ and SRF-EPLL$_{\text{STF-PI}}$, demonstrates that it is effective and always converges to a very good solution as regards power quality problems in the case of source voltages and load conditions. Furthermore, it provides good estimates of the fundamental components of source voltages under unbalanced source voltage conditions. For four leg SAPF injected current regulations, the use of NBC has given very good performances in terms of references tracking for SAPF injected currents under unbalanced loads, very much lower harmonics and switching ripple in source currents, and source reactive power compensation. The simulation results have demonstrated the superiority and major advantages of the proposed strategies.

Appendix

Table 3: SYSTEM AND SIMULATION PARAMETERS

Parameter	Value
Source voltage and frequency	220 V, 50 Hz
Capacitance of the capacitor C_{dc}	$5 \cdot 10^{-3}$F
Dc link voltage	800V
Source impedance R_s , L_s	1 mΩ, 1 mH
Line impedance R_l, L_l	1 mΩ, 1 mH
Coupling filter R_f, L_f	0.1 mΩ, 0.1 mH
Loads impedance R_{ch}, L_{ch}	5 Ω, 10 mH
Unbalanced load R , L	5 Ω, 10 mH
Sampling time	10^{-6}s
Switching frequency fs	14000Hz

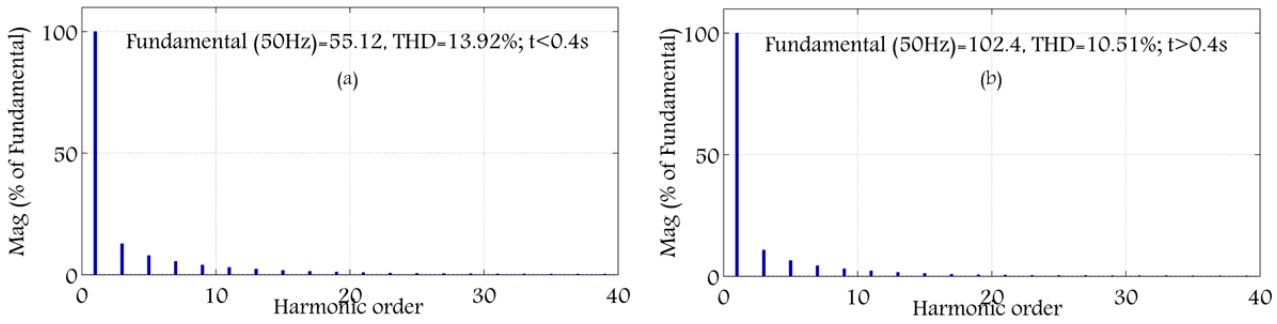

Figure 15: Harmonics analysis of first phase source currents before compensation: (a) Before unbalanced loads, (b) After unbalanced loads

Table 4: REGULATORS AND STF PARAMETERS

PI	NBC	STF
$f_c = 10$ kHz, $\xi = 0.7$	$k_1 = k_2 = k_3 = 8e^6$	$k = 70$, $\omega_c = 220$
$f_{ds} = 4$ Hz	$k_{Vdc} = 100$.	

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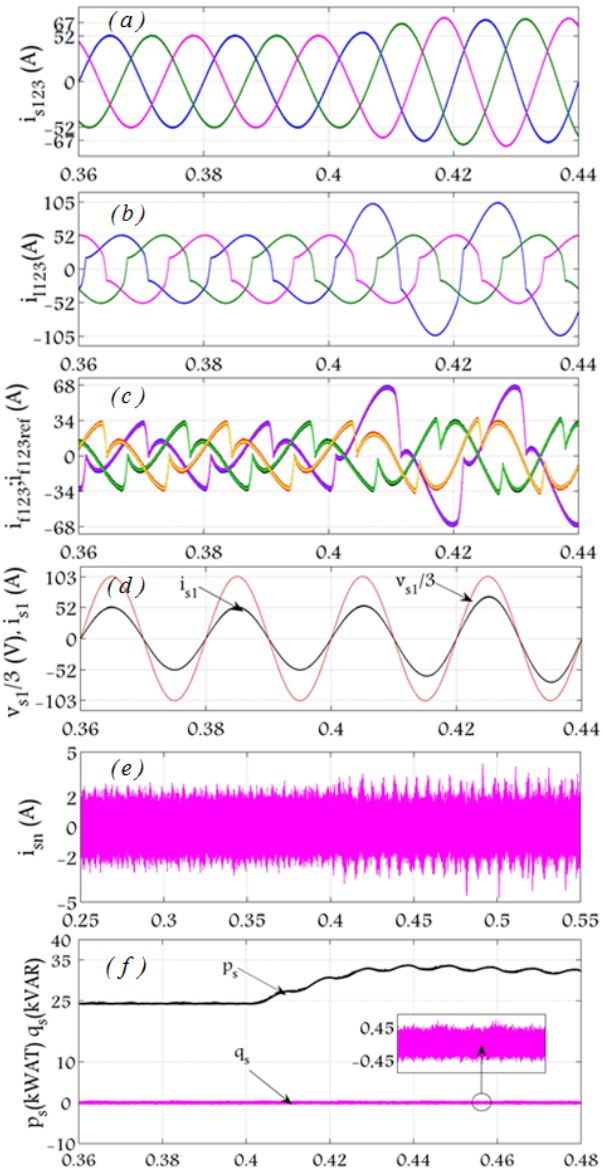

Figure 16: Performance of four leg SAPF controlled by SRF-CPLL$_{PI}$ with balanced source voltages and unbalanced loads.

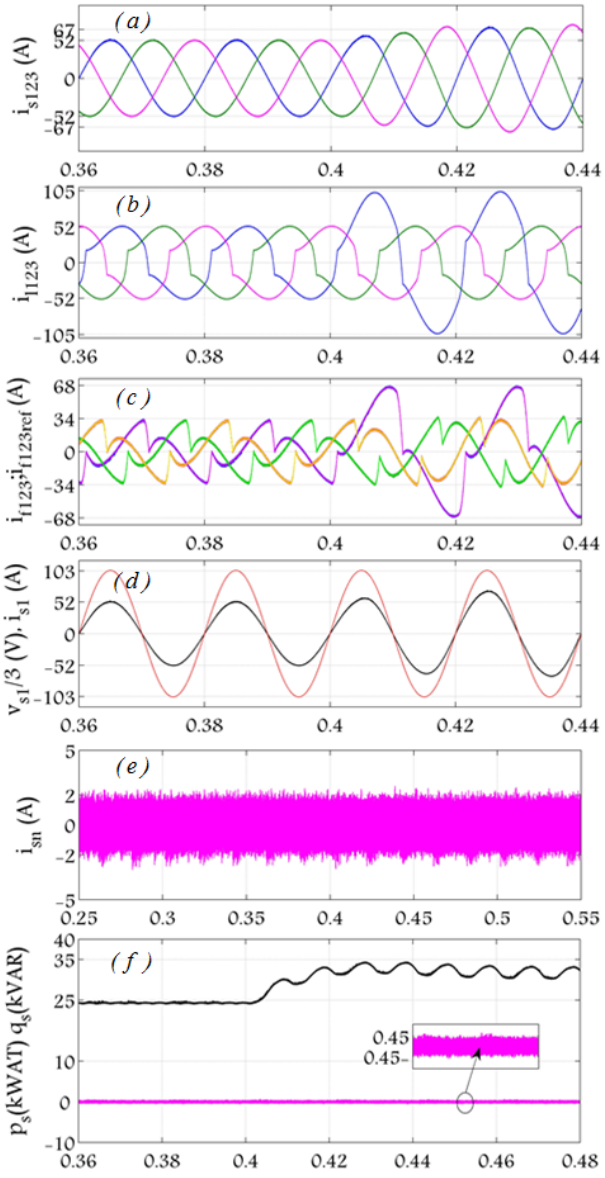

Figure 17: Performance of four leg SAPF controlled by SRF-EPLL$_{\text{STF-PI}}$ with balanced source voltages and unbalanced loads

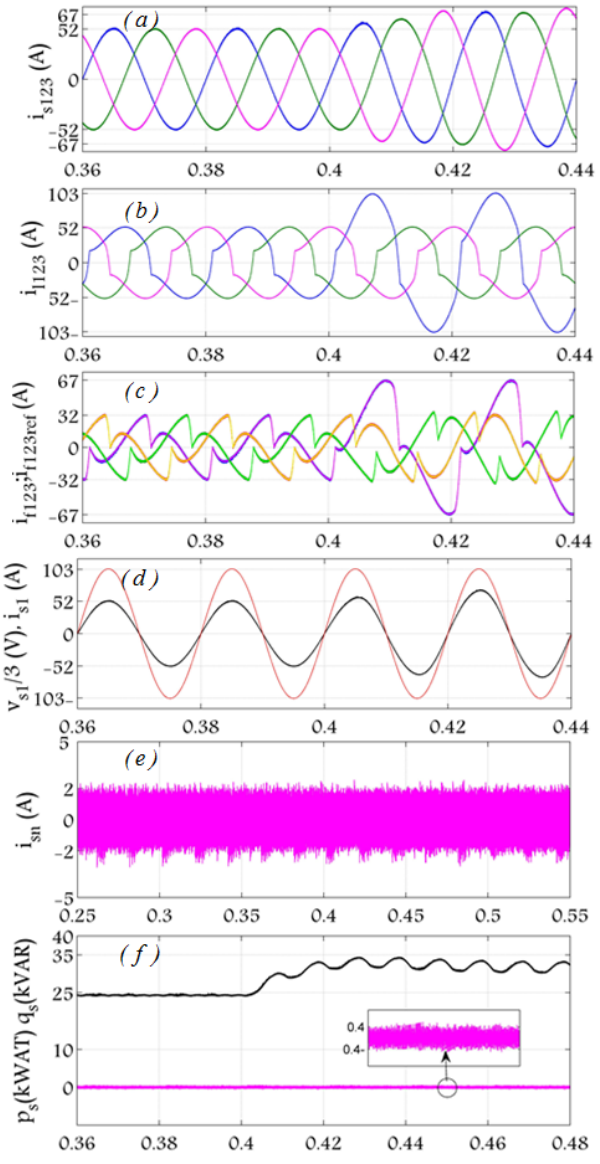

Figure 18: Performance of four leg SAPF controlled by SRF-EPLL$_{\text{STF-PI}}$ with balanced source voltages and unbalanced loads

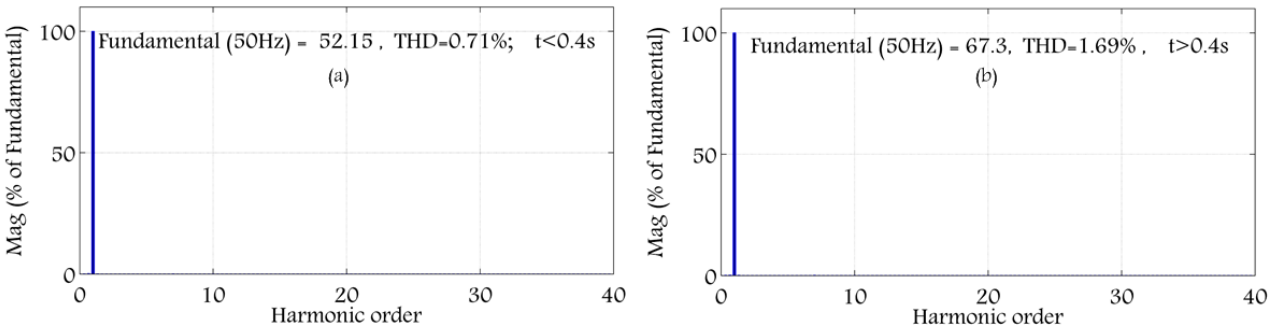

Figure 19: Harmonics analysis of source current with a four leg SAPF controlled by SRF-CPLL$_{PI}$ with balanced source voltages: (a) Before unbalanced loads, (b) After unbalanced loads

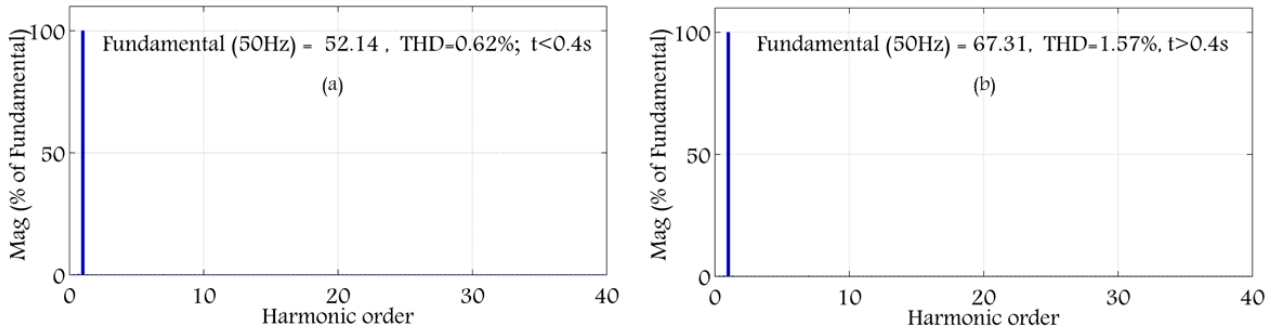

Figure 20: Harmonics analysis of source current with a four leg SAPF controlled by SRF-EPLL$_{STF\text{-}PI}$ with balanced source voltages: (a) Before unbalanced loads, (b) After unbalanced loads

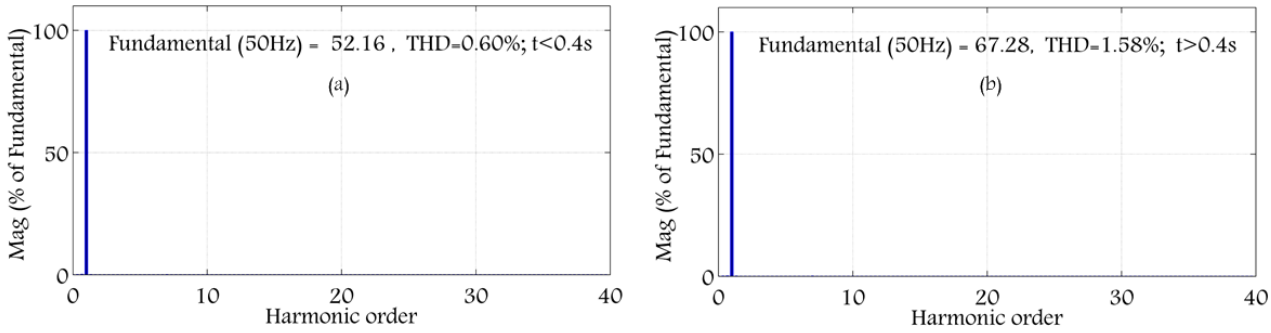

Figure 21: Harmonics analysis of source current with a four leg SAPF controlled by SRF-EPLL$_{FLC\text{-}PI}$ with balanced source voltages: (a) Before unbalanced loads, (b) After unbalanced loads

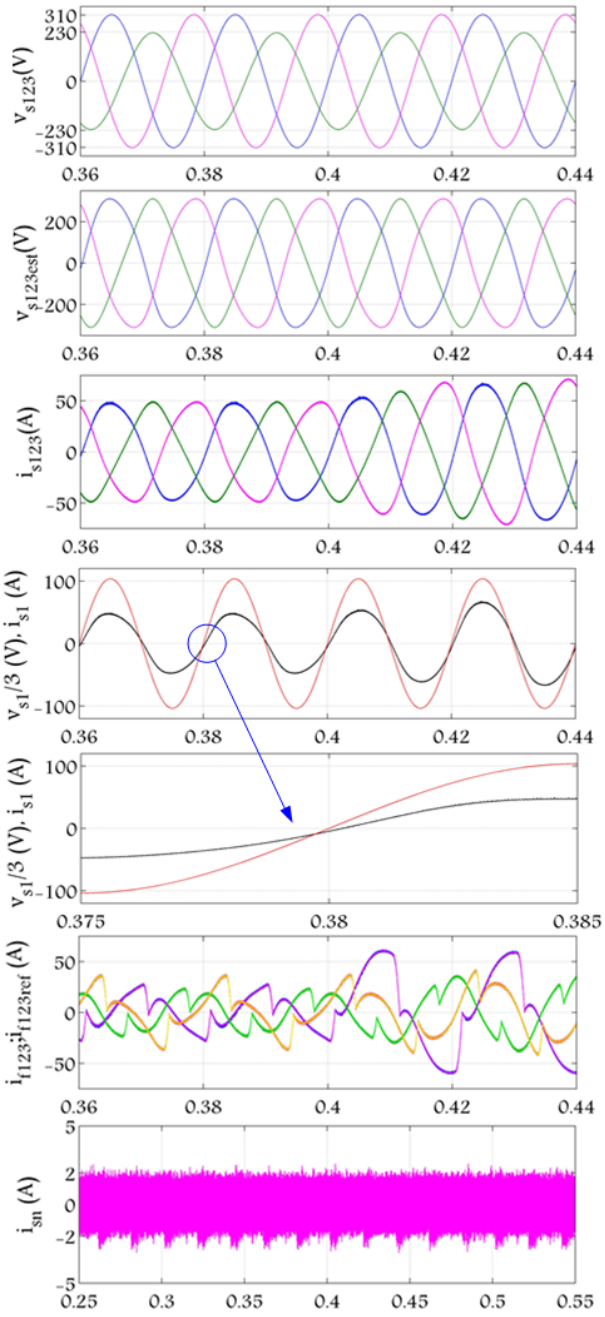

Figure 22: Performance of four leg SAPF controlled by SRF-CPLL$_{\text{-PI}}$ with unbalanced source voltages and loads

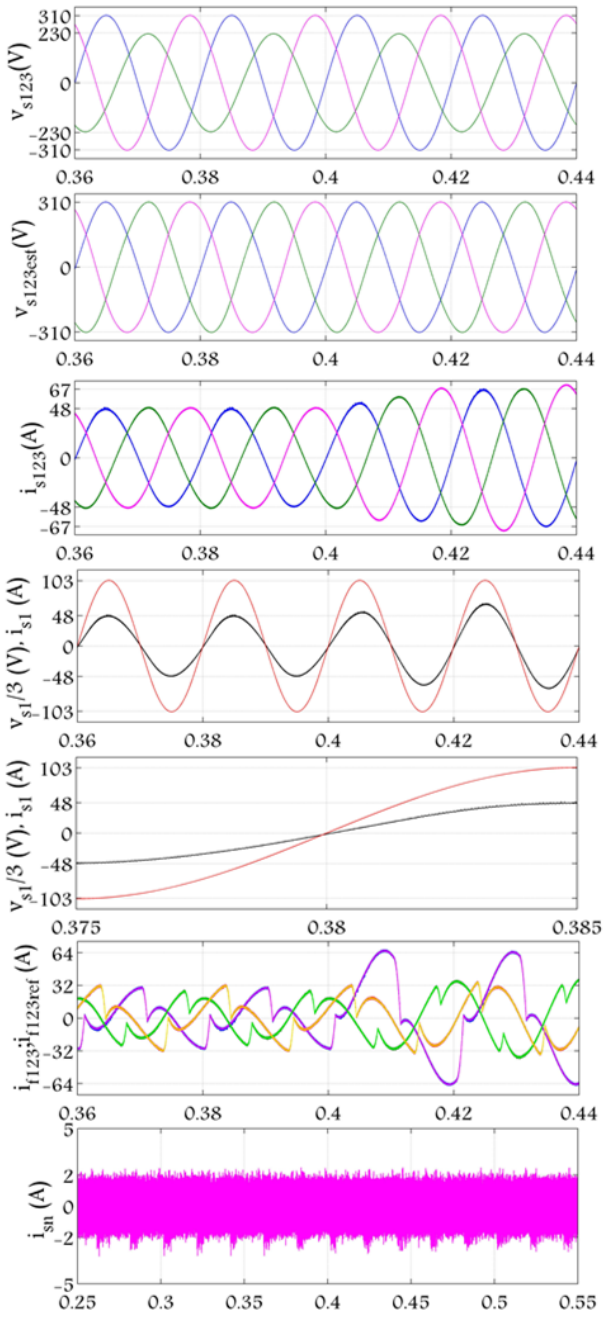

Figure 23: Performance of four leg SAPF controlled by SRF-EPLL$_{\text{STF-PI}}$ with unbalanced source voltages and loads

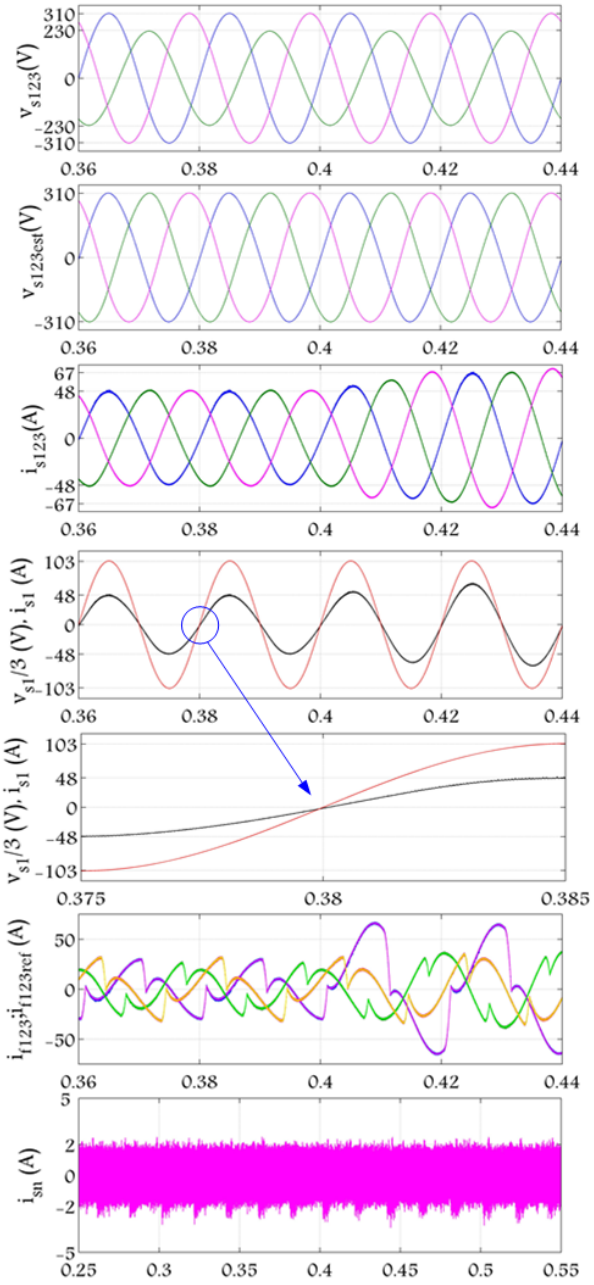

Figure 24: Performance of four leg SAPF controlled by SRF-EPLL$_{STF-FLC}$ with unbalanced source voltages and loads

Table 2: Comparisons of different methods for all simulation tests in this work

Source voltages	Source currents	Phases	Source current harmonic (% of fundamental)							
			Before compensation	After compensation						
				CPLLPI		EPLLSTF-PI		EPLLSTF-FLC		
			t<0.4s	t>0.4s	t<0.4s	t>0.4s	t<0.4s	t>0.4s	t<0.4s	t>0.4s
Balanced source voltages	THD%	Ph-1	13.92	10.51	2.23	2.35	2.79	2.82	2.79	2.82
		Ph-2	13.92	13.92	2.24	2.37	2.77	2.79	2.77	2.79
		Ph-3	13.92	13.92	2.24	2.35	2.80	2.83	2.80	2.83
Unbalanced source voltages	THD%	Ph-1	13.92	10.51	7.75	8.83	2.55	2.82	2.48	2.73
		Ph-2	13.89	13.89	8.08	9.10	2.43	2.85	2.38	2.74
		Ph-3	13.92	13.92	8.42	9.16	2.52	2.88	2.41	2.69

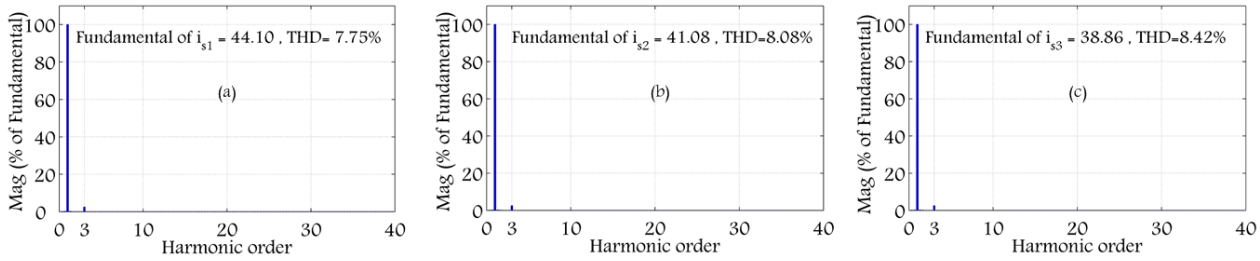

Figure 25: Harmonics analysis of three phase source currents with a four leg SAPF controlled by SRF-CPLL$_{PI}$ with unbalanced source voltages before unbalanced loads

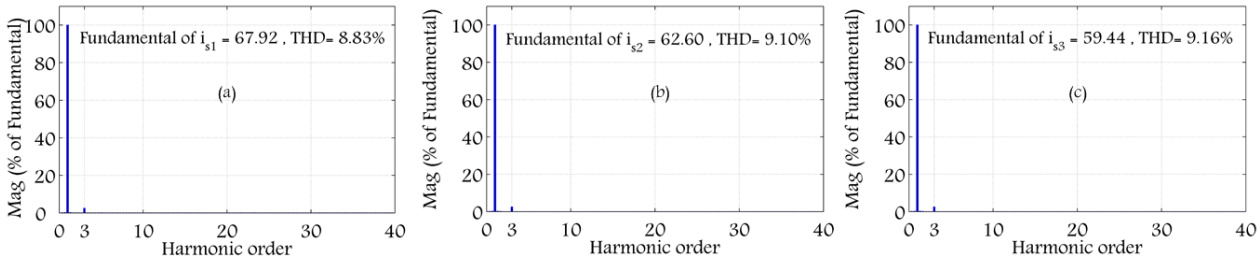

Figure 26: Harmonics analysis of three phase source currents with a four leg SAPF controlled by SRF-CPLL$_{PI}$ with unbalanced source voltages after unbalanced loads

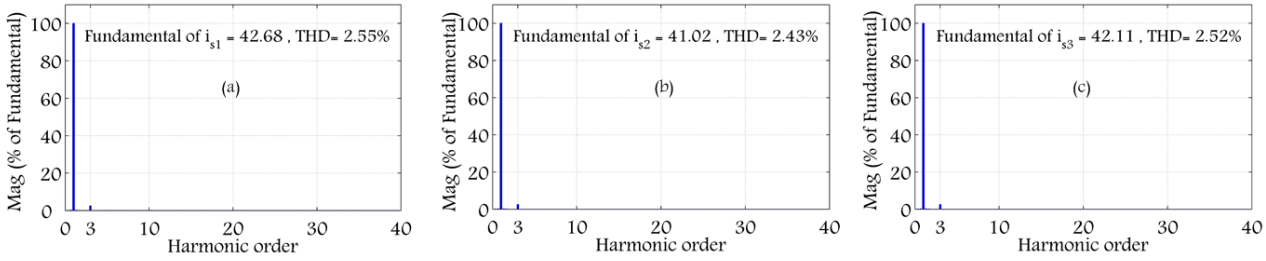

Figure 27: Harmonics analysis of three phase source currents with a four leg SAPF controlled by SRF-EPLL$_{STF-PI}$ with unbalanced source voltages before unbalanced loads

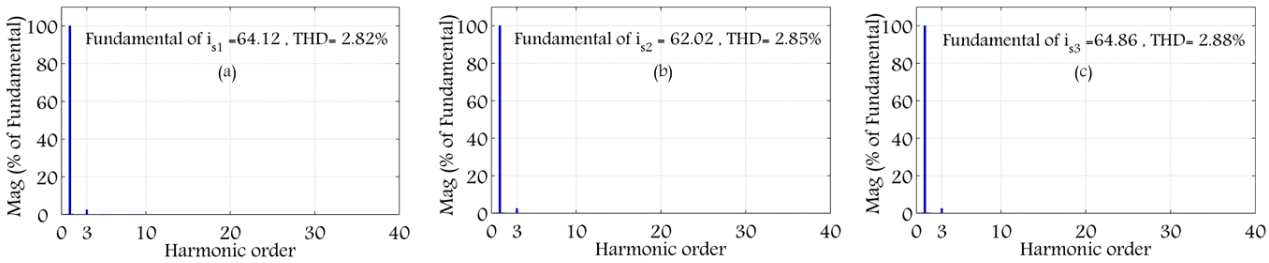

Figure 28: Harmonics analysis of three phase source currents with a four leg SAPF controlled by SRF-EPLL$_{STF-FLC}$ with unbalanced source voltages after unbalanced loads

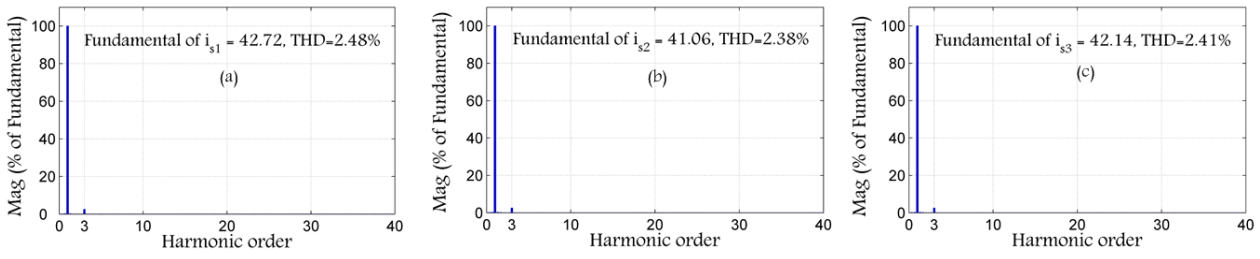

Figure 29: Harmonics analysis of three phase source currents with a four leg SAPF controlled by SRF-EPLL$_{STF-FLC}$ with unbalanced source voltages before unbalanced loads

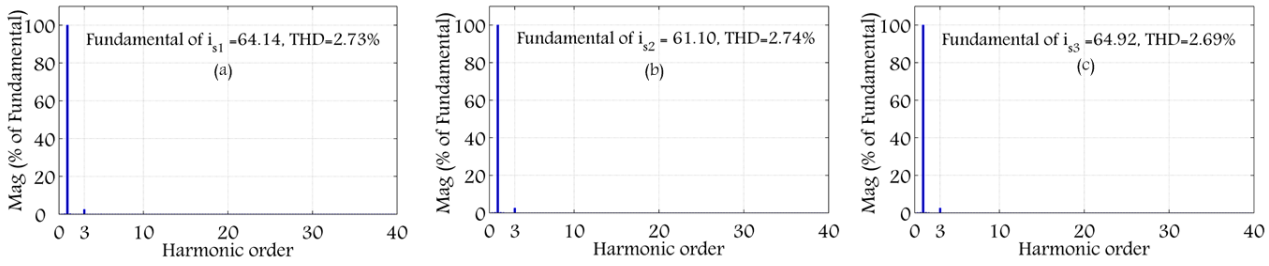

Figure 30: Harmonics analysis of three phase source currents with a four leg SAPF controlled by SRF-EPLL$_{\text{STF-FLC}}$ with unbalanced source voltages after unbalanced loads