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ORIGINAL ARTICLE

Backstepping control of a grid-connected four-leg PWM rectifier under both balanced and unbalanced grid conditions

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Abstract This study focuses on a backstepping control (BSC) of a three-phase four-leg pulse width modulation (PWM) rectifier under balanced and unbalanced load and grid conditions. The proposed BSC for the three-phase four-leg PWM rectifier (3P-4LR) connected to the grid is build up using three independent backstepping controllers based on Lyabonov theory to control simultaneously DC voltage and input currents. As a result, unit power factor, stable DC-bus voltage, sinusoidal input 3P-4LR currents with a lower harmonic content and lower zero-sequence and natural currents can be accurately achieved. Not only that, robustness against voltage grid fluctuations, load and filter inductance variations can also be carried out. The effectiveness, superiority, good dynamic, and steady-state performances of the proposed BSC based 3P-4LR have been validated by numerical simulations compared to the conventional proportional-integral control under balanced and unbalanced load and grid conditions.

Keywords Grid-connected four-leg PWM rectifier · Backstepping control (BSC) · Lyabonov theory · Power quality · Zero-sequence current (ZSC) · Unbalanced conditions

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1 Introduction

Three-phase three-leg PWM rectifiers have been widely studied and used in many power applications, such as grid power factor correction (Bu et al. 2017; Lu et al. 2018), wind energy system based on doubly fed induction generator (DFIG) feeding stand-alone loads (Mazouz et al. 2020), electric vehicle (EV) as charging system (Song et al. 2020), and high-voltage-direct-current (HVDC) systems (Rabie et al. 2021). It is deemed as high-efficiency device for high-power applications due to its superior input current quality waveforms as well as lower input current total harmonic distortion, unit power factor (UPF), controllable DC-bus voltage, and bidirectional power flow. However, for many power applications, the classical three-leg PWM rectifier (3P-3LR) may not be a perfect option due to the unbalanced single phase nonlinear loads connected to the main grid or non-symmetrical grid impedance (Zhang et al. 2000; Kaszewski et al. 2014). In addition, if the 3P-3LR is connected to an unbalanced grid voltage, an uncontrolled second-order harmonic appears as an oscillation on the DC-bus voltage. This effect the capacitor to be further charged than its desired voltage, which leads to further damage to the 3P-3LR power switches, and augments the total harmonic distortion (THD) of the grid currents (Rabie et al. 2021).

To remedy these problems, the use of 3P-4LRs is highly recommended. These converters are suitable to preserve balanced sinusoidal grid voltages and currents under all loading and grid conditions, including unbalanced and other disturbances (Carrasco et al. 2014; Miveh et al. 2016; Mandrioli et al. 2020). The fourth leg, added to the classical 3P-3LR, provides a zero-sequence current (ZSC) channel and regulation, and preserves the ability to handle all unbalanced problems (Olives-Camps et al. 2019; Chebabhi et al. 2015). Four-leg PWM converters are commonly used in

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grid-connected and stand-alone power generation (Olives-Camps et al. 2019; Mandrioli et al. 2020), active filter (AF) (Chebabhi et al. 2015), and distributed static compensator (DSTATCOM) (Dheepanchakkravarthy et al. 2018; Saber et al. 2018).

On the other hand, the performance of the 3P-4LR depends strongly on the selected outer DC-bus voltage controller and three current inner controllers as well. The multiple linear and nonlinear control techniques that have been developed for four-leg PWM converters have the same purpose with various functionalities (Yin and Dieckerhoff 2015). The linear controllers such as PIC and resonant controllers (RC) have been proposed to achieve excellent steady-state (Doan et al. 2017; Dheepanchakkravarthy et al. 2018; Saber et al. 2018). However, the inherent nonlinearities of the 3P-4LR and the undesirable perturbations due to parameters variation affect its dynamics will not only impact the performance and stability of the 3P-4LR linear control, but also lead to poor dynamic responses in transient states (Sun et al. 2016; Djerioui et al. 2019).

To further enhance the performance and to overcome the linear controller problems and limitations, many nonlinear control techniques have been proposed for controlling the four-leg PWM converter in recent years. These approaches include state-space current control (SSCC) (Kaszewski et al. 2014), flatness control (FC) (Djerioui et al. 2019), sliding mode control (SMC) (Pichan and Rastegar 2017; Pichan et al. 2018), fast terminal sliding mode control (FTSMC) (Pichan et al. 2020), and nonlinear backstepping control (BSC) (Chebabhi et al 2016; Badra et al 2017).

Among the aforementioned control techniques, the BSC has been recognized to be an effective control technique due to its advantages of systematic, recursive design, and beneficial performance under various operating conditions. The concept of the BSC technique is to choose appropriate Lyapunov functions depending on the control objectives of various design steps of the overall system (Chebabhi et al 2016; Badra et al 2017). These Lyapunov functions based BSC can ensure asymptotic stability of the system. For these raisons, the BSC has been widely used in renewable energy based distributed resource systems (Roy et al. 2018; Armghan et al. 2020; Aourir et al. 2020). Roy et al. (2018) investigated the BSC of current and voltage for a doubly fed induction generator under balanced and unbalanced grid conditions. Armghan et al. (2020) proposed a BSC of cascade control for DC-microgrid based renewable generation. Aourir et al. (2020) proposed BSC of single stage grid-connected PV system; the stability and robustness against irradiance and parameter variations were verified. As reported in other works, excellent transient and steady-state performances are achieved despite large system parameter variations and unbalanced grid conditions (Sun et al. 2016; Wang et al. 2017). Furthermore, Wai and Yang (2019) adopted the BSC approach for the direct power control of 3P-3LR with the function of controlling both the instantaneous reactive power and DC-bus voltage simultaneously. In these, numerical simulations and experimental results show that the BSC is effective in terms of stability, robustness, harmonic mitigation, and power factor correction. A complete review of the major advantages of BSC in power system applications is presented in (Alyoussef and Kaya 2019). However, in the aforementioned works, the three-leg voltage-source PWM converter is considered as the main device for grid-connected system. Consequently, the ZSC generated in case of unbalanced loads connected to the main grid or under unbalanced grid voltages is not taken in consideration; and the stability and control performance cannot be ensured under these unbalanced conditions.

In this paper, a BSC is suggested to regulate the input currents and DC-bus output voltage of a 3P-4LR in the synchronous rotating frame (dq0-frame) under balanced and unbalanced load and grid conditions. The main contribution in this paper consists of combining the advantages of both 3P-4LR topology and the BSC controller. The 3P-4LR topology is adopted for its ability in providing a ZSC regulation and thus avoiding voltage fluctuation at the point of common coupling (PCC). The BSC controller is designed and proposed for input currents and output voltage control as a decoupling, tracking, and robust controller. The importance of the proposed control approach comes out in obtaining the desired transient and steady-state control performance and power-quality requirements, including the decoupled input currents, response time, robustness, oscillations, current harmonics, and power factor correction. In this work, transient and steady state performances of the proposed 3P-4LR based on BSC are evaluated and compared with those based on PIC in terms of integral performance, trajectory tracking, DC-bus voltage stabilization, reactive power compensation, input current harmonic, ZSC mitigation, neutral current reduction, and power factor correction. The proposed 3P-4LR based on the nonlinear BSC approach illustrates satisfactory results for all the previous performance indicators, which demonstrate its superiority and effectiveness.

This paper is organized as follows: In Sect. 2, the mathematical model of the adopted 3P-4LR tobology is presented. Then, detailed DC-bus voltage and input current control loops based on the proposed BSC technique are developed and detailed in Sect. 3. Section 4 presents the simulation results and discusses the viability and effectiveness of the proposed BSC approach for 3P–4LR. Finally, Sect. 5 summarizes the contributions of this work.

2 Three-phase four-leg PWM rectifier modeling

The 3P-4LR topology connected to the grid at the PCC through magnetically independent filter inductors (L_{fabcn}) with

internal resistors (R_{fabcn}) is illustrated in Fig. 1. The grid is modeled as three sinusoidal voltages (e_{abc}) and a grid neutral line in series with four inductors (L_{gabcn}) having internal resistances (R_{gabcn}) and tied up with the load through DC capacitor (C). The 3P-4LR input currents and grid currents are denoted as i_{fabcn} and i_{gabcn}, respectively. V_{dc}, I_{dc}, I_c, and I_L are the output DC voltage, output DC current, capacitor current, and load current, respectively.

Due to the fourth leg, the 3P-4LR is capable to deliver sixteen switching voltage vector, which is twice the number of voltage vectors of a classical 3P-3LR. These vectors include fourteen active vectors (v_1 to v_{14}) and two inactive vectors (v_0 and v_{15}) (Chebabhi and Fellah 2015). Each voltage vector is well defined by four logical states, which instantaneously lead the four legs of the 3P-4LR (Kumar et al. 2020). The set of voltage vectors delivered by the 3P-4LR are represented by an hexagonal prism in 3D coordinate frame ($\alpha\beta 0$) as shown in Fig. 2.

The mathematical model of 3P-4LR describes the relations beetwin the input voltages (v_{fabc}), currents (i_{fabcn}), and DC-bus voltage (V_{dc}) in abc reference frame is given by the following dynamic equation:

$$\begin{cases} v_{fa} = v_{ga} - R_{fa}i_{fa} - L_{fa}\dfrac{di_{fa}}{dt} + R_{fn}i_{fn} + L_{fn}\dfrac{di_{fn}}{dt} \\ v_{fb} = v_{gb} - R_{fb}i_{fb} - L_{fb}\dfrac{di_{fb}}{dt} + R_{fn}i_{fn} + L_{fn}\dfrac{di_{fn}}{dt} \\ v_{fc} = v_{gc} - R_{fc}i_{fc} - L_{fc}\dfrac{di_{fc}}{dt} + R_{fn}i_{fn} + L_{fn}\dfrac{di_{fn}}{dt} \\ C_{dc}\dfrac{dV_{dc}}{dt} = \left(S_a i_{fa} + S_b i_{fb} + S_c i_{fc} + S_n i_{fn}\right) - I_L \end{cases} \tag{1}$$

where S_a, S_b, S_c, and S_n are the switching states of the 3P-4LR power switches.

The relation between the three-phase input currents i_{fabc} and the neutral phase input current i_{fn} in abc-frame is given by:

$$i_{fa} + i_{fb} + i_{fc} = -i_{fn} \tag{2}$$

By using (2), the ZSC i_{f0} is expressed using the three-phase input currents (i_{fabc}) and neutral input current (i_{fn}) as:

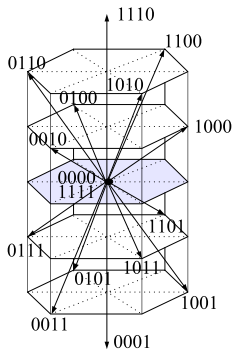


Fig. 2 Prisms and voltage vectors of the four-leg PWM rectifier in the 3D coordinate frame ($\alpha\beta 0$)

$$i_{f0} = \frac{1}{\sqrt{3}}\left(i_{fa} + i_{fb} + i_{fc}\right) = -\frac{1}{\sqrt{3}}i_{fn} \tag{3}$$

This equation demonstrates that the mitigation of ZSC is related directly to the reduction of the neutral input current oscillation magnitude.

The system equations of the 3P-4LR input voltages given by (1) in the dq0-frame becomes:

$$\begin{cases} v_{fd} = v_{gd} - L_f\dfrac{di_{fd}}{dt} - R_f i_{fd} + L_f\omega i_{fq} \\ v_{fq} = v_{gq} - L_f\dfrac{di_{fq}}{dt} - R_f i_{fq} - L_f\omega i_{fd} \\ v_{f0} = v_{g0} - (L_f + 3L_n)\dfrac{di_{f0}}{dt} - (R_f + 3L_n)i_{f0} \\ C_{dc}\dfrac{dV_{dc}}{dt} = \left(S_d i_{fd} + S_q i_{fq} + S_0 i_{f0}\right) - I_L \end{cases} \tag{4}$$

where v_{fd}, v_{fq}, and v_{f0} are the dq0-axes 3P-4LR input voltages, respectively, i_{fd}, i_{fq}, and i_{f0} are the dq0-axes 3P-4LR input currents, respectively, ω is the PCC angular frequency, and S_d, S_q, and S_0 are the switching states in the dq0-frame.

By considering the power balance between the two sides of the 3P-4LR when $P_{AC} = P_{DC}$ based on the grid voltage orientation ($v_{gd} = V_{gmax}$ and $v_{gq} = 0$), the dynamic dq0-axes input currents and DC-bus voltage are expressed as follows:

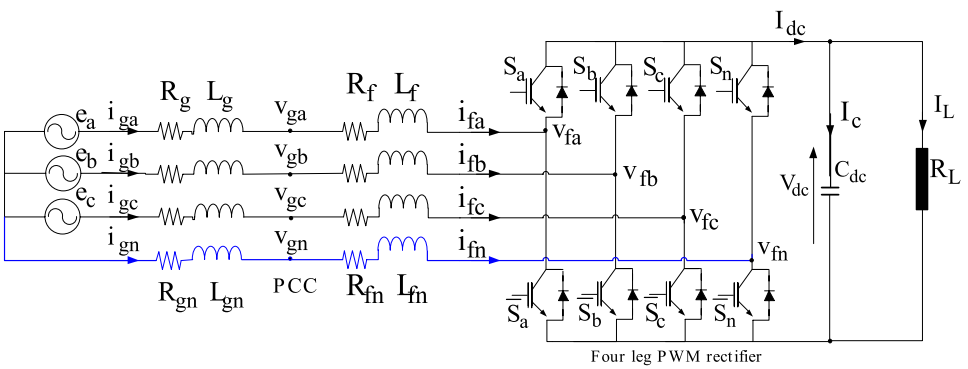


Fig. 1 Structure of four-leg PWM rectifier connected to the grid

$$\begin{cases} \dfrac{di_{fd}}{dt} = -\dfrac{R_f}{L_f} i_{fd} + \omega i_{fq} + \dfrac{v_{gd}}{L_f} - \dfrac{v_{fd}}{L_f} \text{ (a)} \\ \dfrac{di_{fq}}{dt} = -\dfrac{R_f}{L_f} i_{fq} - \omega i_{fd} - \dfrac{v_{fq}}{L_f} \text{ (b)} \\ \dfrac{di_{f0}}{dt} = -\dfrac{(R_f + 3R_n)}{(L_f + 3L_n)} i_{f0} - \dfrac{v_{f0}}{(L_f + 3L_n)} \text{ (c)} \\ \dfrac{dV_{dc}}{dt} = \dfrac{1}{C_{dc}}(I_{dc} - I_L) = \dfrac{v_{gd}}{C_{dc} V_{dc}} i_{fd} - \dfrac{V_{dc}}{C_{dc} R_L} \text{ (d)} \end{cases} \quad (5)$$

where $P_{AC} = v_{gd} i_{fd}$ and $P_{DC} = V_{dc} I_{dc}$.

By observing (2), there are coupling effect between i_{fd} and i_{fq}. In order to realize the decoupling control, the following control variables u_d, u_q, u_0, and u_{dc} are introduced as:

$$\begin{cases} u_d = L_f \dfrac{di_{fd}}{dt} + R_f i_{fd} & \text{(a)} \\ u_q = L_f \dfrac{di_{fq}}{dt} + R_f i_{fq} & \text{(b)} \\ u_0 = (L_f + 3L_n) \dfrac{di_{f0}}{dt} + (R_f + 3R_n) i_{f0} & \text{(c)} \\ u_{dc} = i_{fd} = \dfrac{C_{dc} V_{dc}}{v_{gd}} \left(\dfrac{dV_{dc}}{dt} + \dfrac{V_{dc}}{C_{dc} R_L} \right) & \text{(d)} \end{cases} \quad (6)$$

Using (6), the dynamic model of the 3P-4LR given by system Eqs. (5) becomes:

$$\begin{cases} v_{fd} = -u_d + L_f \omega i_{fq} + v_{gd} & \text{(a)} \\ v_{fq} = -u_q - L_f \omega i_{fd} & \text{(b)} \\ v_{f0} = -u_0 & \text{(c)} \\ i_{fd} = \dfrac{C_{dc} V_{dc}}{v_{gd}} \left(\dfrac{dV_{dc}}{dt} + \dfrac{V_{dc}}{C_{dc} R_L} \right) & \text{(d)} \end{cases} \quad (7)$$

From (7), it is clear that the currents i_{fd} and i_{fq} can be regulated by the decoupling control variables u_d and u_q separately.

3 Proposed control technique

The proposed control scheme in dq0-frame for the 3P-4LR connected to a four-wire grid including the proposed BSC is shown in Fig. 3. As it is shown, the control strategy is founded on voltage/frequency control where the input voltage references are determined by the inner loop controllers and the frequency is provided by a phase-locked loop synchronization method. The q-axis and 0-axis currents of the inner loop are set to zero to achieve UPF control and mitigate the ZSC. The outer DC-bus voltage controller is used to maintain a constant DC-bus voltage and compensate both filter inductances and power switches losses by providing an adequate d-axis input current reference (i^*_{fd}). Three-dimensional space vector modulation (3DSVPWM) technique that was described in (Chebabhi and Fellah 2015; Kumar et al. 2020) is considered in this paper due to its features including constant switching frequency, low input current harmonics, and low DC-bus voltage ripple. The input voltage references $v^*_{f\alpha\beta 0}$ required by the 3DSVPWM technique are obtained by Park transformation of the dq0-axes input voltage references v^*_{fdq0} provided from the proposed BSC to the stationery frame ($\alpha\beta 0$), as illustrated in Fig. 3.

In Fig. 3, the BSC is proposed for the two-cascade outer and inner loops of the 3P-4LR. Indeed, the DC-bus voltage regulation in the outer loop provides i^*_{fd} for the inner current control loop that ensures the input current regulation and ZSC mitigation. The following subsections will be reserved to the proposed BSC design for the outer and inner loops.

3.1 BSC for DC-bus voltage and d-axis input current

By controlling V_{dc} and i_{fd}, two main objectives are intended. The first is to force V_{dc} to track a desired reference value V^*_{dc} in order to accurately provide the appropriate reference i^*_{fd} used in the d-axis input current inner loop. The second objective is to force the d-axis input current to track its reference with zero transient and steady states errors to obtain the d-axis input voltage reference (v^*_{fd}).

The tracking error of V_{dc} is defined as:

$$e_v = V_{dc} - V^*_{dc} = x_v - x^*_v \quad (8)$$

The error time derivative $\dot{e}_v$ can be expressed as:

$$\dot{e}_v = \dot{x}_v - \dot{x}^*_v \quad (9)$$

In order to enforce V_{dc} tracking error e_v to zero asymptotically, the Lyapunov function is defined as $V_v = \frac{1}{2} e_v^2$, and its time derivative is expressed as:

$$\dot{V}_v = e_v \dot{e}_v \quad (10)$$

By using (9) and the dynamic model of Vdc given in (5d), the Eq. (10) becomes:

$$\dot{V}_v = e_v \left(\frac{v_{gd}}{C_{dc} x_v} i_{fd} - \frac{x_v}{C_{dc} R_L} - \dot{x}^*_v \right) \quad (11)$$

In order to ensure the stability of V_{dc} control loop, the term $\left(\frac{v_{gd}}{C_{dc} x_v} i_{fd} - \frac{x_v}{C_{dc} R_L} - \dot{x}^*_v \right)$ must be expressed as:

$$\frac{v_{gd}}{C_{dc} x_v} i^*_{fd} - \frac{x_v}{C_{dc} R_L} - \dot{x}^*_v = -k_v e_v \quad (12)$$

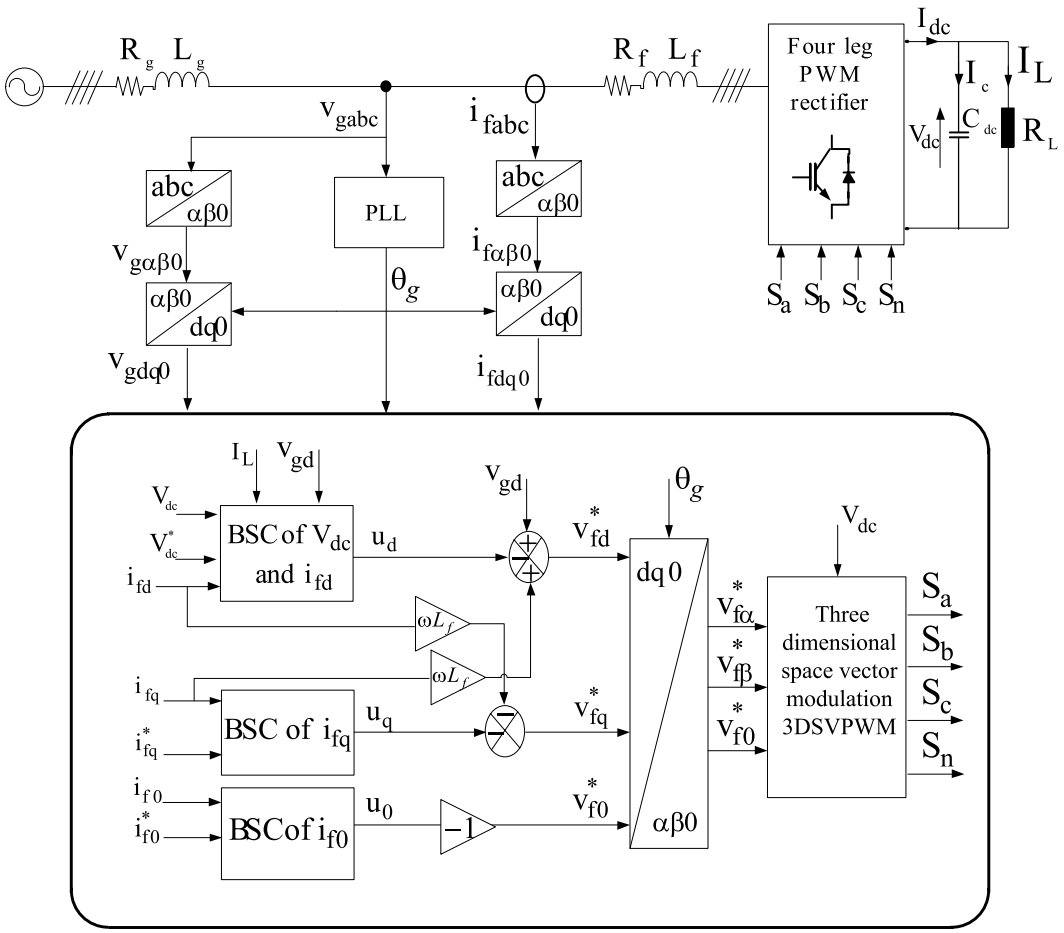


Fig. 3 BSC control scheme of the three-phase four-leg PWM rectifier

where, k_V is a positive constant, which define V_{dc} control loop parameter.

The Lyapunov function given in (11) becomes:

$$\dot{V}_v = -k_v e_v^2 \tag{13}$$

From (13), the control variable $u_{dc} = i_{fd}$ of V_{dc} control loop is given by:

$$u_{dc} = i_{fd}^* = \frac{C_{dc} x_v}{v_{gd}} \left(-k_v e_v + \frac{x_v}{C_{dc} R_L} + \dot{x}_v^* \right) \tag{14}$$

In i_{fd} control loop, the term $\dot{x}_d^* = u_{dc} + \frac{x_v}{R_L}$ can be used as a d-axis input current reference and $x_d = i_{fd}$ as state variable. The i_{fd} tracking error is defined as $e_d = x_d - x_d^*$, and its time derivative can be expressed as:

$$\dot{e}_d = \dot{x}_d - \dot{x}_d^* = \dot{x}_d - \dot{u}_{dc} \tag{15}$$

In order to enforce i_{fd} in tracking the error e_d to zero asymptotically, the corresponding Lyapunov function is defined as $V_d = \frac{1}{2} e_d^2$, and its time derivative can be expressed as:

$$\dot{V}_d = e_d \dot{e}_d \tag{16}$$

Then

$$\dot{V}_d = e_d (\dot{x}_d - \dot{x}_d^*) \tag{17}$$

By substituting $\dot{x}_d$ from (5a) into (17), it results:

$$\dot{V}_d = e_d \left(\frac{1}{L_f} u_d - \frac{R_f}{L_f} x_d - \dot{x}_d^* \right) \tag{18}$$

To guarantee the stability of i_{fd} control loop, the time derivative of the Lyapunov function Eq. (18) must be strictly negative. For this, the term $\left(\frac{1}{L_f} u_d - \frac{R_f}{L_f} x_d - \dot{x}_d^* \right)$ must be expressed as:

$$\frac{u_d}{L_f} - \frac{R_f}{L_f} x_d - \dot{x}_d^* = -k_d e_d \tag{19}$$

where k_d is a positive constant defining i_{fd} control loop parameter.

Substituting (18) and (19), the time derivative $\dot{V}_d$ given by Eq. (16) becomes:

$$\dot{V}_d = -k_d e_d^2 \tag{20}$$

As can be observed from (20), it is clear that the $\dot{V}_d$ is negative. It means that the error e_d will tend close to zero. Thus, the stability of i_{fd} control loop can be ensured.

According to (19), the decoupling control variable u_d of i_{fd} control loop is expressed as:

$$u_d = L_f\left(-k_d e_d + \frac{R_f}{L_f}x_d + \dot{x}_d^*\right) \tag{21}$$

By substituting (21) into (7a), the v_{fd}^* can be expressed as:

$$v_{fd}^* = -L_f\left(-k_d e_d + \frac{R_f}{L_f}x_d + \dot{x}_d^*\right) + L_f\omega i_{fq} + v_{gd} \tag{22}$$

3.2 BSC for q-axis input current

The objective of this controller is to force $x_q = i_{fq}$ to tend to zero with zero steady state error to provide the suitable reactive power compensation. The tracking error of i_{fq} is defined as $e_q = x_q - x_q^*$; and the time derivative of e_q can be expressed as:

$$\dot{e}_q = \dot{x}_q - \dot{x}_q^* \tag{23}$$

In order to enforce i_{fq} tracking error e_q to converge to zero asymptotically, the Lyapunov function V_q is defined as $V_q = \frac{1}{2}e_q^2$, and its time derivative is expressed as:

$$\dot{V}_q = e_q\dot{e}_q \tag{24}$$

$$\dot{V}_q = e_q(\dot{x}_q - \dot{x}_q^*) \tag{25}$$

By replacing $\dot{x}_q$ from (5b) into (25) it results:

$$\dot{V}_q = e_q\left(-\frac{R_f}{L_f}x_q + \frac{1}{L_f}u_q - \dot{x}_q^*\right) \tag{26}$$

Also to guarantee the stability of i_{fq} control loop, the time derivative of the Lyapunov function given by Eq. (26) must be strictly negative. For this, the term $(-\frac{R_f}{L_f}x_q + \frac{1}{L_f}u_q - \dot{x}_q^*)$ must be expressed as:

$$-\frac{R_f}{L_f}x_q + \frac{1}{L_f}u_q - \dot{x}_q^* = -k_q e_q \tag{27}$$

where, k_q is a positive constant define i_{fq} control loop parameter.

By substituting (27) into (26), the time derivative $\dot{V}_q$ given by Eq. (25) is expressed as:

$$\dot{V}_q = -k_q e_q^2 \tag{28}$$

The $\dot{V}_q$ is a exactly negative and the error e_q will tend to zero asymptotically, and the stability of i_{fq} control loop will be also guaranteed.

From (27), the decoupling control variable u_q is expressed as:

$$u_q = L_f\left(-k_q e_q + \frac{R_f}{L_f}x_q + \dot{x}_q^*\right) \tag{29}$$

By substituting (29) and (7b), the q-axis input reference voltage v_{fq}^* can be expressed as:

$$v_{fq}^* = -L_f\left(-k_q e_q + \frac{R_f}{L_f}x_q + \dot{x}_q^*\right) - L_f\omega i_{fd} \tag{30}$$

3.3 BSC for 0-axis input current

The objective of this controller is to force $x_0 = i_{f0}$ to tend to zero with zero steady-state error in order to mitigate the ZSC. The tracking error of i_{f0} is defined as $e_0 = x_0 - x_0^*$ $(x_0^* = 0)$, and its time derivative is expressed as:

$$\dot{e}_0 = \dot{x}_0 - \dot{x}_0^* \tag{31}$$

The Lyapunov function V_0 is defined as $V_0 = \frac{1}{2}e_0^2$, and its time derivative can be expressed as:

$$\dot{V}_0 = e_0(\dot{x}_0 - \dot{x}_0^*) \tag{32}$$

By replacing $\dot{x}_0$ from (5c) into (32), it results:

$$\dot{V}_0 = e_0\left(-\frac{(R_f + 3R_n)}{(L_f + 3L_n)}x_0 + \frac{1}{(L_f + 3L_n)}u_0 - \dot{x}_0^*\right) \tag{33}$$

To guarantee the stability of i_{f0} control loop, the term $\left(-\frac{(R_f+3R_n)}{(L_f+3L_n)}x_0 + \frac{1}{(L_f+3L_n)}u_0 - \dot{x}_0^*\right)$ must be chosen as:

$$\left(-\frac{(R_f + 3R_n)}{(L_f + 3L_n)}x_0 + \frac{1}{(L_f + 3L_n)}u_0 - \dot{x}_0^*\right) = -k_0 e_0 \tag{34}$$

where, k_0 is a positive constant.

Using (33) and (34), the time derivative $\dot{V}_0$ given by Eq. (32) is expressed as:

$$\dot{V}_0 = -k_0 e_0^2 \tag{35}$$

From (34), the decoupling control variable u_0 is given by:

$$u_0 = (L_f + 3L_n)\left(-k_0 e_0 + \frac{(R_f + 3R_n)}{(L_f + 3L_n)}x_0\right) \tag{36}$$

Substituting (36) into (7c), the 0-axis input reference voltage v_{f0}^{*} can be expressed as:

$$v_{f0}^{*} = -(L_f + 3L_n)\left(-k_0 e_0 + \frac{(R_f + 3R_n)}{(L_f + 3L_n)} i_{f0}\right) + v_{g0} \tag{37}$$

Based on the PCC grid voltage orientation and the Eqs. (22), (30), and (37), the dq0-axes input reference voltages $v_{f\sharp q0}^{*}$ are given as:

$$\begin{cases} v_{fd}^{*} = -L_f(-k_d e_d + \dfrac{R_f}{L_f} x_d + \dfrac{C_{dc} x_v}{v_{gd}}(-k_v e_v + \dfrac{x_v}{C_{dc} R_L} + \dot{x}_v^{*})) + L_f \omega i_{fq} + v_{gd} \\ v_{fq}^{*} = -L_f(-k_q e_q + \dfrac{R_f}{L_f} x_q) - L_f \omega i_{fd} \\ v_{f0}^{*} = -(L_f + 3L_n)(-k_0 e_0 + \dfrac{(R_f + 3R_n)}{(L_f + 3L_n)} x_0) \end{cases} \tag{38}$$

4 Simulation study

In order to confirm the viability and effectiveness of the proposed nonlinear BSC in improving the performance of the grid-connected 3P-4LR, several simulation scenarios have been implemented in Matlab/Simulink using the system and the control circuit shown in Figs. 1, 3, respectively. The objectives of these simulation scenarios are to study two different aspects: (a) The effects of the proposed control on response time, reactive power compensation, harmonics and ZSC mitigation, and DC-bus output voltage regulation; (b) The robustness and stability of the proposed control under DC-bus voltage and filter inductors variations, load power and reactive power changes, and grid unbalanced voltage. Along the first one, the BSC based 3P-4LR performance analysis was achieved out at nominal value of filter inductances to get accurate information about the control performance and dynamic responses, after that a comparative study is performed between the proposed BSC and the PIC.

The main indicators considered herein to check the behavior of the 3P-4LR are the power factor operation (first phase grid voltage v_{ga} and its corresponding current i_{ga}), grid currents i_{gabcn} with their THDs likewise their dq0-axes components i_{gdq0}, and essentially the DC-bus voltage. The control errors of DC-bus voltage and dq0-axes input current i_{fdq0} are also represented and analyzed in terms performance integral criteria such as Integral-Absolute-Error (IAE), Integral-Time-Absolute-Error (ITAE), Integral-Square-Error (ISE) and Integral-Time-Square-Error ITSE (Wai et al. 2013; Zamzoum et al. 2020). These errors performance indexes are defined as in (39):

$$\begin{cases} IAE = \displaystyle\int_0^t |x^{*}(t) - x(t)| dt \\ ITAE = \displaystyle\int_0^t t|x^{*}(t) - x(t)| dt \\ ISE = \displaystyle\int_0^t (x^{*}(t) - x(t))^2 dt \\ ITSE = \displaystyle\int_0^t t(x^{*}(t) - x(t))^2 dt \end{cases} \tag{39}$$

where t is the simulation time, and x can be the DC-bus voltage or dq0-axes input currents. The system and simulation parameters and the adopted parameters of the PICs and proposed BSCs are given in Tables 1, 2, respectively.

Table 1 Values of system and simulation parameters

Parameter	Value
AC grid voltage	220 V
Fundamental frequency of grid voltage	50 Hz
DC-bus voltage Vdc	650 V
Capacitor of DC side rectifier C_{dc}	3 mF
DC load resistance R	50 Ω
Input filter inductances L_f, L_{fn}	2 mH, 1 mH
Input filter resistances R_f, R_{fn}	0.15 Ω
Grid inductances L_g, L_{gn}	0.1 mH, 0.05 mH
Grid resistances R_g, R_{gn}	0.1 Ω
Switching frequency f_s	16 kHz

Table 2 PIC and BSC controllers parameters

Controllers	Parameter	Value
PI	Cut-off angular frequency ω_{c-vdc} of V_{dc}	100 rad/s
	Cut-off angular frequency $\omega_{c-if\ dq0}$ of i_{fdq0}	3500 rad/s
	Damping factor ξ	0.707
Proposed BSC	k_v	300
	K_{dq0}	10^8

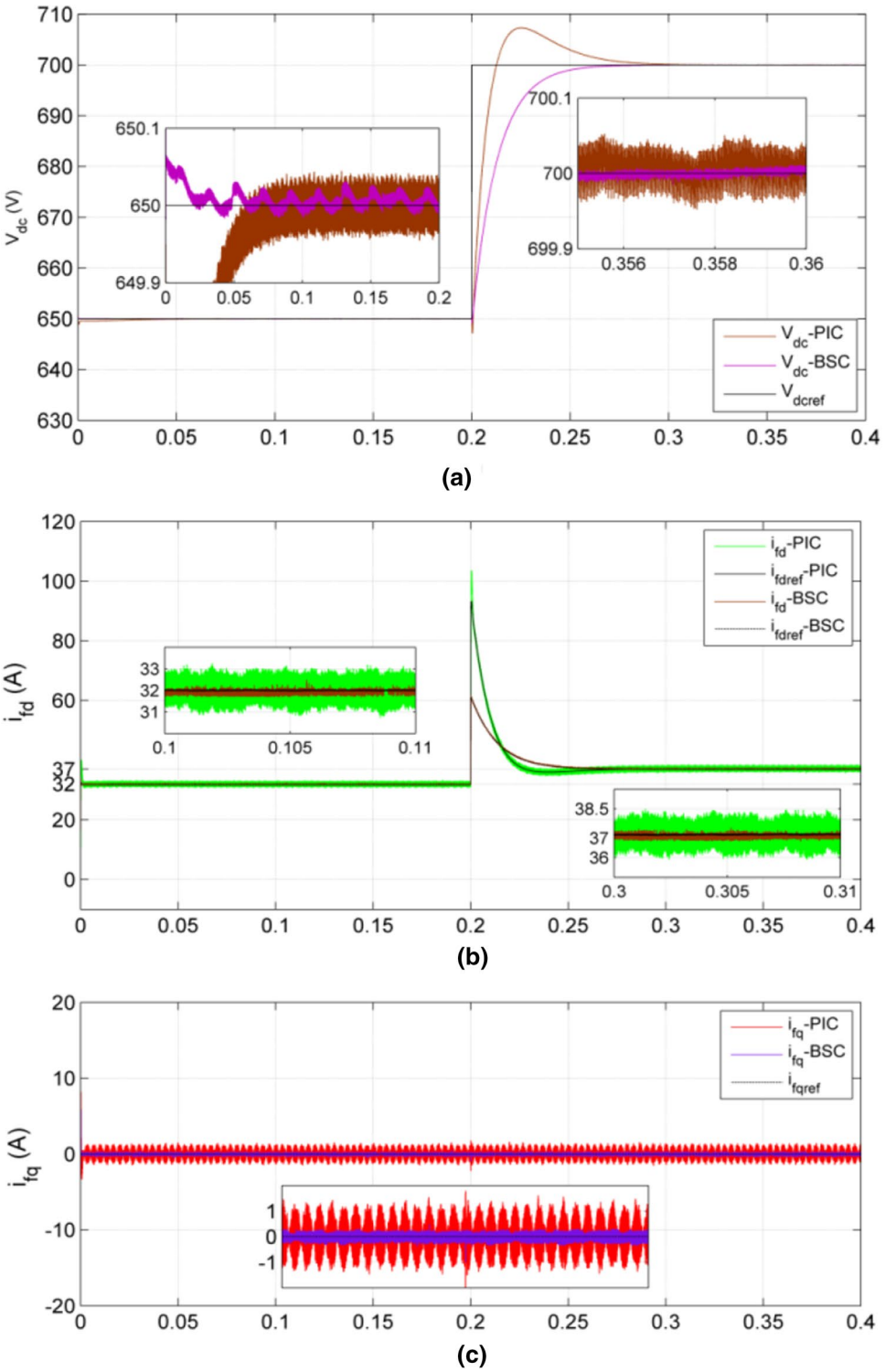
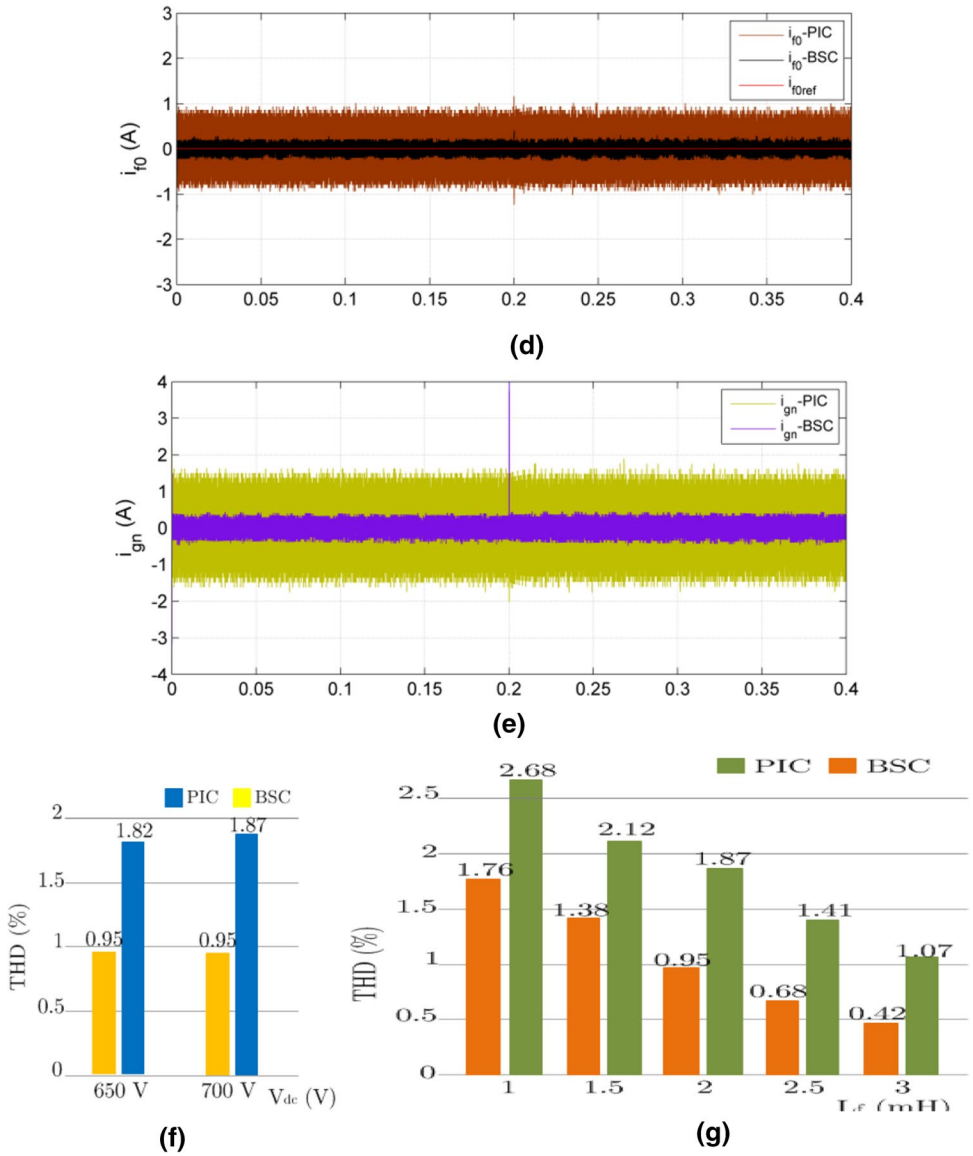


Fig. 4 Comparative study between BSC and PIC in transient and steady states under DC-bus voltage reference change from 650 to 700 V at 0.2 s: **a** DC-bus voltage; **b** *d*-axis input current; **c** *q*-axis input current; **d** 0-axis input current; **e** Neutral current; **f** of Grid-current harmonic analysis before and after DC-bus voltage variation; **g** Grid current THD versus filter inductor variation

Fig. 4 (continued)



At first, a comparative study between the PIC and proposed BSC during DC-bus voltage variation from 650 to 700 V at 0.2 s is performed, as shown in Fig. 4. The oscillation magnitude values for each dynamic response (V_{dc}, i_{fd}, i_{fq}, i_{f0} and i_{gn}) and the integral error performance indexes (IAE, ITAE, ISE and ITSE) values for each controller are analyzed and illustrated in Tables 3, 4, respectively. Also, Fig. 4a, b, c compare the transient and steady-state responses of DC-bus voltage, dq0-axes input currents, and neutral grid current.

According to Fig. 4a, the DC-bus voltage has voltage oscillations before and after the change and an overshoot at the change of DC-bus voltage at t = 2 s. In this, the DC-bus voltage reaches its reference with a fast response at the starting of the 3P-4LR and at the change of DC-bus voltage (t = 0.03 s) with small oscillations before and after this change using proposed BSC as shown in Table 3. From this table, it can be seen also that the maximum values of overshoot are very small than those of the PIC, and

Table 3 Comparison between PIC and BSC in terms of magnitude oscillations under DC-bus voltage change from 650 to 700 V

Controlled variable	Magnitude oscillation values	
	PIC	Proposed BSC
Before DC-bus voltage change		
V_{dc}	0.08 V	0.04 V
i_{fd}	1.8 A	0.8 A
I_{fq}	2.4 A	0.6 A
i_{f0}	1.84 A	0.46 A
I_n	3.2 A	0.8 A
After DC-bus voltage change		
V_{dc}	0.1 V	0.05 V
i_{fd}	2.1 A	1.2 A
I_{fq}	2.4 A	0.7 A
i_{f0}	2 A	0.55 A
I_n	3.6 A	0.94 A

the lowest values of all error's performance indexes are obtained using the proposed BSC.

Figure 4b–e compare the transient and steady-state responses of the dq0-axes input currents and the neutral grid current before and after the DC-bus voltage change for both controllers. The dq0-axes input currents track their references with smaller oscillations in case of BSC compared to the PIC. The maximum value of d-axis input current drawan at the change of DC-bus voltage is 73 A in case of PIC; this value is significantly reduced to 28 A using the proposed BSC. The maximum neutral grid current oscillation is also perfectly reduced from 3.2A using PIC to 0.8 A using BSC before DC-bus voltage change and from 3.6 A using PIC to 0.94 A using BSC before DC-bus voltage change as shown in Fig. 4e and Table 4. The q0-axes input currents are kept constant at zero before and after this change, which demonstrates that the grid UPF operation under DC-bus voltage change is accurately achieved. Moreover, the integral current error performance indexes illustrated in Table 3 and the oscillation magnitude values of each current listed in Table 4 demonstrate that the values of these performance indexes have been enhanced by using the proposed BSC.

Table 4 Comparison between PIC and BSC in terms of the four performance indexes under DC-bus voltage change from 650 to 700 V

		Before DC-bus voltage variation				After DC-bus voltage variation			
		IAE	ITAE	ISE	ITSE	IAE	ITAE	ISE	ITSE
PIC	e_v	$1.107.10^{-2}$	$4.202.10^{-4}$	$2.766.10^{-3}$	$2.765.10^{-5}$	$40.47.10^{-2}$	$8.769.10^{-2}$	7.71	1.579
	e_d	$9.857.10^{-2}$	$9.283.10^{-3}$	0.2238	$5.773.10^{-3}$	0.1154	$3.306.10^{-2}$	0.537	0.1141
	e_q	$5.878.10^{-2}$	$5.667.10^{-3}$	$3.995.10^{-2}$	$3.195.10^{-3}$	$5.571.10^{-2}$	$1.665.10^{-2}$	$3.091.10^{-2}$	$9.203.10^{-3}$
	e_0	$4.783.10^{-2}$	$4.792.10^{-3}$	$2.096.10^{-2}$	$2.099.10^{-3}$	$4.65.10^{-2}$	$1.394.10^{-2}$	$2.012.10^{-2}$	$6.022.10^{-3}$
Proposed BSC	e_v	$1.46.10^{-3}$	$6.016.10^{-5}$	$2.632.10^{-4}$	$5.048.10^{-7}$	$15.72.10^{-2}$	$1.032.10^{-2}$	4.538	0.4109
	e_d	$2.314.10^{-2}$	$2.078.10^{-3}$	$4.536.10^{-2}$	$0.324.10^{-3}$	$2.909.10^{-2}$	$3.948.10^{-3}$	0.1592	$0.8443.10^{-2}$
	e_q	$1.636.10^{-2}$	$1.606.10^{-3}$	$3.899.10^{-3}$	$1.998.10^{-4}$	$1.686.10^{-2}$	$2.529.10^{-3}$	$2.238.10^{-3}$	$3.346.10^{-4}$
	e_0	$1.488.10^{-2}$	$1.459.10^{-3}$	$1.693.10^{-3}$	$1.458.10^{-4}$	$1.633.10^{-2}$	$2.461.10^{-3}$	$1.837.10^{-3}$	$2.779.10^{-4}$

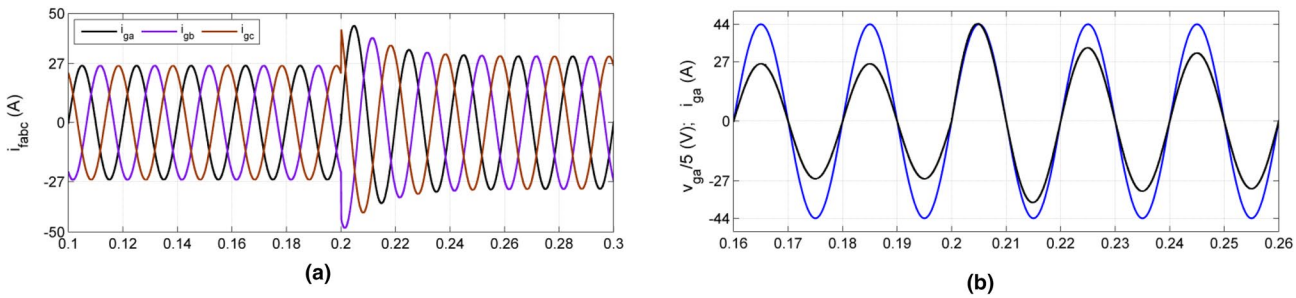


Fig. 5 Dynamic responses of 3P-4LR controlled by BSC under DC-bus voltage change: **a** Three-phase grid currents; **b** First-phase grid voltage and its corresponding current

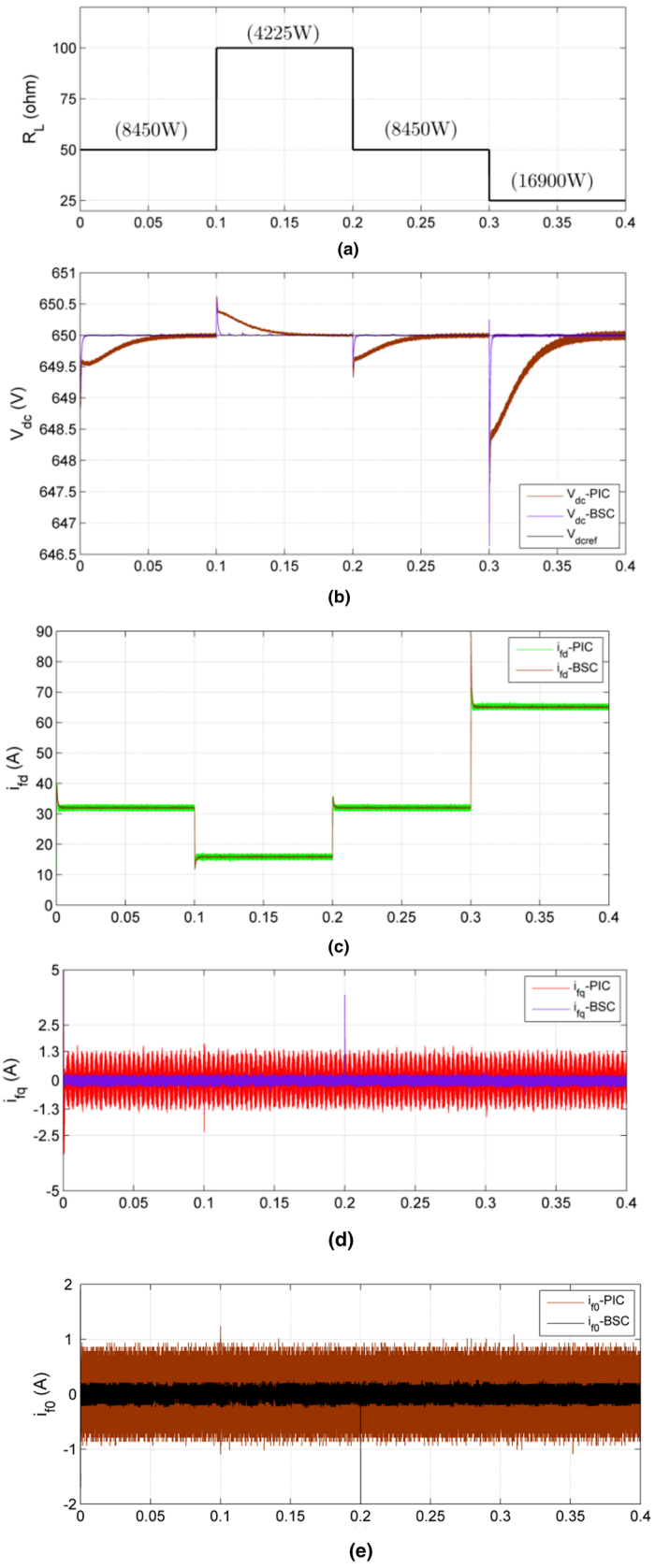
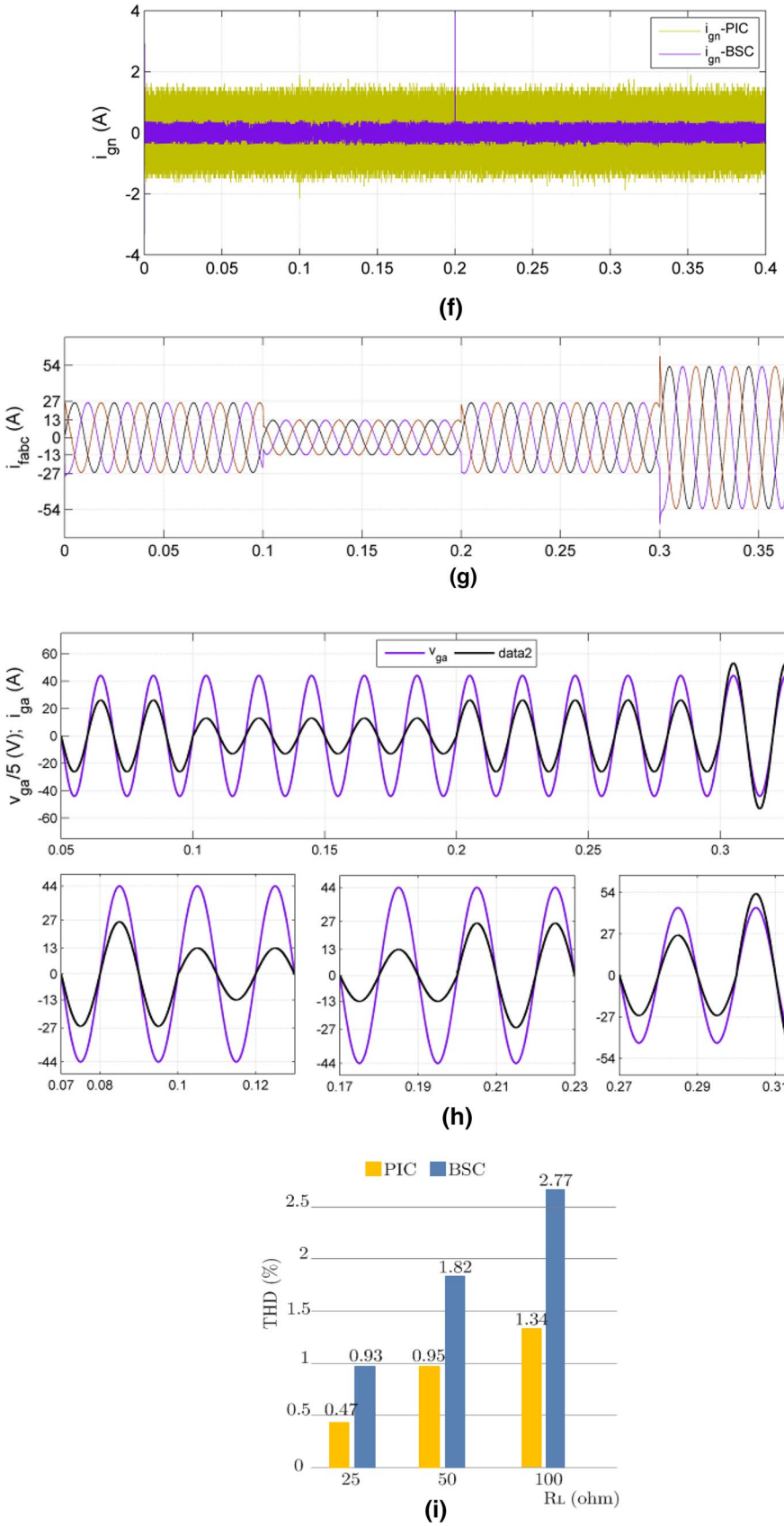


Fig. 6 Dynamic response of 3P-4LR controlled by BSC under load power changes: **a** Load power profile; **b** DC-bus voltage; **c** d-axis input current; **d** *q*-axis input current; **e** 0-axis input current; **f** Neutral current; **g** Three-phase grid currents; **h** First-phase grid current and its corresponding voltage; **i** Grid-current THD versus load power change

Fig. 6 (continued)



The input current harmonics analysis before and after the change of DC-bus voltage are illustrated in Fig. 4f. Using PIC, the THD values are 1.82% before the DC-bus voltage change and 1.87% after this change. These THD values are significantly reduced to 0.95% before and after this change using the proposed BSC, which fits the IEEE 519 standard for current distortion limits.

Figure 4g compares the input currents THDs versus the filter inductance using both controllers, when the filter inductance is varied from 1 to 3 mH (from 50 to 200% of the rated filter inductance $L_f = 2$ mH). From this comparative study, it can be observed that the input currents THDs are decreased from 1.76% to 0.42% using the BSC and from 2.68% to 1.07% using the PIC, which demonstrates again the superiority of the proposed BSC.

The three-phase grid currents (igabc) and the first-phase source voltage and its corresponding current are illustrated in Fig. 5a, b, respectively. It can be observed from these figures that the grid currents are sinusoidal and in phase with their corresponding source voltages before and after the change of DC-bus voltage, which confirms that the grid UPF operation under the DC-bus voltage changing is accurately fulfilled.

Figure 6 shows another comparative study between the conventional PIC and proposed BSC in transient and steady-states during load variations. As shown in Fig. 6a, the load power is reduced from 8450 to 4225 W at $t = 0.1$ s, recovered again to 8450 W at $t = 0.2$ s, and increased at $t = 0.3$ s to 16,900 W. As shown in Fig. 6b, the load power changes cause overshoots and undershoots in the DC-bus voltage response whatever the BSC or PIC is used. However, the BSC provides smaller overshoots and undershoots with a very fast response than the PIC.

As illustrated in Fig. 6c, d, e, the dq0-axes input currents track their references even under load power changes, but with very small oscillations when the BSC is considered. The d-axis input current follows the load power change, while the q0-axes input currents are kept oscillating around zero. Note that also, the oscillation magnitude of the neutral grid current is enhanced by using the proposed BSC compared to PIC, as depicted in Fig. 6f.

The three-phase grid currents (igabc) and the-first phase source voltage and its corresponding currents are illustrated in Fig. 6g, h, respectively. It can be observed from these figures that the grid currents behavior is sinusoidal and can be kept in phase with their corresponding voltages guaranteeing UPF operation of the 3P-4LR. The THD values of the three phase grid currents under load power change are illustrated in Fig. 6i, which demonstrates that the THDs is reduced to smaller values when the load power is reduced and inversely.

The responses of the 3P-4LR controlled by both PIC and the proposed BSC when the q-axis input current reference is changed to – 10 A at 0.1 s and recovered again to zero at $t = 0.2$ s are illustrated in Fig. 7. Figure 7a, b, c, d show that the DC-bus voltage and dq0-axes input currents track their references with small oscillations using the proposed BSC, and the d0-axes input currents are not influenced by the change in the q-axis input current reference. The behavior of neutral grid current is almost the same before and after change in reference of q-axis input current with very small oscillations using the proposed BSC as shown in Fig. 7e.

Also, as can be observed from Fig. 7f, the first phase source voltage and its corresponding current are in phase before 0.1 s, and the grid current lags the corresponding source voltage after 0.1 s, which are recovered in phase after the q-axis input current reference is returned to zero at $t = 0.2$ s. Using BSC, the grid currents THDs have small values and are almost unaffected by the change in reference q-axis input current as shown in Fig. 7g.

The dynamic behavior of the 3P-4LR controlled by both control methods under unbalanced source voltages with a 10% voltage sag in the first phase occurred at $t = 0.1$ s and recovered again to 220 V at $t = 0.2$ s is illustrated in Fig. 8. As shown in Fig. 8b, c, the unbalanced source voltages cause overshoots, undershoots, and second-order harmonic ripples in the DC-bus voltage and d-axis input current responses whatever the BSC or PIC is used. However, the proposed BSC provides better performance than the PIC in terms of overshoots, undershoots, oscillations, ripples and response time. As illustrated in Fig. 8d, e, the q0-axes input currents track their references under unbalanced source voltages with very smaller oscillations using the proposed BSC compared to PIC.

It can also clearly be observed from these figures that the neutral grid current and the power factor are unaffected by the unbalanced source voltages. When compared this case to the balanced source voltages case, the THD values with

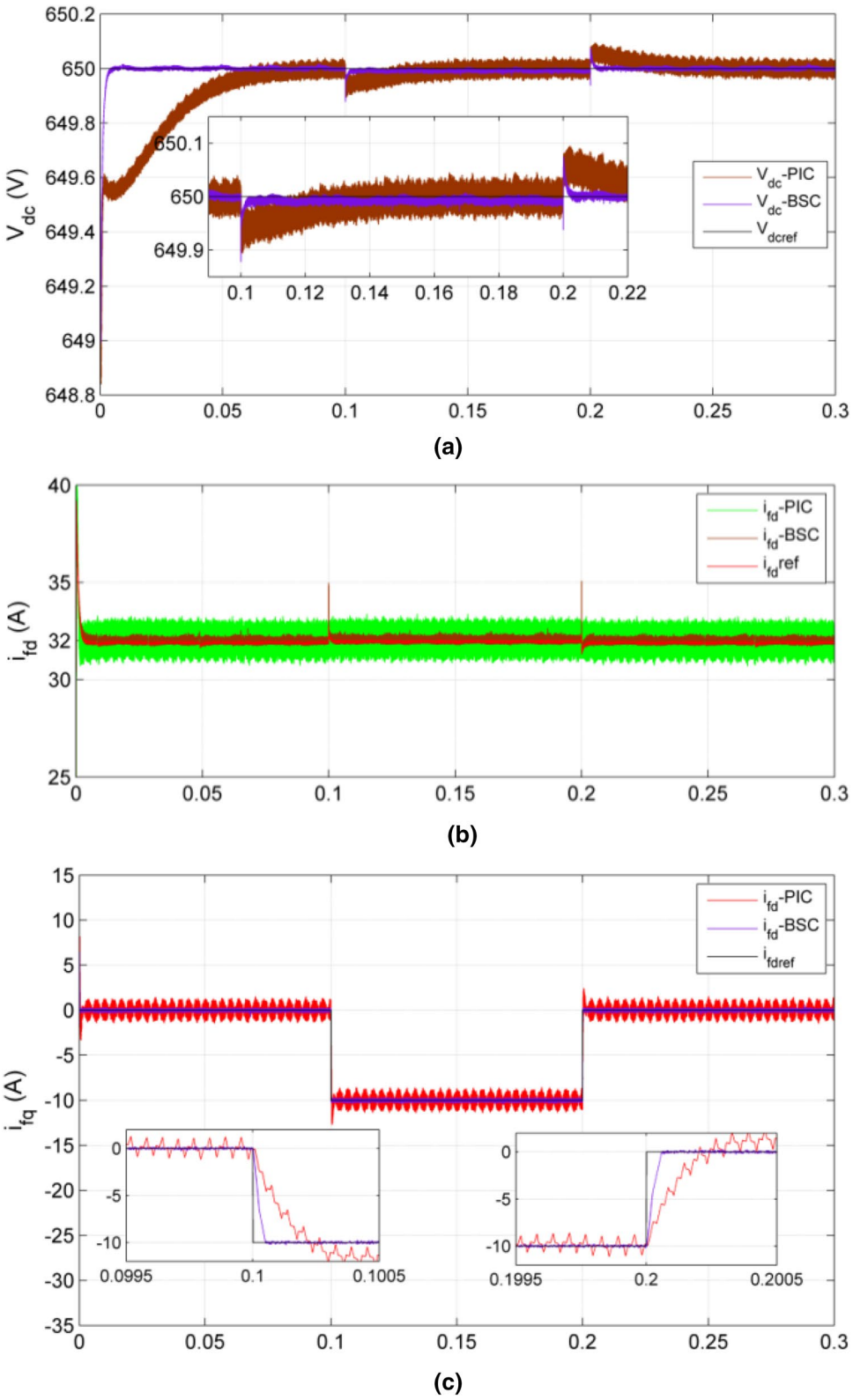
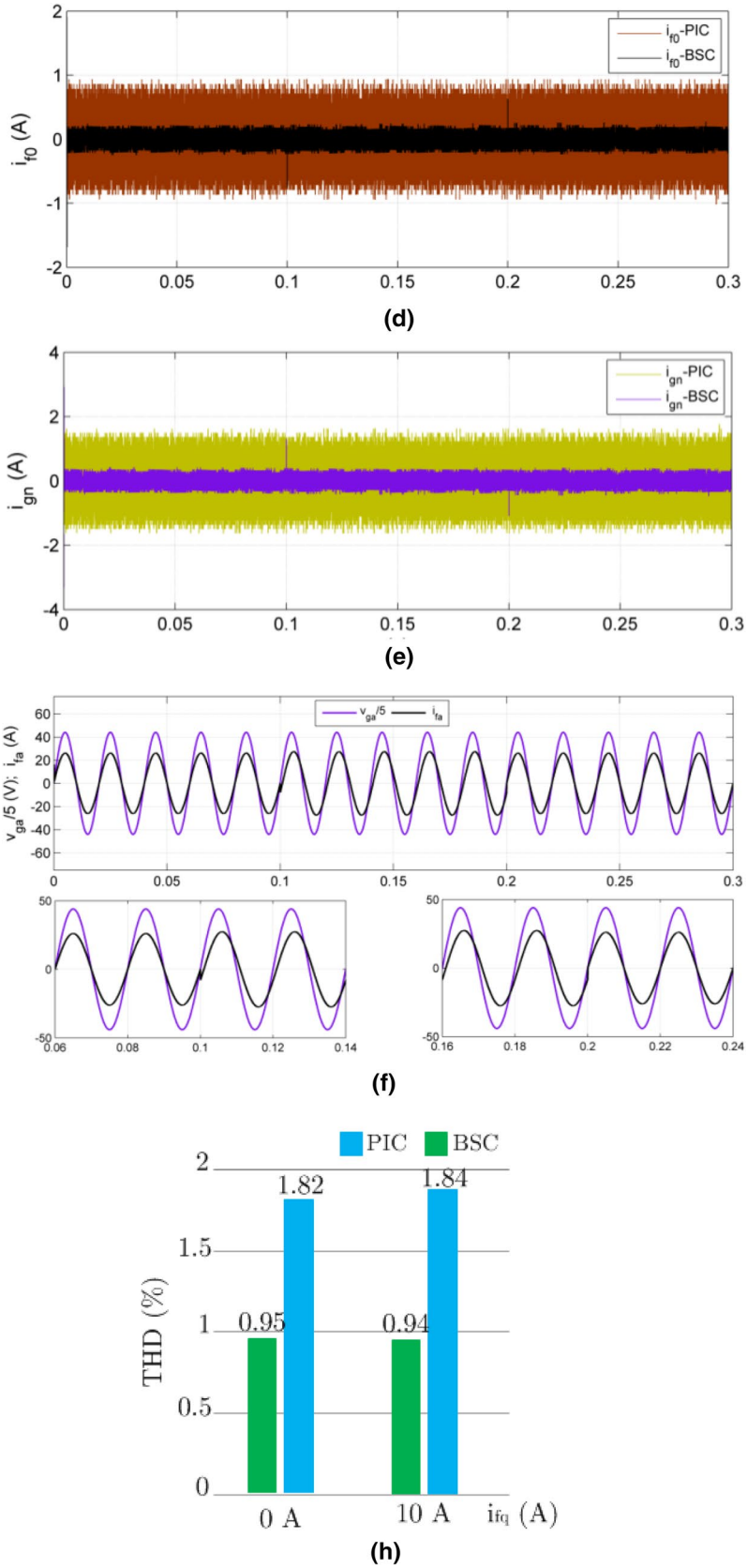


Fig. 7 Dynamic responses of 3P-4LR controlled by BSC under q-axis input current change: **a** DC-bus voltage; **b** d-axis input current; **c** q-axis input current; **d** 0-axis input current; **e** Neutral current; **f** First phase grid current and its corresponding voltage; **g** Harmonic spectrum of grid-current

Fig. 7 (continued)



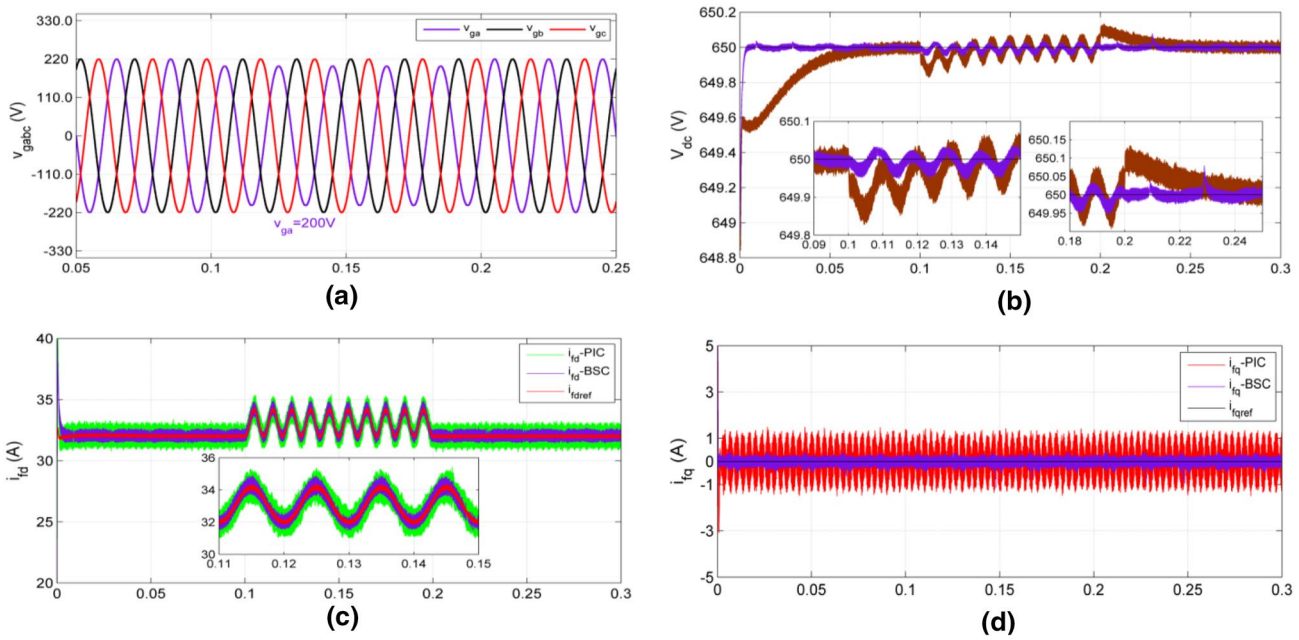


Fig. 8 Dynamic responses of 3P-4LR controlled by BSC under unbalanced grid voltage with 10% a-phase voltage sag: **a** Three-phase source voltages; **b** DC-bus voltage; **c** d-axis input current; **d** q-axis input current; **e** 0-axis input current; **f** Neutral current; **g** Three-phase grid currents; **h** First-phase grid current and its corresponding voltage; **i** Harmonic spectrum of grid-current

the PIC increase from 1.82% to 3.43%, while with the proposed BSC they increase from 0.95% to 2.32%; in this, the proposed BSC outclasses the PIC.

Table 5 presents a qualitative comparison between the PIC and proposed BSC applied on a three-phase grid-connected 3P-4LR. The reference tracking, overshoot, response time, and stability of input currents and DC-bus voltage demonstrate the straight dominance of the proposed BSC. In addition to that, BSC surpasses its counterpart PIC in terms of THDs and oscillations values.

5 Conclusion

In this paper, a backstepping control (BSC) of a three-phase grid-connected four-leg PWM rectifier (3P-4LR) is successfully performed. Comprehensive simulations confirm that the objectives of DC-bus voltage stabilization, power factor correction, sinusoidal input currents, and zero-sequence current mitigation are accurately achieved by using the proposed BSC under both DC-bus voltage and filter inductance variations. The effectiveness, robustness and superiority of the proposed BSC are also verified through a comparative study with PIC based on several performance indices. From this study, the BSC offers excellent steady-state and dynamic control performance compared to the PIC. Indeed, the BSC provides faster DC-bus voltage response time, less oscillations in DC-bus voltage and neutral current, and less input THDs currents as well. Furthermore, the proposed BSC has a high robustness against parameter variations and has the ability to enhance the integral DC-bus voltage and dq0-axes input current error performance indexes compared to the PIC. Other tests involving load power and reactive power changes, and grid voltage unbalanced demonstrate once more the effectiveness of the proposed BSC in terms of response time, power factor, input current THD, and oscillations.

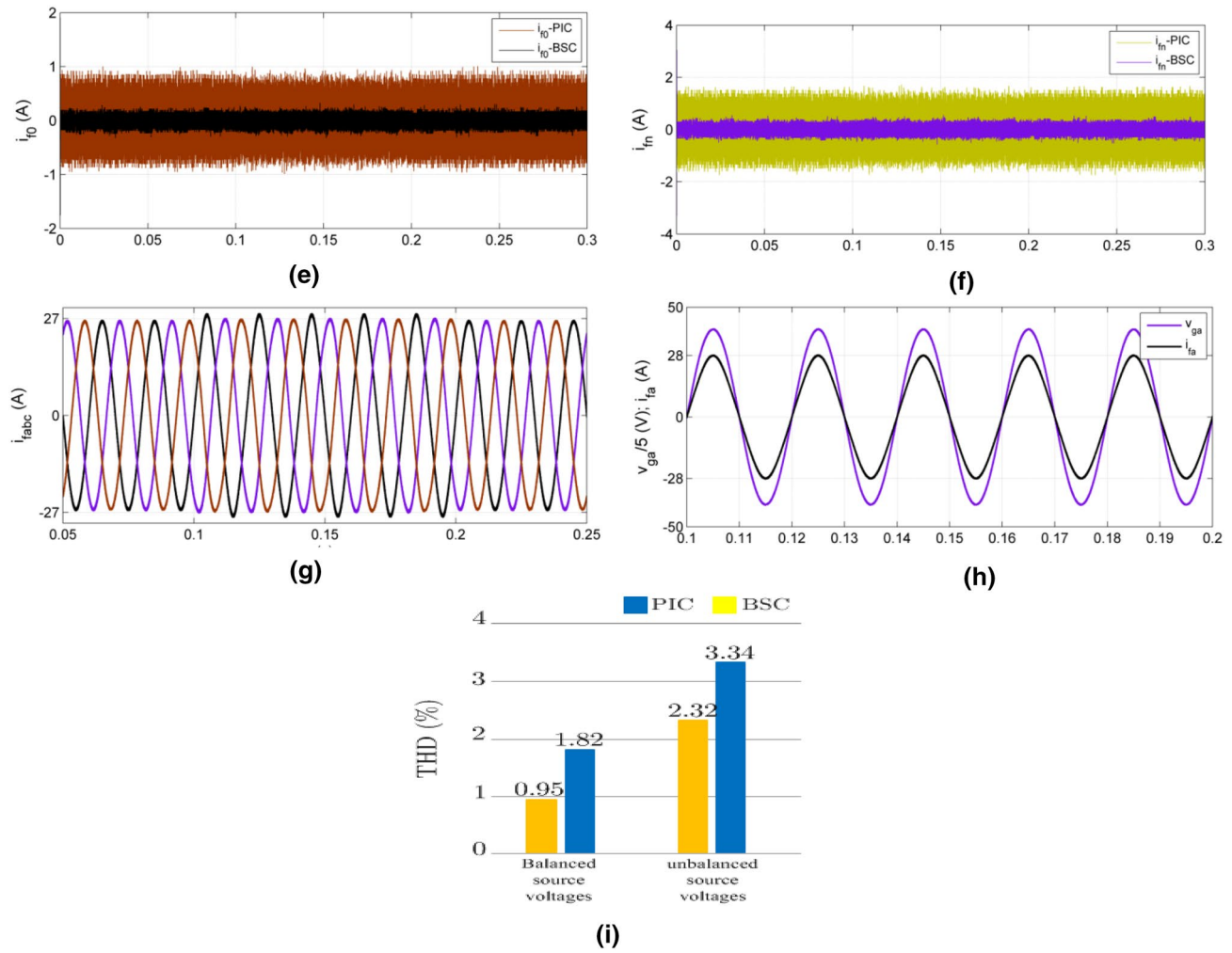


Fig. 8 (continued)

Table 5 Performance comparison resulted from both controllers in all simulation tests

	PIC	Proposed BSC
Reference tracking	Acceptable	Good
Overshoot	High	Very low
Stability	Slow	Fast and asymptotic
Response time	Slow	Very fast
THDs	High	Very small
Oscillations	Large	Very small
Robustness	Poor	High
Steady-state dynamic and control performance	Acceptable	Good and reliable

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Declarations

Conflict of interest All Authors declare that they have no conflict of interest.

Ethical approval This article does not contain any studies with human participants or animals performed by any of the authors.

Informed consent Informed consent was obtained from all individual participants included in the study.

References

Alyoussef F, Kaya I (2019) A review on nonlinear control approaches: sliding mode control back-stepping control and feedback linearization control. International engineering and natural sciences conference (IENSC), 2019 November, pp. 608–619. https://www.icens.eu/2019-icens-book-proceedings-now-available

Aourir M et al (2020) Nonlinear control and stability analysis of single stage grid-connected photovoltaic systems. Intern J Electr Power Energy Syst 115:105439. https://doi.org/10.1016/j.ijepes.2019.105439

Armghan H et al (2020) Nonlinear integral backstepping based control of a DC microgrid with renewable generation and energy storage systems. Intern J Electr Power Energy Syst 117:105613. https://doi.org/10.1016/j.ijepes.2019.105613

Badra MS, Barkat S, Bouzidi M (2017) Backstepping control of three-phase three-level four-leg shunt active power filter. J Fundam Appl Sci 9(1):274–307. https://doi.org/10.4314/jfas.v9i1.18

Bu W, Xu L (2017) Direct power control strategy of PWM rectifier based on improved virtual flux-linkage observer. J Control Sci Eng 2017:1–9. https://doi.org/10.1155/2017/9376735

Carrasco G et al (2014) Control of a four-leg converter for the operation of a DFIG feeding stand-alone unbalanced loads. IEEE Trans Ind Electron 62(7):4630–4640. https://doi.org/10.1109/tie.2014.2364155

Chebabhi A et al (2015) Comparative study of reference currents and DC bus voltage control for three-phase four-Wire four-leg SAPF to compensate harmonics and reactive power with 3D SVM. ISA Trans 57:360–372. https://doi.org/10.1016/j.isatra.2015.01.011

Chebabhi A et al (2016) A new balancing three level three dimensional space vector modulation strategy for three level neutral point clamped four leg inverter based shunt active power filter controlling by nonlinear back stepping controllers. ISA Trans 63:328–342. https://doi.org/10.1016/j.isatra.2016.03.001

Chebabhi A, Fellah MK (2015) 3D space vector modulation control of four-leg shunt active power filter using pq0 theory. Revue Roumaine des Sciences Techniques-Serie Électrotechnique et Énergétique 60(2):185–194. http://revue.elth.pub.ro/index.php?action=main&year=2015&issue=2

Dheepanchakkravarthy A et al (2018) Performance analysis of FPGA controlled four-leg DSTATCOM for multifarious load compensation in electric distribution system. Eng Sci Technol Intern J 21(4):692–703. https://doi.org/10.1016/j.jestch.2018.05.004

Djerioui A et al (2019) Flatness-based grey wolf control for load voltage unbalance mitigation in three-phase four-leg voltage source inverters. IEEE Trans Ind Appl 56(2):1869–1881. https://doi.org/10.1109/tia.2019.2957966

Doan V et al (2017) Design of a hybrid controller for the three-phase four-leg voltage-source inverter with unbalanced load. J Power Electron 17(1):181–189. https://doi.org/10.6113/JPE.2017.17.1.181

Kaszewski A et al (2014). State-space current control for four-leg grid-connected PWM rectifiers with active power filtering function. IEEE 16th international power electronics and motion control conference and exposition, 2014 September, pp.1265–1271. doi: https://doi.org/10.1109/epepemc.2014.6980686

Kumar AP, Kumar GS, Sreenivasarao D (2020) Model predictive control with constant switching frequency for four-leg DSTATCOM using three-dimensional space vector modulation. IET Gener Transm Distrib 14(17):3571–3581. https://doi.org/10.1049/iet-gtd.2019.1775

Lu J et al (2018) An enhanced state observer for dc-link voltage control of three-phase AC/DC converters. IEEE Trans Power Electron 33(2):936–942. https://doi.org/10.1109/tpel.2017.2726110

Mandrioli R et al (2020) A comprehensive AC current ripple analysis and performance enhancement via discontinuous PWM in three-phase four-leg grid-connected inverters. Energies 13(17):4352. https://doi.org/10.3390/en13174352

Mazouz F et al (2020) Adaptive direct power control for double fed induction generator used in wind turbine. Int J Electr Power Energy Syst 114:105395. https://doi.org/10.1016/j.ijepes.2019.105395

Miveh M et al (2016) Control techniques for three-phase four-leg voltage source inverters in autonomous microgrids: a review. Renew Sustain Energy Rev 54:1592–1610. https://doi.org/10.1016/j.rser.2015.10.079

Olives-Camps JC et al (2019) Voltage control of four-leg VSC for power system applications with nonlinear and unbalanced loads. IEEE Trans Energy Conver 35(2):640–650. https://doi.org/10.1109/tec.2019.2957185

Pichan M, Rastegar H (2017) Sliding-mode control of four-leg inverter with fixed switching frequency for uninterruptible power supply applications. IEEE Trans Ind Electron 64(8):6805–6814. https://doi.org/10.1109/tie.2017.2686346

Pichan M, Karimi M, Simorgh H (2018) Improved low-cost sliding mode control of 4-leg inverter for isolated microgrid applications. Inter Trans Electr Energy Syst 28(12):e2642. https://doi.org/10.1002/etep.2642

Pichan M, Arab Markadeh G, Blaabjerg F (2020) Continuous finite-time control of four-leg inverter through fast terminal sliding mode control. Inter Trans Electr Energy Syst 30(6):e12355. https://doi.org/10.1002/2050-7038.12355

Rabie D et al (2021) Study and analysis of voltage source converter control stability for HVDC system using different control techniques. Ain Shams Eng J 12(3):2763–2779. https://doi.org/10.1016/j.asej.2020.12.013

Roy TK et al (2018) Direct power controller design for improving FRT capabilities of DFIG-based wind farms using a nonlinear backstepping approach. IEEE 8th international conference on power and energy systems (ICPES), 2018 December, pp.240–245. doi: https://doi.org/10.1109/icpesys.2018.8626979

Saber B et al (2018) Neutral current compensation of three-phase four-wire distribution system using three-level four-leg DSTATCOM based on simplified 3DSVM Algorithm. IEEE 6th international conference on control engineering & information technology (CEIT) 2018, October, pp. 1–6). doi: https://doi.org/10.1109/ceit.2018.8751759

Song T et al (2020) Suppression method of current harmonic for three-phase PWM rectifier in EV charging system. IEEE Trans Vehic Technol 69(9):9634–9642. https://doi.org/10.1109/tvt.2020.3005173

Sun D, Wang X, Fang Y (2016) Backstepping direct power control without phase-locked loop of AC/DC converter under both balanced and unbalanced grid conditions. IET Power Electron 9(8):1614–1624. https://doi.org/10.1049/iet-pel.2015.0653

Wai RJ, Yang Y (2019) Design of backstepping direct power control for three-phase PWM rectifier. IEEE Trans Ind Appl 55(3):3160–3173. https://doi.org/10.1109/tia.2019.2893832

Wai RJ et al (2013) Design of backstepping control for high-performance inverter with stand-alone and grid-connected power-supply modes. IET Power Electron 6(4):752–762. https://doi.org/10.1049/iet-pel.2012.0579

Wang X, Sun D, Zhu ZQ (2017) Resonant-based backstepping direct power control strategy for DFIG under both balanced and unbalanced grid conditions. IEEE Trans Ind Appl 53(5):4821–4830. https://doi.org/10.1109/ecce.2016.7855399

Yin H, Dieckerhoff S (2015) Experimental comparison of DPC and VOC control of a three-level NPC grid connected converter. IEEE international symposium on power electronics for distributed generation systems, 2015 June, pp.1–7. doi: https://doi.org/10.1109/pedg.2015.7223072

Zamzoum O et al (2020) Performance analysis of a robust adaptive fuzzy logic controller for wind turbine power limitation. J Clean Prod 265:121659. https://doi.org/10.1016/j.jclepro.2020.121659

Zhang R et al (2000) Four-legged three-phase PFC rectifier with fault tolerant capability. IEEE 31st annual power electronics specialists conference (Cat. No. 00CH37018) 2000 June, pp.359–364. doi: https://doi.org/10.1109/pesc.2000.878878