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A. Aib, D.E. Khodja, S. Chakroune, H. Rahali

Fuzzy current analysis-based fault diagnostic of induction motor using hardware co-simulation with field programmable gate array

Introduction. *Presently, signal analysis of stator current of induction motor has become a popular technique to assess the health state of asynchronous motor in order to avoid failures. The classical implementations of failure detection algorithms for rotating machines, based on microprogrammed sequential systems such as microprocessors and digital signal processing have shown their limitations in terms of speed and real time constraints, which requires the use of new technologies providing more efficient diagnostics such as application specific integrated circuit or field programmable gate array (FPGA). The* ***purpose*** *of this work is to study the contribution of the implementation of fuzzy logic on FPGA programmable logic circuits in the diagnosis of asynchronous machine failures for a phase unbalance and a missing phase faults cases.* ***Methodology.*** *In this work, we propose hardware architecture on FPGA of a failure detection algorithm for asynchronous machine based on fuzzy logic and motor current signal analysis by taking the RMS signal of stator current as a fault indicator signal.* ***Results.*** *The validation of the proposed architecture was carried out by a co-simulation hardware process between the ML402 boards equipped with a Virtex-4 FPGA circuit of the Xilinx type and Xilinx system generator under MATLAB/Simulin*k. ***Originality.*** *The present work combined the performance of fuzzy logic techniques, the simplicity of stator current signal analysis algorithms and the execution power of ML402 FPGA board, for the fault diagnosis of induction machine achieving the best ratios speed/performance and simplicity/performance.* ***Practical value.*** *The emergence of this method has improved the performance of fault detection for asynchronous machine, especially in terms of hardware resource consumption, real-time online detection and speed of detection.* References 22, tables 3, figures 19.

Key words: **asynchronous machine, fuzzy current analysis, field programmable gate array, hardware co-simulation.**

Вступ. *В даний час аналіз сигналу струму статора асинхронного двигуна став популярним методом оцінки стану працездатності асинхронного двигуна, щоб уникнути відмов. Класичні реалізації алгоритмів виявлення несправностей машин, що обертаються, засновані на мікропрограмних послідовних системах, таких як мікропроцесори і цифрова обробка сигналів, показали свої обмеження з точки зору швидкості та обмежень у реальному часі, що вимагає використання нових технологій, що забезпечують більш ефективну діагностику. наприклад, інтегральна схема для конкретної програми або програмована вентильна матриця (FPGA).* ***Метою*** *даної є дослідження внеску реалізації нечіткої логіки на програмованих логічних схемах FPGA в діагностику відмов асинхронних машин при несиметрії фаз і обривах фази.* ***Методологія***. *У цій роботі ми пропонуємо апаратну архітектуру на FPGA алгоритму виявлення відмов асинхронної машини на основі нечіткої логіки та аналізу сигналів струму двигуна, приймаючи середньоквадратичний сигнал статора струму як сигнал індикатора несправності.* ***Результати***. *Валідація запропонованої архітектури проводилася шляхом апаратного моделювання між платами ML402, оснащеними схемою Virtex-4 FPGA типу Xilinx та генератором системи Xilinx під керуванням MATLAB/Simulink.* ***Оригінальність***. *Дана робота поєднала в собі ефективність методів нечіткої логіки, простоту алгоритмів аналізу сигналів струму статора та виконавчу потужність плати ML402 FPGA для діагностики несправностей асинхронних машин, досягаючи найкращих співвідношень швидкість/продуктивність та простота/продуктивність.* ***Практична цінність***. *Поява цього методу покращила продуктивність виявлення несправностей асинхронної машини, особливо з точки зору споживання апаратних ресурсів, онлайн-виявлення в реальному часі та швидкості виявлення.* Бібл. 22, табл. 3, рис. 19.

Ключові слова: **асинхронна машина, аналіз нечітких струмів, програмована вентильна матриця, апаратне спільне моделювання.**

Introduction. The advances in electronics, power electronics and control circuits have contributed to the growing use of asynchronous machines in electrical drive systems. The use of asynchronous machines is mainly linked to their robustness, their specific power and their manufacturing cost. Their maintenance and monitoring make it possible to make the installations profitable. It is therefore important to develop diagnostic tools for early detection of faults that may appear in these machines [1].

Usually, diagnostic methods require knowledge of the healthy state of the machine regardless of the physical quantity used. The detection of a fault is based on the comparison of the signature of a given state with a healthy state, by considering an indicator resulting from a measurement that is known to be sensitive to a particular fault [2]. Analysis and processing of measurable quantities in the electrical system, in particular stator currents, has taken a preponderant place in the approaches for detecting and diagnosing faults in electrical machines.

In the last decades, the diagnosis of the asynchronous machine has known a growing enthusiasm on the part of the scientific community. The model approach consists of the analytical modeling of machine [3]. The occupation of Lipo et al. [4] and Cornell et al. [5] all relate to the accurate modeling of the machine. Those of Toliyat are characterized by the winding function and the consideration of space harmonics [6]. On the other hand, Devanneaux et al. studies [7] are based on the multi-winding model. This work has greatly enriched the accurate modeling oriented towards diagnosis. Filippetti's et al. research for the diagnosis defects in the induction motor by using the technique of artificial intelligence [8] and neural networks [9]. The signal approach consists in the detection of indicators or signatures of defects [10]. This operation is carried out by the extraction and quantification of measurable electrical or mechanical quantities of reliable indices related to defects. Work has been illustrated by the search for internal indicators (magnetic field, etc.) [2], others by external indicators (voltage, current, torque, speed) [6]. The system approach consists of extracting and classifying or interpreting the results. A form of automation of the diagnostic procedure from acquisition to decision-making has been developed and presented [11].

Intelligent techniques such as fuzzy logic and neural networks are increasingly integrated into algorithms for detecting the failure of electrical machines, particularly in the classification of faults. Filippetti et al. [9] introduced neural networks for the rotor faults diagnosis, in particular for the detection and estimation of the number of broken bars. In [12] presented a new method for on-line detection of faults in asynchronous machine by monitoring stator current based on artificial neural networks. His essays prove the interest of neural networks for classification and decision making. In [13] introduced the Kalman filter in a parametric study for detection of broken bars with estimation of rotor resistance. Another study [14], in which was presented a method for the diagnosis of electrical faults, based on Park vector approach using the technique of artificial neural networks as a decision criterion for the discrimination between healthy and failed cases. In [15] were proposed a system for identifying and classifying asynchronous machine faults. This system is based on radial function-based neural networks. The author [16] proposed a parameter selection method based on a genetic algorithm. It allows a notable reduction of the dimension of this vector without significant loss of information. In [17] was presented a new estimation model without sensors of inaccessible quantities of asynchronous machine for control and monitoring, based on artificial intelligence techniques, such as artificial neural networks and neuro-fuzzy networks. Furthermore, he gave the notion of neuro-fuzzy extended Kalman filters for the estimation of the internal parameters of asynchronous machine.

Online fault diagnosis plays a vital role in monitoring operation and provides early protection against faults in many industrial areas without stopping production lines. The use of field programmable gate array (FPGA) for implementing fault diagnosis algorithm solves the biggest obstacle of system complexity by reducing interconnections and wiring problems [18].

The condition monitoring and diagnosis of faults that occur in an asynchronous machine makes the machine highly reliable, helping to avoid unplanned downtime, which leads to more lost revenue and interrupted production. This can only be achieved when irregularities produced due to faults are detected as they occur and diagnosed quickly so that appropriate action to protect the equipment can be taken. This requires intelligent control with a performing scheme [19]. Therefore, FPGA architecture based on a hardware implementation of the motor current signal analysis (MCSA) failure detection algorithm and fuzzy logic is suggested in this article to diagnose the fault more efficiently and almost instantaneously.

The **purpose** of this work is to study the contribution of the implementation of fuzzy logic on FPGA programmable logic circuits in the diagnosis of asynchronous machine failures for a phase unbalance and a missing phase faults cases. In this study, we start with the adaptation of the fuzzy logic in order to allow an optimal implementation. This implementation must ensure efficiency, speed of execution and a minimum possible space on the FPGA circuit.

Basic calculation relationships and assumptions. A proposed system consists of a power supply block having an AC-DC inverter node and a DC-AC inverter node, an asynchronous machine, a flux and torque estimation block, a fault based on fuzzy MCSA, a controller block based on direct torque control (DTC) command. The input signals corresponding to the currents at the terminals of the asynchronous machine are transformed into output signals indicating the torque and the flux by the estimation block. These signals are fed into the controller block, which creates input signals for the DTC block, which processes and generates appropriate pulses for the bipolar transistor inverter. The fault diagnosis block receives signals corresponding to the stator currents of the asynchronous motor and gives the states (healthy or faulty) of the asynchronous machine.

The diagnostic block diagram of the asynchronous machine with a fuzzy MCSA implementation based on FPGA is shown in Fig. 1.

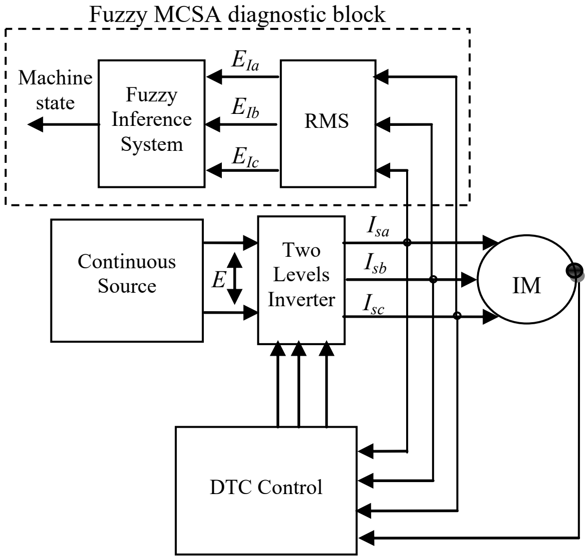


Fig. 1. Schematic of fuzzy-MCSA-based fault diagnosis drive system

Fuzzy inference system will automatically detect the fault of lack of phase, imbalance of the three phases and short circuit also between the turns as soon as it appears on the asynchronous motor.

RMS signal of the asynchronous motor stator phase current is used as a fault indicator signal

$$RMS = \sqrt{\frac{1}{t}\int_0^t u^2(t)\mathrm{d}t} \ . \tag{1}$$

For a periodic signal T, the relation will be:

$$RMS = \sqrt{\frac{1}{2T}\int_0^T u^2(t)\mathrm{d}t} \ . \tag{2}$$

The RMS values for the three phases of stator currents are compared with their nominal values. The results of this comparison give the three fault indicator signals: fault indicator of phase A current (E_{Ia}), fault indicator of phase B current (E_{Ib}) and fault indicator of phase C current (E_{Ic}) in the method proposed in this work.

Signals (E_{Ia}, E_{Ib} and E_{Ic}) represent the linguistic variables for the inputs of the proposed fuzzy inference system. These variables can take three linguistic values: N (negative), Z (zero) or P (positive). Figure 2 shows the fuzzification membership functions of the RMS error.

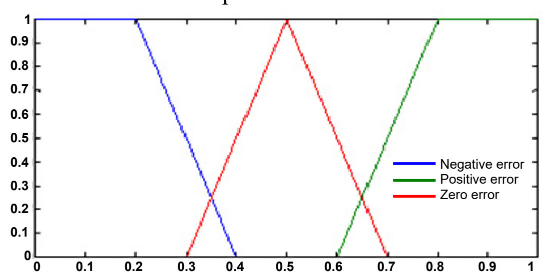


Fig. 2. The fuzzification membership functions of the RMS error

Output signal of the proposed fuzzy inference system is presented by the linguistic variable *EM*, which represents the state of the machine and can take the following linguistic values *S* (Healthy); *D*1 (Fault degree 1°); *D*2 (Fault degree 2°); *D*3 (Fault degree 3°). The fuzzification membership functions of the machine state *EM* is presented in Fig. 3.

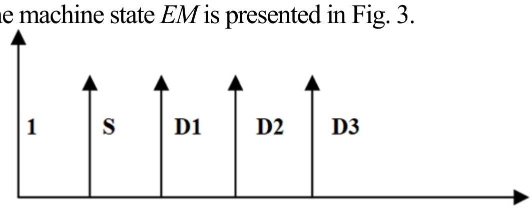


Fig. 3. The fuzzification membership functions of the *EM*

Fuzzy inference system decides according to the following rules:

- if all the fault indicators are zero then the state of the *EM* machine takes the value *S* (Healthy);
- if only one fault indicator is non-zero then the state of the *EM* machine takes the value *D*1 (Fault degree 1°);
- if only two fault indicators are non-zero then the state of the EM machine takes the value *D*2 (Fault degree 2°);
- if all the fault indicators are non-zero then the state of the *EM* machine takes the value *D*3 (Fault degree 3°).

FPGA implementation of RMS function. The RMS block is used to calculate the effective value of a signal using (1) [20]. Consider a signal form $u(t)$ in Fig. 4 a signal form $u^2(t)$ will be as in Fig. 5.

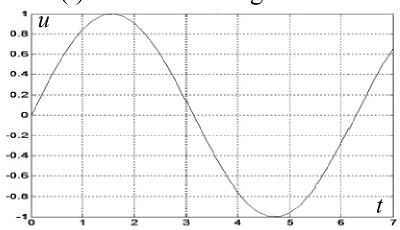


Fig. 4. Signal form $u(t)$

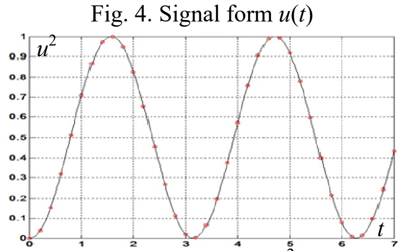


Fig. 5. Signal form $u^2(t)$

A signal sampled by a sampling steps T_e. Signal $u^2(t)$ will only be known at sampling instants. Figure 6 shows the signal $u^2(t)$ sampled. Signal $\int_0^t u^2(t)\mathrm{d}t$ can be approximated by the area between $u^2(t)$ discretized and the time axis as shown in Fig. 7.

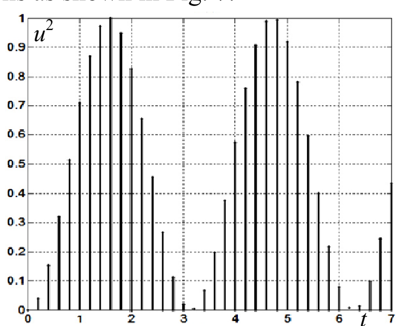


Fig. 6. Sampled $u^2(t)$

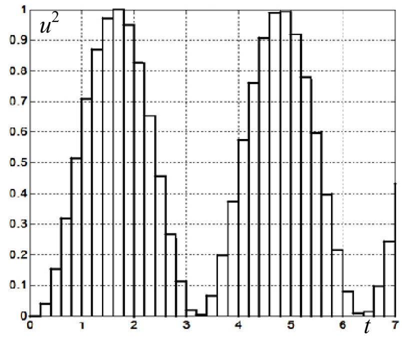


Fig. 7. Area between $u^2(t)$ discretized and the time axis

For *N* samples:

$$\int_0^t u^2(t)\mathrm{d}t \cong \sum_{i=0}^{N-1} u_i^2 \cdot T_e ,$$

so

$$RMS \cong \sqrt{\frac{1}{N \cdot T_e}\sum_{i=0}^{N-1} u_i^2 \cdot T_e} \Rightarrow RMS \cong \sqrt{\frac{1}{N}\sum_{i=0}^{N-1} u_i^2} . \quad (4)$$

The hardware implementation on FPGA we used a counter to count the number of samples, a multiplier to calculate the square of a sampled signal u_i^2, an accumulator to cumulate the values of u_i^2, then multiply the value of the accumulator and the inverse of counter at the end make the square root of it to obtain the result.

The hardware architecture on FPGA of the RMS function is presented in Fig. 8.

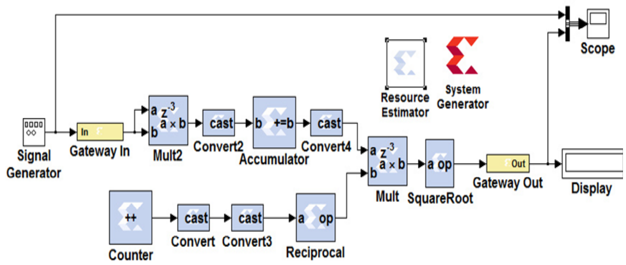


Fig. 8. Hardware architecture on FPGA of the RMS function

FPGA implementation of fuzzy inference system. The hardware implementation of a fuzzy inference system consists in implementing the three phases of a regulation by fuzzy logic: fuzzification, fuzzy inferences and defuzzification.

Fuzzification module implementation. In this study, we employ a memory-oriented approach for implementing the fuzzification module, which allows us to determine the degree of membership in a fuzzy set using a member ship function. This approach calculates the output values offline and stores them in memory. One advantage of this solution is that it simplifies the process of changing a member ship function [21].

To represent each linguistic input/output variable, we use tables that store the degree of membership for each linguistic value. These tables are implemented in hardware using Read Only Memory blocks that can be addressed with a single entry. These memory blocks contain the degree of membership for each linguistic value and provide a representation of the discrete speech universe. For instance, if we have a normalized discourse universe [0, 1] with 64 points of discretization, we would use an address space of

[0:63]. The hardware implementation of these functions is detailed in [22].

Implementation of rule inference and evaluation module. The implementation of rule inference and evaluation is shown in Fig. 9. This module takes three blocks from the fuzzification module as input. The rules selector block helps construct the rule base, which consists of 27 rules. The realization of all the possible combinations between the fuzzy values of «RMS error» makes it possible to obtain this base of rules.

The (min/max) operators are implemented by a 2-1 multiplexer and a comparator on XSG «Xilinx System Generator» hardware tool. If an operator (min/max) has more than two inputs, multiple two-input (min/max) operators are used. For instance, to implement a min operator with three inputs, two min operators with two inputs are employed.

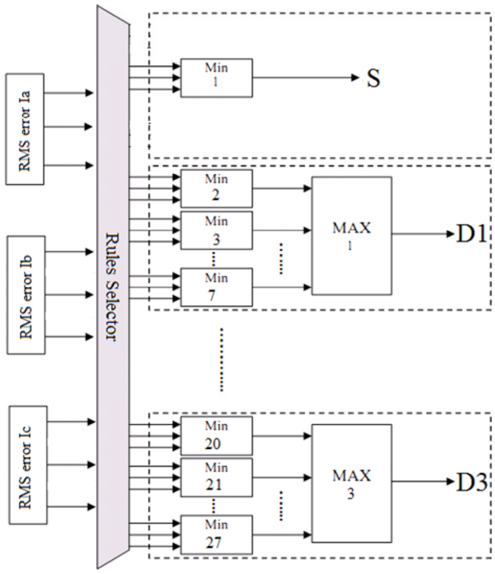


Fig. 9.Architecture of the inference engine module

Implementing the defuzzification module. The hardware description of the defuzzification module is performed by a MAX operator as shown in Fig. 10. The inputs of this module are the outputs of the inference module. The output of this block is representing the output of the entire EM fuzzy block, which represents the state of the machine.

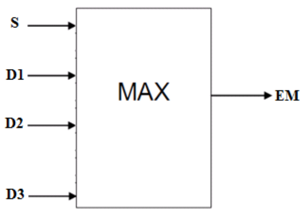


Fig. 10. Defuzzification architecture

Results, simulations and validation. This phase consists of the integration of a fuzzy inference system in the MCSA algorithm for diagnosis of asynchronous machine defects. During this part and similar to the simulation with MATLAB, we will simulate the proposed hardware architecture using the Xilinx generator system.

The diagnostic algorithm is applied to an induction motor, whose specifications are given in Table 1.

Table 1

Induction motor parameters

Stator resistance R_S, Ω	10
Rotor resistance R_r, Ω	6.3
Stator inductance L_S, H	0.4642
Rotor inductance L_r, H	0.4612
Mutual inductance L_m, H	0.4212
Moment of inertia j, kg·m^2	0.02
Machine pair pole number p	2

Synthesis results. Table 2 presents the performances in terms of resource consumption obtained during the implementation of the diagnostic algorithm proposed on the FPGA Virtex 4 given by the architecture presented in Fig. 1.

Note that the proposed architecture optimizes the use of the hardware resources of the FPGA card 4.8 % of slices and 13.7 % of look up tables (LUTs), moreover this architecture considerably reduces the logical components to be used compared to the architectures presented in [19, 21].

Table 2

FPGA proposed diagnostic algorithm

Target Device: ML402 Virtex-4 xc4vsx35-10ff668				
Logic utilization	RMS	Fuzzy system	Available	Utilization
Number of slice flip flops	170	1304	30720	4.8 %
Number of occupied slices	422	1685	15360	13.7 %
Total number of 4 Input LUTs	1286	2173	30720	11.25 %
Number of bonded input output block (IOBs)	65	58	448	27.4 %

Table 3 presents operating frequency comparison between our implementation and previous implementations of induction motor diagnostics algorithms.

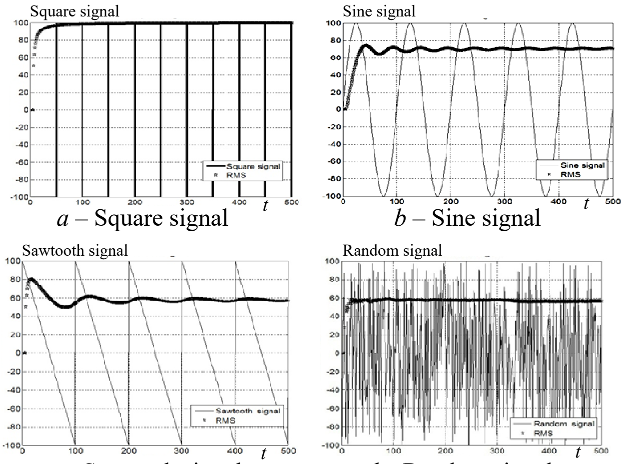
Table 3

Operating frequency comparison

References	[21]	[21]	[19]	Proposed fuzzy MCSA
Device family	Intel Pentium Dual Core processor	FPGA Altera Cyclone-II	FPGA Xilinx Spartan-3E	FPGA Xilinx Virtex-4
Maximum clock frequency	2.95 kHz	45.45 kHz	92.1 MHz	231.64 MHz
Minimum period	338 μs	22 μs	10.857 ns	4.317 ns

The synthesis tool sets the maximum clock frequency at 231.64 MHz, corresponding to a minimum period of 4.317 ns. Table 3 presents a comparative study of the operating frequencies among various references within the same research axis.

MATLAB/Simulink and XSG/Xilinx simulations. The structure of the fuzzy MCSA diagnostic algorithm block is shown in Fig. 1. This proposed algorithm consists of two modules. RMS module is used to calculate the effective value for the three phases of stator currents. This signal is used as the signal fault indicator and the diagnostic module based on a fuzzy inference system, we simulated these modules separately on MATLAB/Simulink with Xilinx generator system. Simulation results of the RMS module for the different types of input signals are illustrated in Fig. 11.



a – Square signal *b* – Sine signal
c – Sawtooth signal *d* – Random signal

Fig. 11. RMS function for different types of input signals

FPGA hardware co-simulation validation. After a simulation step, the proposed hardware architecture was validated by co-simulation on the target device ML402 equipped with a Virtex4 FPGA circuit. This last is dedicated to the implementation of the proposed diagnostic algorithm on a development board integrating an FPGA component. It is mainly intended for the verification and validation of the digital implementation of control and diagnostic algorithms on FPGA targets in a «Hardware in the loop» simulation environment.

Figure 12 shows the principle of validation of the architecture proposed by Hardware co-simulation.

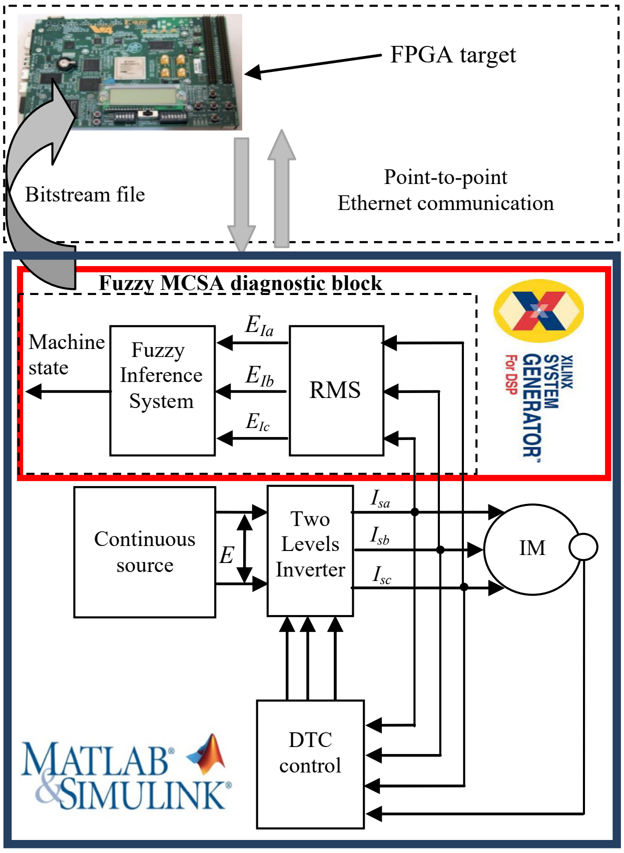


Fig. 12.Hardware in the loop validation of fuzzy MCSA diagnostic algorithm

Upon completion of the simulation and timing analysis, the hardware co-simulation process in XSG follows a procedure to generate a bitstream file from the prototype and a point-to-point Ethernet block. This facilitates the Hardware-in-the-Loop (HIL) procedure. The generated block (Fig. 13) replaces the previously constructed hardware architecture for the fuzzy MCSA diagnostic algorithm.

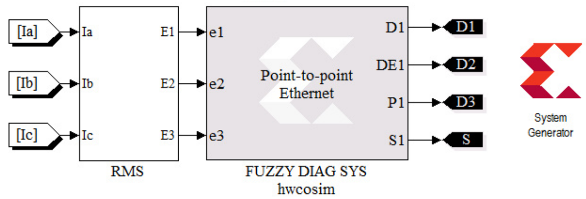


Fig. 13. Fuzzy MCSA diagnostic algorithm HIL point-to-point Ethernet block

During the HIL validation process, the point-to-point Ethernet blocks are connected to both the inverter and the induction motor. In this setup, the motor model, DTC control, and inverter models are simulated in the MATLAB/Simulink environment, while the XSG architectures of the fuzzy MCSA diagnostic algorithm are implemented on the ML402 FPGA device.

To perform the HIL validation, the target device is connected to a PC using an Ethernet cable. This allows for real-time communication and interaction between the simulated models running on the PC and the hardware implementation running on the FPGA device.

1. *For phase unbalance*: phase *A* voltage V_{sa} = 40 % V_{sa} at t = 0.5 s the waveform responses of the induction motor speed, torque, phase voltages and currents are shown in the Fig. 14, 15.

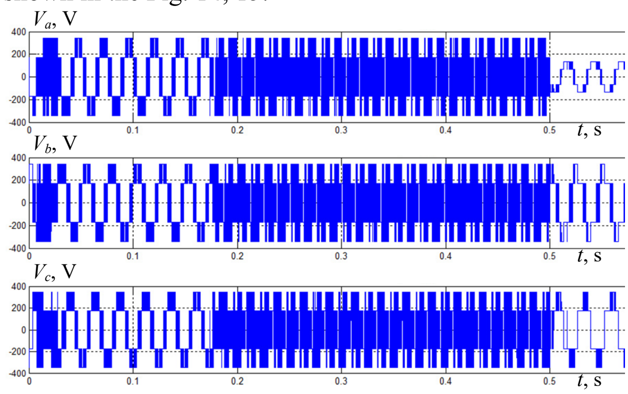


Fig. 14. Behavior of induction motor phase voltages

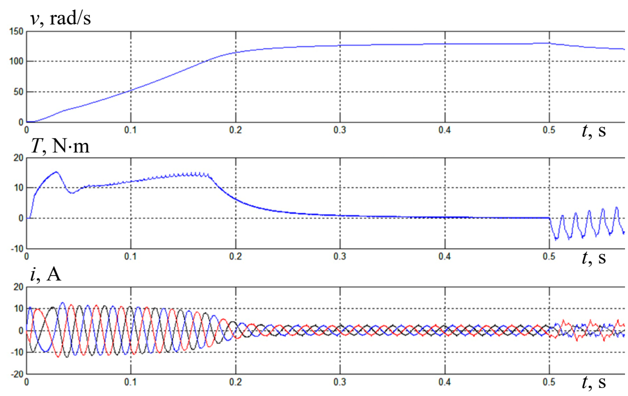


Fig. 15. Behavior of induction motor speed, torque and phase currents

Figure 16 presents the results of the analysis by the fuzzy MSCA algorithm proposed for the phase currents of the previous Fig. 15.

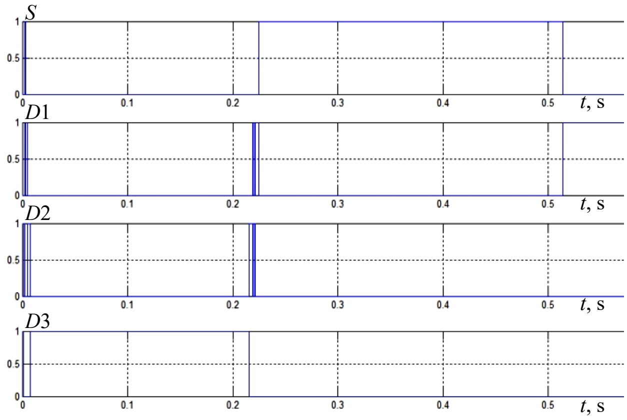


Fig. 16. Proposed fuzzy MSCA analysis of the phase currents

In the machine start-up phase (transient regime) from 0 to 0.2 s the three current phases are greater than their nominal values so it is obvious to have a class *D*3 fault in this time interval.

In the interval 0.2 to 0.5 s the machine reaches their permanent regime and the three current phases resume their nominal values so the state of the machine takes the value Healthy.

At instant 0.5 s a fault appeared and the state of the machine changes from the *S* value to the value *D*1.

The fault does not have a great influence on the dynamic response of the machine speed; this is due to the robustness of the DTC command.

2. *For missing of a phase*: $V_{sa} = 0$ at $t = 0.5$ s the waveform responses of the induction motor speed, torque, phase voltages and currents are shown in the Fig. 17 and 18.

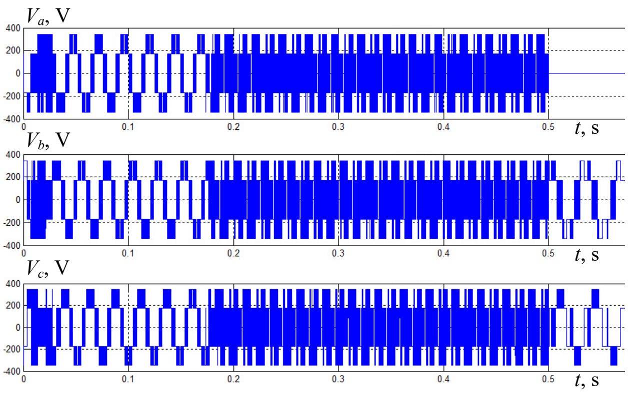


Fig. 17. Behavior of induction motor phase voltage

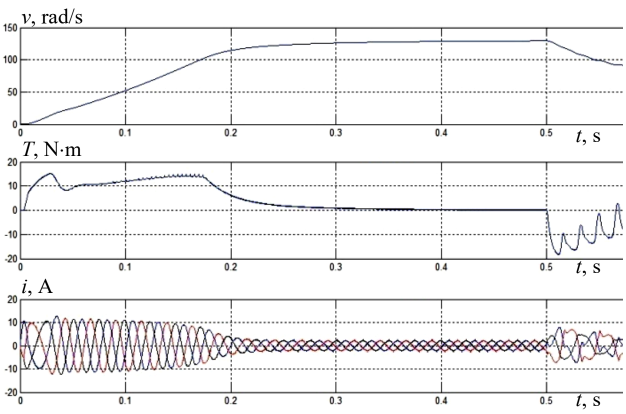


Fig. 18.Behavior of induction motor speed, torque and phase currents

Figure 19 presents the results of the analysis by the fuzzy MSCA algorithm proposed for the phase currents of the previous Fig. 18.

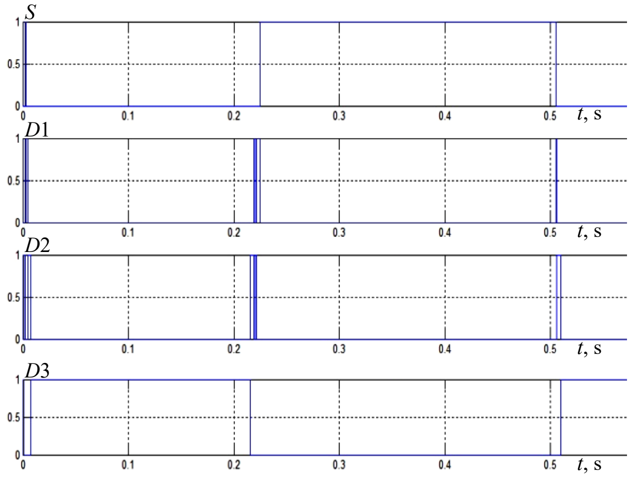


Fig. 19. Proposed fuzzy MSCA analysis of the phase currents

In the machine start-up phase (transient regime) from 0 to 0.2 s the three current phases are greater than their nominal values so it is obvious to have a class *D*3 fault in this time interval.

In the interval 0.2 to 0.5 s the machine reaches their permanent regime and the three current phases resume their nominal values so the state of the machine takes the value Healthy.

At instant 0.5 s a fault appeared and the state of the machine changes from the *S* value to the value *D*3.

The lack of phase fault has a great influence on the dynamic response of the machine speed, this is due to the catastrophic nature of the lack of phase fault.

Conclusions.

1. The purpose of this work was, firstly, to evaluate the performance of the use of field programmable gate array programmable logic circuits for the diagnosis of faults in an asynchronous machine by introducing a fuzzy inference system into the algorithm of the analysis of the motor current signal analysis by taking the RMS signal of the stator phase current as the fault indicator signal. Secondly, to implement and validate the proposed hardware detection algorithm.
2. The originality of our work has been to combine the performance of artificial intelligence techniques, the simplicity of motor current signal analysis algorithms and the execution power of programmable logic circuits, for the definition of a fault diagnosis structure for the asynchronous machine achieving the best simplicity/performance and speed/performance ratios.
3. Finally, we believe that the proposed solution has improved the performance of fault detection for the asynchronous machine, especially in terms of hardware resource consumption, real-time online detection and speed of detection.

Conflict of interest. The authors of the article declare that there is no conflict of interest.

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Abdelghani Aib [1]*, Doctor of Electrotechnical,*
Djalal Eddine Khodja[2]*, Doctor of Electrotechnical, Professor,*
Salim Chakroune[1]*, Doctor of Electrotechnical, Professor,*
Hilal Rahali [1]*, Doctor of Electrotechnical,*
[1] Research Laboratory on the Electrical Engineering,
Faculty of Technology,
University of M'Sila, BP 166, Ichbilia 28000, Algeria,
e-mail: abdelghani.aib@univ-msila.dz;
salim.chakroun@univ-msila.dz (Corresponding Author);
Hilal.rahali@univ-msila.dz
[2] Signals & Systems Lab,
Institute of Electrical and Electronic Engineering,
Boumerdes, 35000, Algeria,
e-mail: djalaleddine.khodja@univ-msila.dz

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