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# Certificate of Participation

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**Fuzzy Direct Torque Control Validation Of Induction Machine By FPGA Hardware Co-simulation**

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# Fuzzy Direct Torque Control Validation of Induction Machine By FPGA Hardware Co-simulation

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***Abstract*— this work describes the development, implementation and validation of hardware architecture on FPGA for fuzzy DTC control of induction motor. This approach enables addressing the primary challenges associated with this control technique, which include mitigating torque ripples, minimizing flux fluctuations, and achieving precise switching frequency control. The introduction of this method has sparked numerous research endeavors aimed at demonstrating its effectiveness and resolving its inherent limitations. Specifically, this study focuses on validating a fuzzy DTC implementation hardware on the development card ML402, which utilizes an FPGA circuit of the Xilinx Virtex-4 type. This validation is carried out using Xilinx system generator and VHDL description language. The results obtained show the effectiveness of the proposed approach for controlling the induction machine and reducing flux and torque ripples.**

***Keywords— Fuzzy Control, FPGA, DTC, power system, XSG.***

## I. INTRODUCTION

The DTC (Direct Torque Control) method developed by TAKAHASHI and DEPENBROCK [1] has gained increasing popularity and garnered significant interest among both researchers and industry professionals working in variable speed applications [2]. However, this approach suffers from two significant drawbacks. Firstly, it exhibits a highly variable switching frequency, and secondly, it struggles to maintain precise control over the ripples of the flux and torque across the entire speed range of operation [3]. It's important to note that these torque ripples not only contribute to additional noise and vibrations but also lead to wear and tear in the rotating shaft, affecting its longevity [4]. To mitigate the adverse effects of these problems on the lifespan of the machines, we believe that using intelligent techniques can offer valuable enhancements.

When it comes to real-time management of intelligent-based applications, there's a growing trend towards adopting new hardware design solutions, notably Field Programmable Gate Arrays (FPGAs) and Application Specific Integrated Circuits (ASICs) [5, 6]. These programmable circuits can serve for implementing algorithms of control as digital platforms within SOCs [7]. The adoption of such an approach offers numerous advantages, including a reduction in execution time through rapid prototyping of digital controls, parallel execution on FPGA, and enabling the application of complex intelligent control techniques that may be computationally intensive. These enhancements contribute to improved control quality in electric machine applications [8].

Advancements in semiconductor technology, micro computing, and the accessibility of speedy control tools like Digital Signal Processors (DSPs) and Field Programmable Gate Arrays (FPGAs) have empowered the scientific community to undertake highly intricate controls, accommodating the non linear mathematical models of asynchronous machines [9].

The primary goal of this study is to assess the effectiveness of employing a fuzzy Direct Torque Control (DTC) inference system in comparison to the traditional DTC method based on hysterized comparators, specifically for controlling induction machines using an FPGA platform.

## II. STRUCTURE OF FUZZY DTC INDUCTION MACHINE CONTROL

The central focus of this research work revolves around the utilization of innovative technological solutions to realize intelligent control through the Direct Torque Control of an induction machine within an environment hardware grounded on an FPGA circuit. This hardware implementation primarily aims to mitigate the fluctuations in electromagnetic torque and stator flux. In this section, we replace the conventional approach of employing two hysteresis regulators and the Takahashi switching table with a fuzzy regulator. Figure 1 illustrates the structure of the induction machine control based on fuzzy DTC.

For this endeavor, we have incorporated an optimized estimator as developed in [10].

## III. IMPLEMENTATION OF FUZZY DTC

### *A. Fuzzy DTC architecture development*

The implementation hardware of a fuzzy logic inference system involves three key: Fuzzification, Defuzzification, and Fuzzy Inferences.

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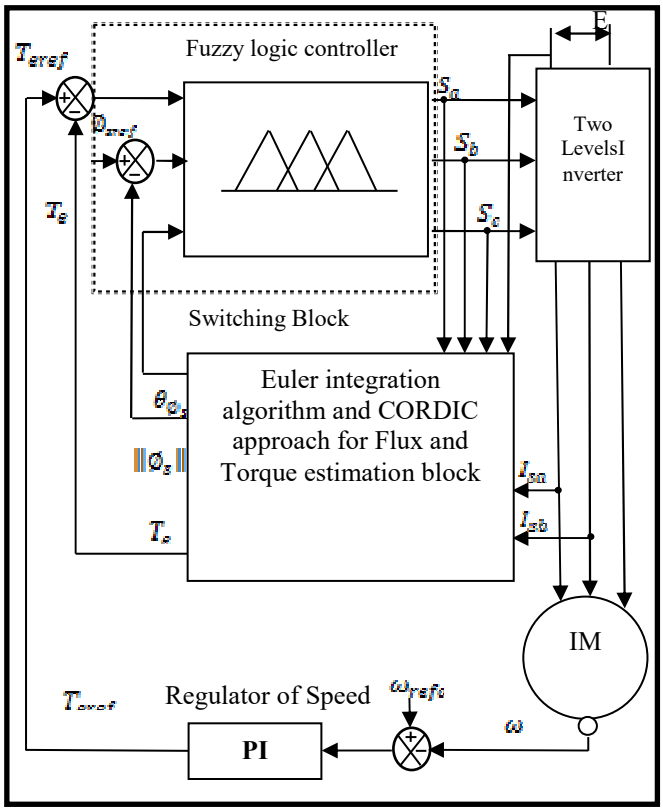


Fig. 1. Structure of Fuzzy DTC induction machine control

*1) Fuzzification module description*

This module is the crucial procedure in order to obtain fuzzy linguistic values based on input data. There are two main approaches in the literature for determining the degree of membership of a linguistic variable in a member ship function. The first approach is the memory-oriented method, where, the output values are pre computed and stored in memory for a finite number of inputs. This approach offers the advantage of flexibility in changing member ship functions. The calculation-oriented method is the second approach, where in order to facilitate the real-time calculation of output values for each member ship function only the characteristics of the member ship functions are stored in memory. For example the triangular member ship functions, these characteristics typically include the slope "a" and the center of the triangle "c". The implementation hardware of this approach involves a combinatorial circuit comprising components like subtractors, adders, multipliers, multiplexers, and often a control unit.

In this work, we have adopted the memory-oriented approach. Specifically, each linguistic output/input variable is represented by tables, with one table for the degree of membership of each linguistic value. These tables are implemented in hardware using ROMs memory blocks, which are addressable by a single input. These memory blocks function similarly to the memory boxes storing the membership degree for linguistic values. To illustrate, for a universe of discourse, let's say for normalized speech ranging from [0:1], discretized into 64 samples, we utilize an address space of [0: 63]. The XSG representation of the proposed linguistic variables is depicted through the architectures hardware shown in Figures 2, 3, and 4.

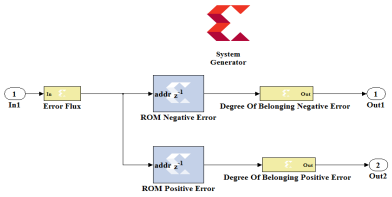


Fig. 2. Linguistic variable "Flux Error" Hardware implementation

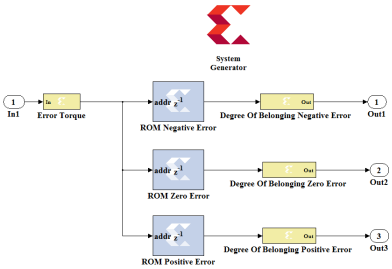


Fig. 3. Linguistic variable "Torque Error" Hardware implementation

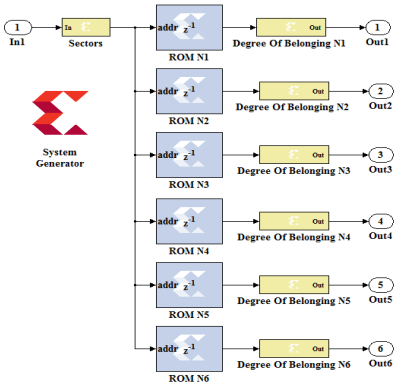


Fig. 4. Linguistic variable "Sectors" Hardware implementation

*2) Implementation of inference module*

The hardware architecture of the fuzzy logic inference system is presented in Figure 5. This block takes three output of the fuzzification block as input. The rules elector block facilitates the construction of the rule base, consisting of a total of 36 rules. These rules are generated by considering all possible cases between values of torque error, flux error and stator flux angle.

The implementation hardware of operators (min / max) with two inputs in "XSG" involves the use of a 2-1 multiplexer and a comparator. The figure 6 illustrates the max/min functions wiring.

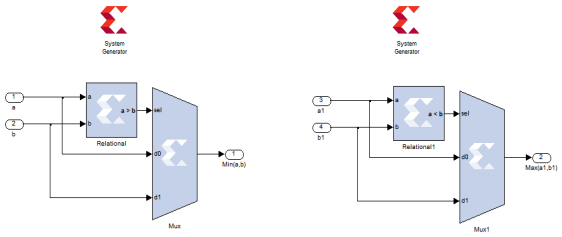


Fig. 6. XSG Max and Min functions Implementation

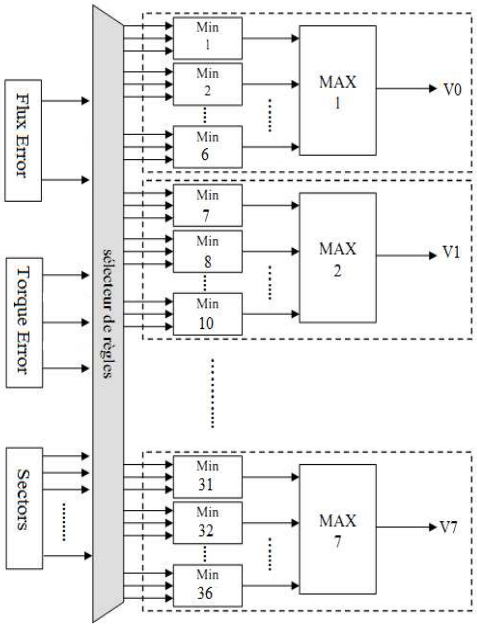


Fig. 5. The module "fuzzy inference" Architecture

For operators (min / max) that involve more than two inputs, a combination of two-input (min / max) operators is employed to implement them. To implement for example a three-input operator, two two-input operators are used.
When composing rules, if multiple rules can be simultaneously activated, each suggesting actions with varying degrees of validity for the same output, we consider these rules to be linked by an OR operator. Mathematically, it's expressed by a Max function.

*3) The Defuzzification module Implementation*

Moving on to the description of the defuzzification module, it is implemented using a MAX function, as depicted at Figure 7. The entrances to this function are the exits from the fuzzy inference block. As mentioned in the previous section, Vi (i : 0 to 7) corresponds to the activation degree of voltages V. The exit of this module is the exit of the entire fuzzy inference system, representing the voltage that needs to be practical to the bounds of the induction machine via the inverter.

Assignments in competitive mode implement the defuzzification MAX function by VHDL hardware architecture.

## *B. Induction machine fuzzy DTC simulation*

In this stage entails the inclusion of the proposed fuzzy inference block into the algorithm of Direct Torque Control. At this section, akin to the simulation performed using SIMULINK, we will simulate the architectures of both conventional DTC control and fuzzy DTC control using Xilinx System Generator.

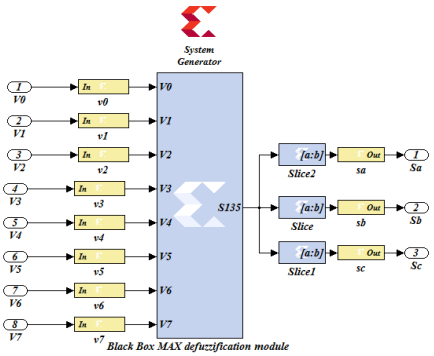


Fig. 7. Defuzzification block VHDL Implementation

The proposed control is applied to an induction motor, and its specifications are detailed in the following table:

TABLE I. INDUCTION MOTOR PARAMETERS

| | |
|---|---|
| $\mathbf{R_S}$ | 10 Ω |
| $\mathbf{R_r}$ | 6.3 Ω |
| $\mathbf{L_S}$ | 0.4642 H |
| $\mathbf{L_r}$ | 0.4612 H |
| $\mathbf{L_m}$ | 0.4212 H |
| **J** | 0.02 kg.m$^2$ |
| **P** | 2 |

The fuzzy DTC control structure, shown in Figure 2, replaces the switching table of DTC control and the hysteresis comparators by a FIS system that has been designed and validated. To facilitate a comprehensive comparison between these two control approaches, we conducted simulations using MATLAB/Simulink integrated with the Xilinx System Generator. The outcomes of these simulations are presented in Figure 8.

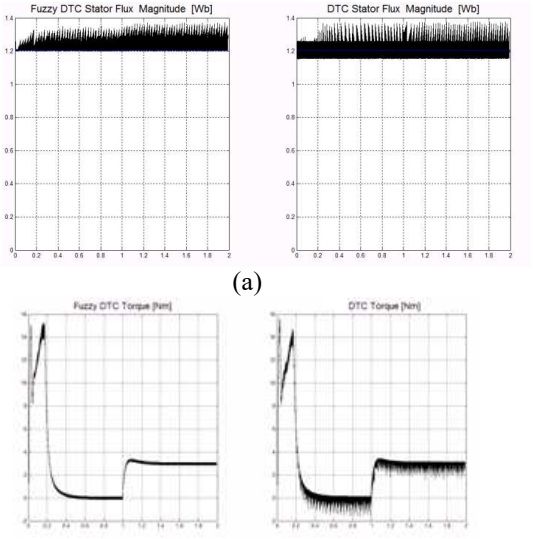


Fig. 8. Flux and torque Comparison between DTC and Fuzzy DTC

The obtained results from the Xilinx System Generator (XSG) simulator for DTC and Fuzzy DTC are illustrated in Figure 8. It is noteworthy that the Fuzzy DTC control demonstrates an enhancement in electromagnetic flux and torque when compared to the classical DTC control, showcasing an important ripples reduction.
Table 2 provides an overview of the performance metrics, specifically utilization of resource, acquired through the fuzzy DTC control architecture implementation on the ML402 FPGA card, as depicted in Figure 1.

TABLE II. FUZZY DTC CONTROL ALGORITHM RESOURCES CONSUMPTION ON FPGA

| **Target Device:ML402 Virtex-4 xc4vsx35-10ff668** | | | |
|---|---|---|---|
| **Logic Utilization** | **Used** | **Available** | **Utilization** |
| **Slice Flip Flops** | 1,365 | 30,720 | 04% |
| **occupied Slices** | 1,620 | 15,360 | 10% |
| **LUTs** | 2,453 | 30,720 | 07% |
| **Input Output Blocks** | 58 | 448 | 12% |
| **RAMB16s / FIFO16** | 12 | 192 | 06% |
| **BUFGCTRLs / BUFG** | 04 | 32 | 12% |

It is evident that the suggested architecture optimally utilizes FPGA hardware resources with only 10% of Slices and 7% of LUTs consumed. Additionally, the maximum clock frequency achieved in this architecture is 231.64MHz, resulting in a minimum period of 4.317ns. In contrast, previous works such as [12] have reported a maximum clock frequency of 54MHz using dSPACE, and [13] had a minimum period of 50ns. These differences in execution time can be attributed to the sequential processing of dSPACE.

The table III provides a comparison of resource consumption between the proposed architecture and previous works in the same research domain.

### *C. The proposed fuzzy DTC hardware architecture Validation*

Following the simulation phase, the proposed hardware architecture of the fuzzy controller underwent validation through hardware in the loop process on the peripheral target ML402 equipped by a FPGA VIRTEX4 card. This crucial step involved the implementation on the FPGA development board the control algorithms. Its primary purpose was to verify and validate the implementation digital of control algorithms on the targets FPGA within a Co-simulation environment "Hardware in the Loop".

The figure Fig.9. shows the principle of validation of architecture proposed by hardware Co-Simulation.

TABLE III. RESOURCES CONSUMPTION COMPARISON

| **Logic Utilization** | **References** | | | | |
|---|---|---|---|---|---|
| | [5] | [14] | [15] | [10] | Proposed Fuzzy DTC |
| **FPGA device family** | Xilinx Virtex-4 | Altera DE-115 | Altera CYCLONE II | Xilinx Virtex-4 | Xilinx Virtex-4 |
| **Multiplier 9-bit elements** | / | 80 | 57 | / | / |
| **Logic elements** | 10.346 | 6.931 | 3.256 | 2.909 | **2.836** |
| **Combinational functions** | 18.594 | 6.491 | 2.549 | 7.411 | **7.686** |

After completing the timing analysis and simulation, the hardware co-simulation procedure in Xilinx System Generator involves generating a bitstream file from the hardware prototype. Additionally, it incorporates an Ethernet Point-to-Point block, which is essential for conducting the HIL procedure.

The produced HIL block in **(Fig. 10.)** substitutes the hardware architecture of Fuzzy DTC that was constructed before.

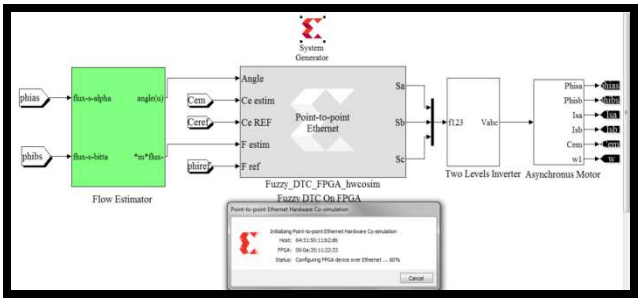

Fig. 10. Ethernet point to point Fuzzy DTC Co-simulation

In Figure 10, you can observe the integration of Point-to-Point Ethernet blocks, connecting the inverter and the induction motor for a Hardware-in-the-Loop simulation. In this scenario, the motor and inverter models are simulated within the Matlab/Simulink environment, while the hardware architectures for Fuzzy DTC are implemented using Xilinx System Generator on the ML402 FPGA device. The Hardware-In-the-Loop validation is executed by connecting the target device to PC via an Ethernet cable.
The figure 12 shows the waveforms of induction machine speed for the proposed control in HIL process.

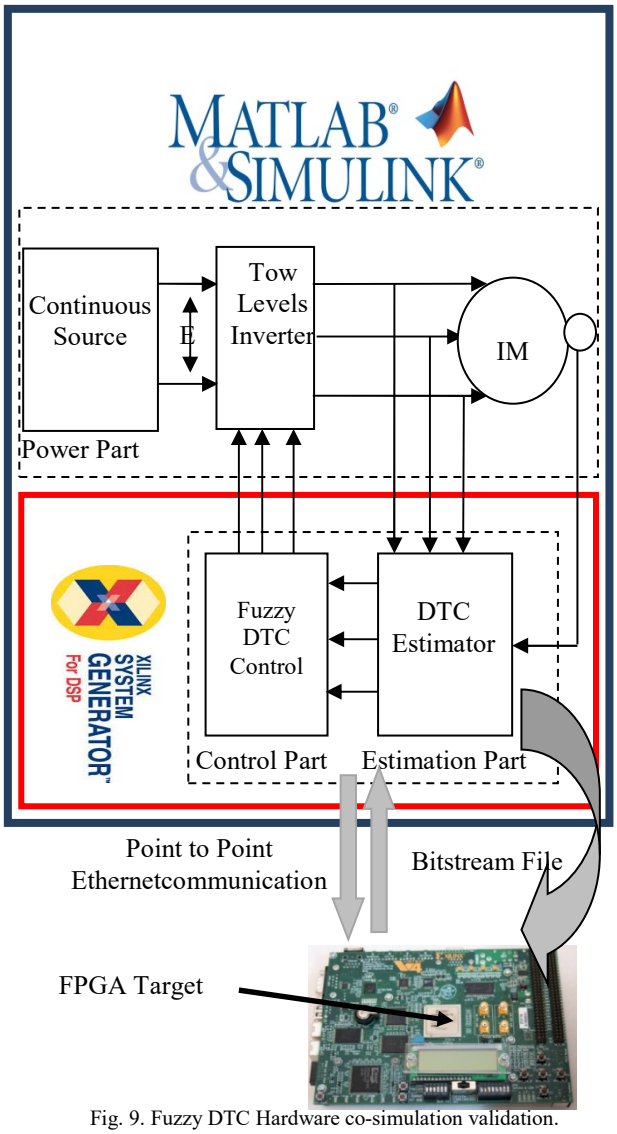


Fig. 9. Fuzzy DTC Hardware co-simulation validation.

Fig. 11. Fuzzy DTC Point to Point Ethernet HIL process

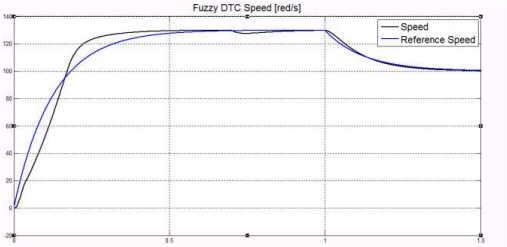


Fig. 12. Behavior of induction motor speed

### ❖ Spectral Analysis & Performance Comparison

In Figure 13, MATLAB's the analysis by Powergui FFT Tool reveals the electromagnetic torque spectrum for the classical DTC as presented in [17]. Figure 14 displays the spectrum for the neuronal DTC described in [8], while Figure 15 illustrates the spectrum for Fuzzy DTC.

During steady-state operation, conventional DTC exhibits harmonics in the electromagnetic torque spectrum, unlike Fuzzy DTC, which maintains a harmonics-free spectrum.

Table 4 provides a comprehensive comparison of the maximum ripple band and RMS error for both stator flux and electromagnetic torque in three control approaches: classical DTC, neuronal DTC, and Fuzzy DTC.

This comparison quantifies the performance and control quality, emphasizing Fuzzy DTC's ability to minimize harmonics and enhance control stability, as reflected in the spectral analysis results.

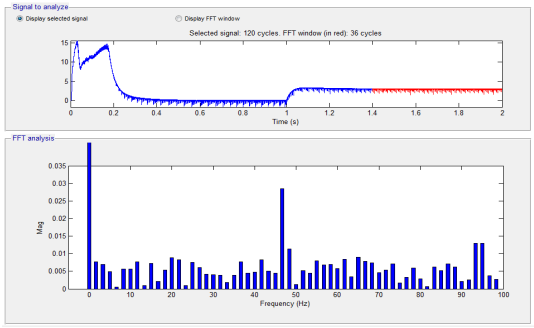


Fig. 13. Conventional DTC torque Powergui Spectral analysis

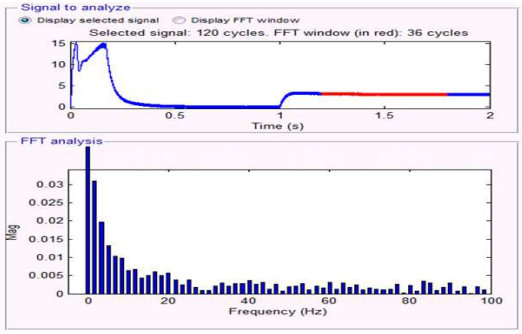


Fig. 14. Neuronal DTC torque Powergui Spectral analysis

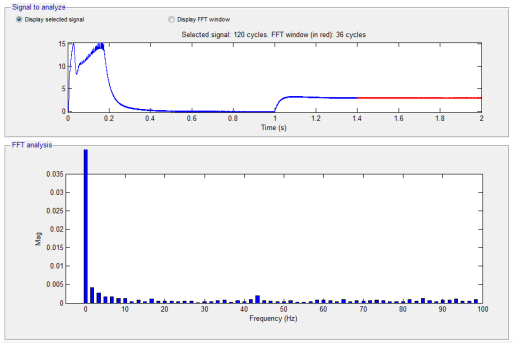


Fig. 15. Fuzzy DTC torque Powergui Spectral analysis

TABLE 4. PERFORMANCE METRICS COMPARISON

| | | Error RMS | min-max |
|---|---|---|---|
| **Electromagnetic Torque (N · m)** | **Classical DTC** | 0.0367 | 2.164 |
| | **Fuzzy DTC** | **0.0096** | **0.827** |
| | **Neuronal DTC** | 0.0314 | 0.955 |
| **The stator flux magnitude (Wb)** | **Classical DTC** | 0.0024 | 0.250 |
| | **Fuzzy DTC** | 0.0017 | 0.171 |
| | **Neuronal DTC** | **0.0011** | **0.090** |

The results presented in Table 4 clearly demonstrate the effectiveness of intelligent techniques-based DTC control in significantly reducing ripples in both stator flux and electromagnetic torque compared to classical DTC control. Among the intelligent techniques, the proposed fuzzy DTC control architecture stands out as it not only excels in reducing ripples but also demonstrates superior performance in terms of hardware resource consumption.

## IV. CONCLUSION

In summary, this work aimed to enhance the performance dynamic of DTC control practiced to asynchronous machine powered by two levels inverters through including a fuzzy inference block. The primary objectives were to prove the feasibility of this approach and evaluate its control quality. The development, implementation, and validation of hardware architecture on FPGA for fuzzy DTC control of induction motors were detailed.

The novelty of this work lies in the fusion of the power of computational programmable logic circuits and the techniques of artificial intelligence, leading to a control structure that achieves optimal ratios of speed-to-performance and simplicity-to-performance. Unconventional tools of control we reutilized to realize a commutation strategy without the need for the hysteresis comparators and switching table typically used in standard DTC approach.

In conclusion, the proposed solution has not only improved the dynamic performance of induction motors but has also significantly mitigated the drawbacks associated with conventional DTC control, including torque ripples, flux ripples, and switching frequency issues. This worker presents a notable step forward in advancing the control of induction motors with the integration of intelligent techniques and hardware implementation.

## ACKNOWLEDGMENT

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