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FPGA Hardware in the Loop Validation of Fuzzy MCSA current analysis-based fault diagnostic of induction motor

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FPGA Hardware in the Loop Validation of Fuzzy MCSA current analysis-based fault diagnostic of induction motor

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***Abstract*— Currently, the analysis of the stator current signal of induction motors (known as MCSA) has gained popularity as a method to evaluate the operational condition of asynchronous motors and prevent potential breakdowns. Traditional approaches for detecting faults in rotating machinery, relying on micro-programmed sequential systems like microprocessors and DSPs, have demonstrated its limits in terms of real-time requirements and processing speed. To address these challenges, it has become essential to embrace cutting-edge technologies, such as ASICs or FPGAs, which offer more efficient diagnostic capabilities. The innovation in our research lies in the development of a fault detection algorithm implemented on FPGA hardware architecture for a induction machines. This algorithm leverages fuzzy logic and analyzes the stator current signal (MCSA), specifically by considering the "Root Mean Square" (RMS) of the stator current as an indicator of potential faults. To validate this architecture, we conducted hardware in the loop validation procedure using Xilinx Virtex-4 ML402 FPGA board and XSG within the Matlab/Simulink environment. Our hardware architecture has significantly enhanced the fault detection performance in induction machines, notably in terms of online real-time detection, detection speed, and resource utilization.**

Keywords— FPGA, Hardware Co-simulation, XGS, Fuzzy current analysis, Diagnostics, Asynchronous machine.

I. INTRODUCTION

Progress in power electronics, control circuitry, and electronics has played a pivotal role in the increasing adoption of induction machines in electrical systems drive. The utilization of induction machines is primarily attributed to their durability, power efficiency, and cost-effectiveness in manufacturing. Effective monitoring and maintenance of these machines contribute significantly to the profitability of installations. Consequently, there is a pressing need to create diagnostic instruments for the early identification of potential faults that could manifest in these machines.

In general, diagnostic techniques necessitate an understanding of the machine's normal operating condition, irrespective of the specific physical parameter being observed. Identifying a fault involves comparing the characteristic pattern of a specific state with that of a healthy state. This comparison relies on an informer derived from a known measurement to be responsive to a particular defect. The analysis and manipulation of quantifiable quantities within electrical systems, particularly currents of stator, have assumed a significant role in strategies aimed at detecting and diagnosing faults in electrical machines.

In recent years, there has been a growing interest within the scientific community in diagnosing induction machines. The model-based approach involves analytically modeling the machine, with researchers like Lipo and Cornell focusing on highly accurate modeling [1,2,3]. Toliyat's work stands out for its incorporation of winding functions and consideration of space harmonics [4]. In contrast, Ritchie's studies are centered on a multi-winding model [5]. Furthermore, researchers like Filippetti have delved into the appliance of neural networks and techniques of artificial intelligence for diagnosing defects in induction motors [6,7]. The signal-based approach revolves around the detection of indicators or signatures of faults [8].

Intelligent methods like neural networks and fuzzy logic are progressively being incorporated into methods designed for the identification of failures in electrical machines, especially in fault categorization [9]. Filippetti, for example, introduced neural networks for diagnosing rotor faults, with a specific focus on detecting and estimating the quantity of broken bars [10]. Online defect identification holds a crucial position in monitoring the maneuver of machinery and offers early safeguards against defect across various manufacturing sectors, all while keeping production lines in continuous operation. The utilization of FPGA for the implementation of fault diagnosis algorithms effectively addresses one of the primary challenges of system complexity through decrease wiring and interconnections issues [11].

To ensure the reliable operation of asynchronous machines and minimize unplanned downtime, online condition monitoring and fault diagnosis play a crucial role.

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Detecting irregularities caused by faults in real-time enables prompt action to protect the equipment and prevent revenue loss and production interruptions. Achieving this requires intelligent control and an efficient diagnostic scheme [12].To address these needs, this work proposes a FPGA architecture that incorporates a hardware implementation of fuzzy logic and failure detection algorithm MCSA. This approach ensures more efficient and almost instantaneous fault diagnosis.

The objective in this study is the implementation of fuzzy logic on an FPGA circuit. The goal of this implementation is to investigation the influence of hardware integration solutions (FPGA) in induction machine failures diagnosis for a lack of phase fault case. In our research, we initiate by customizing fuzzy logic to enable an optimal implementation. This implementation is geared towards ensuring efficiency, rapid execution, and minimal space usage on the FPGA circuit.

II. DESCRIPTION OF THE PROPOSED SYSTEM

The diagnostic block diagram in Figure 1 depicts the configuration of an asynchronous machine with an FPGA-based fuzzy MCSA implementation. The system comprises various components, including an inverter DC-AC and a converter power supply block AC-DC, a block of flux and torque estimation, an induction machine, a block of DTC controller, and a fuzzy MCSA defect diagnosis block.

The DTC block handles the signals of currents and generates the necessary inverter pulses.

The block of defect detection receives signals representing the induction machine stator currents and assesses the condition of the asynchronous machine, discerning whether it is operating in a healthy state or if a fault is present.

The fuzzy inference system is designed to autonomously detect faults such as phase loss, three-phase imbalance, and short circuits between turns as soon as they manifest in the induction machine. It relies on the stator phase current RMS signal as a indicator of defect.

$$RMS = \sqrt{\frac{1}{t}\int_0^t u(t)^2.dt} \quad (1)$$

The relation for a periodic signal typically done by:

$$RMS = \sqrt{\frac{1}{2T}\int_0^T u(t)^2.dt} \quad (2)$$

The RMS values of the stator currents in the three phases are evaluated against their specified nominal values. This evaluation produces three fault indicator signals: EIa, EIb, and EIc, as outlined in the methodology introduced in this research.

These signals, namely EIa, EIb, and EIc, serve as the fuzzy parameters for the proposed fuzzy inference system linguistic inputs. These parameters are able to be categorized into three fuzzy states: negative by N, null by Z, and positive by P.

The fuzzy inference system's output signal is denoted as the EM linguistic variable, which signifies the situation of the machine and be able to adopt one of the next linguistic states: Hale(S); Fault°01 (D1); Fault°02 (D2) and Fault°03(D3).

The fuzzy inference system makes decisions based on the subsequent directives:

- When all indicators of defect are zero, then EM is classified as S: Healthy.
- When exactly two indicators of defect are zero, then EM is classified as D1.
- When only one indicator of defect is zero, then EM is classified as D2.
- When all indicators of defect are non-zero, then EM is classified as D3.

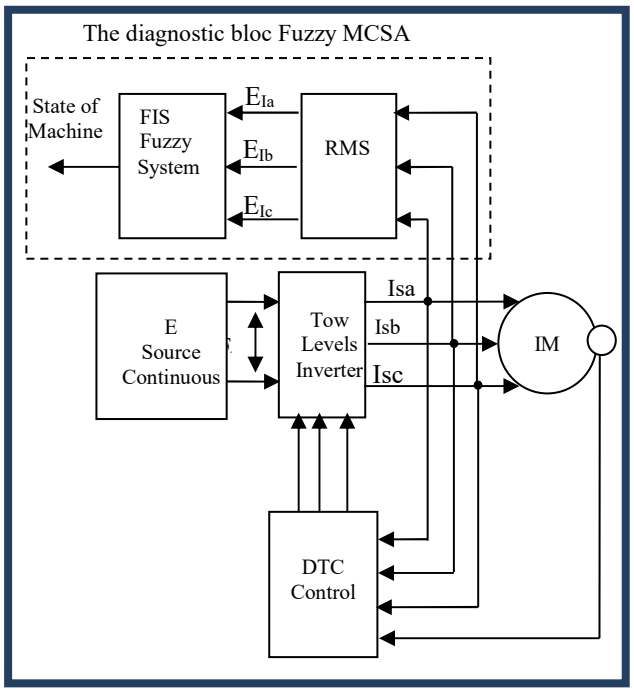


Fig. 1. Schematic of fault diagnosis by Fuzzy-MCSA

III. RMS FUNCTION IMPLEMENTATION ON FPGA

The effective value of a signal is calculating by the block RMS "Root Mean Square" using the following formula [9]:

- $$RMS = \sqrt{\frac{1}{t}\int_0^t u(t)^2.dt} \quad (3)$$

Consider a periodic signal u(t). $u(t)^2$ will be as shown in the figure 2.

For a Te sampling steps the sampled signal $u(t)^2$ will known only at instants of sampling. Whereas the area between the time axis and the sampled signal $u(t)^2$ can be approximate the integral $\int_0^t u(t)^2.dt$.

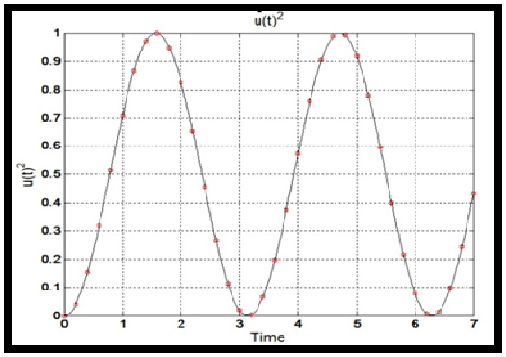


Fig. 2. $u(t)^2$ signal form

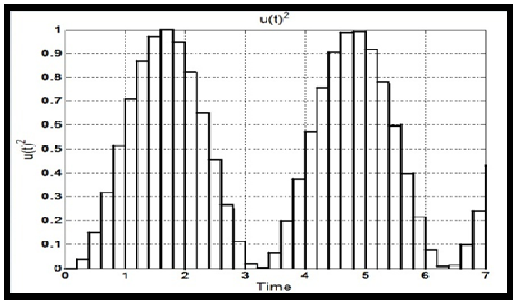


Fig. 3. The area of the discretized signal

For N samples: $\int_0^t u(t)^2.dt \cong \sum_{i=0}^{N-1} u_i^2 \times Te$ so:

$$RMS \cong \sqrt{\frac{1}{N \times Te} \sum_{i=0}^{N-1} u_i^2 \times Te}$$

$$\Rightarrow \quad RMS \cong \sqrt{\frac{1}{N} \sum_{i=0}^{N-1} u_i^2} \qquad (4)$$

In the FPGA hardware implementation, we employed several components to process the data. A counter was utilized to keep track of the number of patterns. For calculate the square of each (u_i^2) sampled signal we used one multiplier, and one accumulator was employed to accumulate these squared values. Finally, we multiplied the value stored in the accumulator by the inverse of the counter, and subsequently, the square root of this product was calculated to obtain the final result.

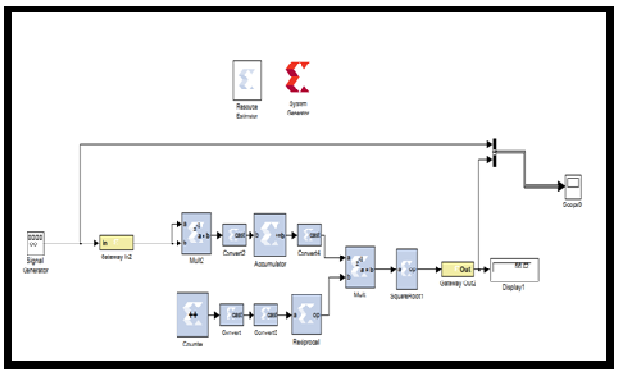


Fig.. 4. RMS function FPGA hardware architecture

IV. FUZZY INFERENCE SYSTEM IMPLEMENTATION ON FPGA

The hardware realization of a fuzzy inference system involves three phases: fuzzy inferences, defuzzification, and fuzzification.

A. Realization of fuzzification unit.

The memory-based approach was adopted in this research, for implementing the fuzzification unit. This approach enables us to assess the membership degree within a fuzzy set by employing a predefined membership function. The key feature of this method is that it precomputes and stores the output values in memory. One notable advantage of this approach is its facilitation of member ship function adjustments, simplifying the process significantly.

We make use a tables for store the membership degrees associated with each linguistic value to depict each input/output linguistic variable. These tables are integrated into the hardware design utilizing blocks of ROM memory, each of which is able to be accessed with a unique entrance. The grade of membership for every linguistic value is stored within these memory blocks; the discrete speech universe was represented by the index of these memory blocks. As an example, in the case of a normalized discourse universe spanning from 0 to 1 and discretized into 64 points, we would configure an address space ranging from 0 to 63 to cover the entire range of values.

B. Fuzzy inference and fuzzy evaluation realization

The figure depicting the realization of fuzzy inference and fuzzy evaluation block, as shown in Figure 5, receives the fuzzification three blocks as its entrances. The block selector of rules plays a crucial role in constructing the rule base, which comprises a total of 27 rules. This rule base is derived from the exploration of each combination possible among the fuzzy values associated with "RMS error."

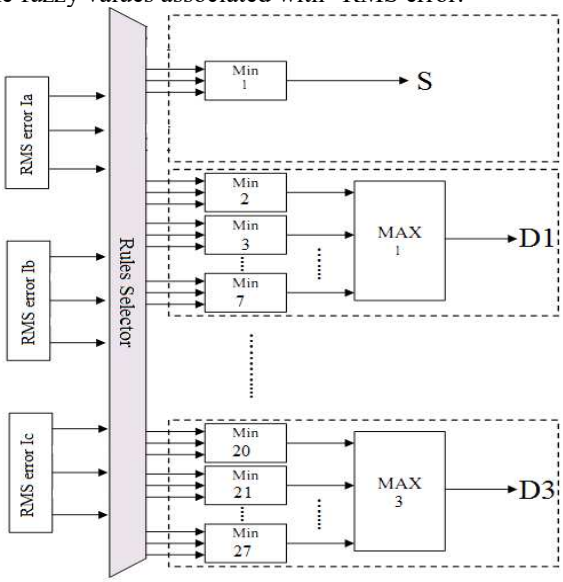


Fig. 5. Inference system Architecture

The Xilinx System Generator hardware tool implements the operators (max/min) by a comparator and a 2-1 multiplexer.

Multiple operators two-input (min/max) are used for a (max/ min) block with three or more entrances.

C. Realization of defuzzification block

MAX operator as depicted in figure 6 was used to describe the defuzzification component. The entrances to this unit are the outputs of the fuzzy inference component.

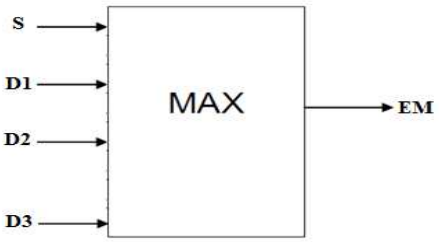


Fig. 6. Defuzzification block realization

V. PROPOSED ARCHITECTURE VALIDATION AND SIMULATIONS

This stage involves the incorporation of a fuzzy logic module into the algorithm MCSA for the identification of induction machine faults. In this phase, akin to the simulation MATLAB, we will replicate the suggested hardware design by utilizing for simulation the Xilinx system generator.

A. *Results of synthesis.*

The following table Illustrates the resource utilization metrics during the execution phase for the algorithm of diagnostic applied to the VIRTEX 4 FPGA, as defined by the hardware architecture depicted in Figure 1.

TABLE 1 FPGA CONSUMPTION FOR THE PROPOSED ALGORITHM OF DIAGNOSTIC

FPGA Device: ML402 Virtex-4				
Utilization	**RMS**	**Fuzzy system**	**Available**	**Utilization**
Slice Flip Flops	170	1304	30,720	4.8%
occupied Slices	422	1685	15,360	13.7%
LUTs 4 input	1286	2173	30,720	11.25%
IOBs	65	58	448	27.4%

The proposed architecture demonstrates an optimized utilization of the FPGA card's hardware resources, utilizing only 13.7% of LUTs and 4.8% of Slices. Additionally, this hardware significantly reduces the number of logical elements required compared to the architectures discussed in [11] and [13].

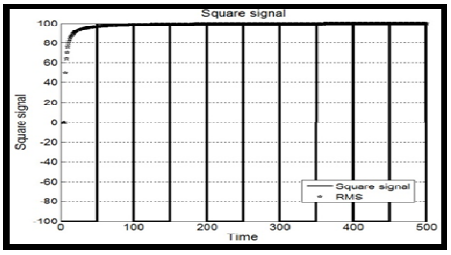
The maximum clock frequency was 231.64MHz established by the synthesis tool, equivalent to a minimal period of 4.317ns. Here is a table that provides an operating frequencies comparative analysis of across different references inside the similar research domain:

TABLE 2 COMPARISON OF OPERATING FREQUENCY

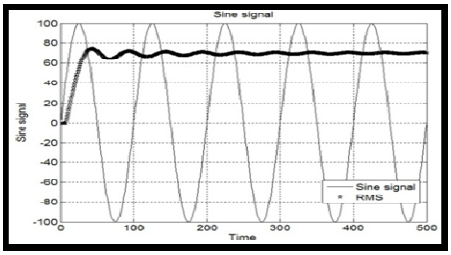
References	**[13]**	**[13]**	**[12]**	**Proposed Fuzzy MCSA**
device family	Intel Pentium Dual Core processor	FPGA Altera CYCLONE- II	FPGA Xilinx Spartan-3E	FPGA Xilinx Virtex-4
maximum clock frequency	2.95 KHz	45.45 KHz	92.1 MHz	231.64 MHz
minimum period	338 us	22 us	10.857 ns	4.317 ns

B. *Simulations by XSG/Xilinx in Matlab/Simulink.*

The design of the algorithm of diagnostic fuzzy MCSA depicted in Figure 1 comprises two primary modules. The first module is the RMS (Root Mean Square) component, which serves the purpose of computing the effective values for the three stator current phases. This resulting signal is employed as the indicator of defect, and it interfaces with the component of diagnostic, which operates on a fuzzy inference structure, these modules were simulated independently through Xilinx/ XSG in MATLAB/Simulink environment. The following figures present the simulation results for some types of input signals of the RMS module.



(a) Square signal



(b) Sine signal

Fig. 7. RMS function for square and sine signals

C. Validation on FPGA by co-simulation hardware.

Subsequent to the procedure of simulation, the proposed architecture hardware was confirmed through hardware Co-Simulation using the ML402 board tool, which is provided by a FPGA VIRTEX4 circuit.

The purpose of this step is to implement the proposed diagnostic algorithm on a board of development that incorporates a FPGA module. This step primarily aims to verify and validate the realization digital for the algorithms of diagnostic and command on FPGA card with "Hardware in the loop" environment of simulation.

The figure 8 illustrates the essential of validating the proposed method through Co-Simulation Hardware:

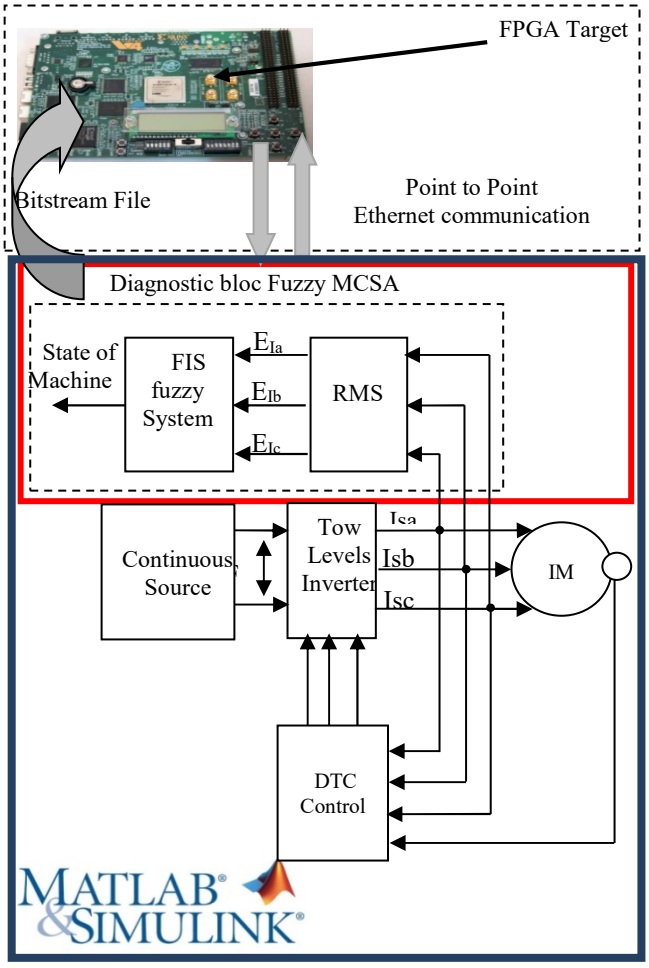


Fig. 8. Validation of fuzzy MCSA diagnostic algorithm by hardware in the loop process

After finishing the timing analysis and, simulation the co-simulation hardware procedure within XSG proceeds to execute a series of steps to create a bitstream file using a Point-to-Point Ethernet module and the hardware model. This action supports the (HIL) Hardware-In-the-Loop procedure. The newly generated module, as illustrated in Figure 9, substitutes the beforehand established hardware structure for the algorithm of diagnostic Fuzzy MCSA.

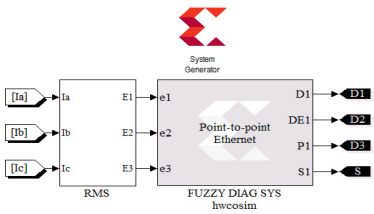


Fig. 9. Point to point Ethernet HIL block for Fuzzy MCSA algorithm

Throughout the Hardware-In-the-Loop corroboration procedure, the Ethernet Point-to-Point components are linked to both the induction machine and the inverter. In this arrangement, the DTC control, the inverter, and the machine models are validated inside the environment Matlab/Simulink, while the XSG structures of the algorithm of diagnostic Fuzzy MCSA are deployed on the device FPGA ML402. To conduct the validation by HIL, the PC is linked to the FPGA device with a cable of Ethernet. This enables a communication in real-time and interaction between the implementation hardware working on the ML402 FPGA tool and the models of simulation executing on the PC.

1. When addressing unbalance phase with 40% of Vsa at t=0.5s, the waveforms depicting the behaviors of the induction machine's torque, speed, and currents are displayed in the following figures:

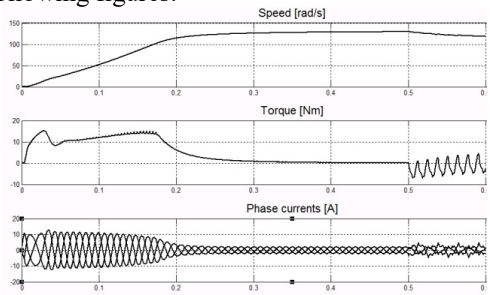


Fig. 10. Induction motor speed, phase currents and Torque

The presented figure, denoted as Figure 11, illustrates the outcomes of the examination performed by the algorithm of Fuzzy MSCA, which is designed to address the phase currents as shown in the previous figure.

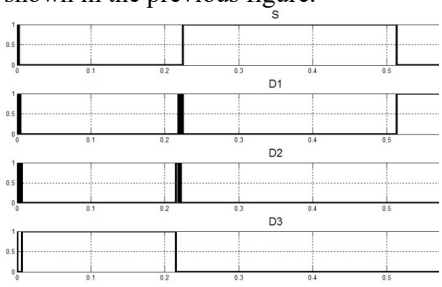


Fig. 11. Phase currents Fuzzy MSCA analysis

During the initial phase of machine start-up, which is considered the transient regime and spans beginning 0 to 0.2 seconds, all three phases of current exceed their nominal values. This deviation indicates the presence of a fault D3 within this interval of time.

In the interval of time between 0.2 and 0.5 seconds, the machine transitions into its steady-state or permanent

regime, and during this period, the three phases of current return to their nominal values. Consequently, the machine's condition is considered "Healthy" during this phase.

At the precise moment of 0.5 seconds, a fault manifests, leading to a transition in the machine's condition from "S" to "D1." Interestingly, the fault doesn't significantly impact the speed machine's dynamic response. This resilience is attributed to the robustness of the Direct Torque Control, which can effectively mitigate the effects of the fault on the machine's performance.

2. In the case of a phase missing, where Vsa becomes 0 at t=0.5s, the waveforms depicting the behaviors of the induction machine's torque, speed, and currents are displayed in the figures provided.

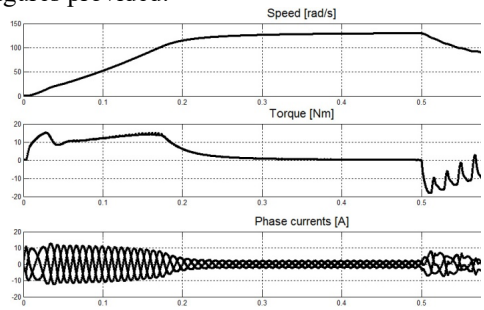


Fig. 12. Induction motor speed, phase currents and Torque

The figure labeled as Figure 13 displays the results obtained through the analysis performed by the Fuzzy MSCA algorithm, which is designed to address the phase currents as presented in the previous figures.

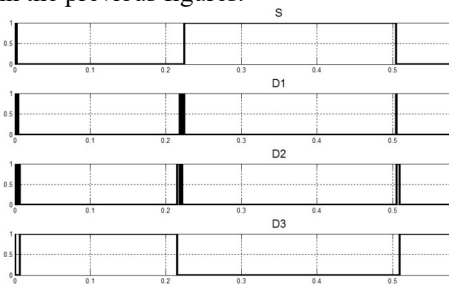


Fig. 13. Phase currents Fuzzy MSCA analysis

At the specific moment of 0.5 seconds, a fault emerges, resulting in a transition in the machine's condition from "S" to "D3." The fault absence of phase has a profound impact on the speed machine's dynamic response, primarily because it is a catastrophic fault, and its consequences are severe in nature.

VI. CONCLUSION

The primary objective of this study was twofold. First, it aimed to assess the effectiveness of employing FPGA logic programmable circuits for identifying defects in an induction machine. This was achieved by integrating a fuzzy inference structure into the analysis approach of stator current signals (MCSA), with the RMS (Root Mean Square) of the stator current of phase serving as the key indicator for detecting faults. Second, the study sought to develop and verify the functionality of the suggested hardware-based detection algorithm. The originality of our work lies in the integration of the techniques of artificial intelligence, the simplicity of the algorithms MCSA (stator current signal analysis), and the computational capabilities of the logic programmable circuits. This unique combination allows for the development of a defect diagnosis architecture for induction machines that achieves optimal ratios in terms of speed/performance and simplicity/performance. Furthermore, we believe that our proposed solution offers significant improvements in fault detection performance for asynchronous machines. This is particularly evident in the efficient utilization of hardware resources, high-speed detection, and online real-time detection capabilities.

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