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Commandes avancées d'un système de production décentralisée photovoltaïque à base de convertisseurs parallèles à quatre bras

Presented by

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I, AL-DWA Ala Addin Mohammed Mohammed Hussin, declare that this thesis is submitted in fulfillment of the requirements for the award of Doctor of Philosophy in the Faculty of Technology at the University of M'sila.

This thesis is wholly my own work unless otherwise referenced or acknowledged. In addition, I certify that all information sources and literature used are indicated in the thesis. I also certify that the work in this thesis has not previously been submitted for a degree, nor has it been submitted as part of the requirements for a degree except as fully acknowledged within the text.

This research is supported by the University Training Research Projects titled Commande intelligents d'un système de production décentralisé photovoltaique dans les réseau électriques qutre fils à base de convertisseurs qutre bras avec tolérence aux pannes under the matriculation A01L07UN280120220005/2022.

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Abstract :

In recent years, the integration of decentralized generation based on photovoltaic energy sources and static power converters has significantly increased, particularly in three-wire power networks. This trend supports the use of local energy resources near consumption points.

The photovoltaic-grid system is considered a promising solution to increase the share of renewable energy and enhance power quality within electrical networks. However, such systems are highly sensitive to variations in load or source parameters and power levels, which can impact their stability, synchronization, and energy quality. These technical challenges raise concerns about the reliability of decentralized generation systems.

This research primarily aims to explore various topologies and control strategies for decentralized photovoltaic-grid systems. These systems utilize interleaved DC-DC converters and four-leg inverters to inject power and improve power quality in four-wire electrical networks.

To enable the integration of high-power decentralized generation into four-wire networks, the study also investigates the use of multilevel converters and parallel configurations of static power converters.

A key focus is on selective control strategies for decentralized photovoltaic–grid systems and on addressing the issue of circulating currents in parallel converter structures. Solutions will be proposed to optimize the number of active converters based on the power requirements of the four-wire network.

To further enhance the performance of decentralized photovoltaic–grid systems, advanced control techniques will be introduced. These include adaptive nonlinear control, 3D Space Vector Pulse Width Modulation (3DSVPWM), and intelligent control strategies. These methods have demonstrated effectiveness in maintaining stability, ensuring synchronization, improving power quality, and dealing with parameter and power variations from loads or energy sources.

Keywords:

Photovoltaic system, Two-level four-leg inverter, Circulating current, Power quality, Advanced and intelligent control strategies.

الملخص:

شهدت السنوات الأخيرة تزايدًا ملحوظًا في دمج أنظمة التوليد اللامركزي المعتمدة على مصادر الطاقة الشمسية الكهروضوئية ومحولات القدرة الساكنة، خاصة في الشبكات الكهربائية ثلاثية الأسلاك، مما يتيح الاستفادة من الموارد المحلية القريبة من أماكن الاستهلاك.

تُعد أنظمة الربط بين الطاقة الشمسية والشبكة الكهربائية من البدائل الواعدة لزيادة نسبة الطاقة المتجددة وتحسين جودة الطاقة في الشبكات الكهربائية. ومع ذلك، فإن استقرار هذه الأنظمة وتزامنها وجودة الطاقة التي توفرها تتأثر بشكل كبير بتقلبات الأحمال أو مصادر الطاقة، مما يثير تحديات تقنية تتعلق بموثوقية أنظمة التوليد اللامركزي.

يركز هذا البحث على دراسة مختلف البنى الطوبولوجية واستراتيجيات التحكم لأنظمة التوليد اللامركزي الكهروضوئية المتصلة بالشبكة، والتي تعتمد على محولات DC-DC المتداخلة وعواكس رباعية الأذرع، بهدف تحسين جودة الطاقة وضخ القدرة في الشبكات الكهربائية رباعية الأسلاك.

ولدمج التوليد اللامركزي في الشبكات رباعية الأسلاك ذات القدرة العالية، يتناول البحث أيضًا استخدام المحولات متعددة المستويات، بالإضافة إلى البنى التي تعتمد على توصيل محولات القدرة الساكنة على التوازي.

سيتم تقديم استراتيجيات تحكم انتقائية لهذا النوع من الأنظمة، إلى جانب حلول لمشكلة التيارات الدوارة في البنى المتوازية للمحولات، بهدف تحسين عدد المحولات العاملة بناءً على متطلبات القدرة في الشبكة رباعية الأسلاك.

ولتطوير أداء هذه الأنظمة، سيتم تقديم تقنيات تحكم متقدمة مثل التحكم غير الخطي التكيفي، وتقنية تعديل عرض النبضة ثلاثية الأبعاد (3DSVPWM)، بالإضافة إلى تقنيات تحكم ذكية. وقد أثبتت هذه الطرق فعاليتها من حيث الاستقرار، والتزامن، وجودة الطاقة، وقدرتها على التعامل مع تقلبات الأحمال أو مصادر الطاقة.

الكلمات المفتاحية

النظام الكهروضوئي، العاكس رباعي الأذرع ثنائي المستوى، التيار الدوّار، جودة الطاقة، استراتيجيات التحكم المتقدمة والذكية.

Résumé :

Ces dernières années, l'intégration croissante de la production décentralisée basée sur des sources d'énergies photovoltaïqueet des convertisseurs statiques est en forte progressionpour les réseaux électriquesà trois filsqui permettent l'exploitation des ressources locales proches des lieux de consommation.

Le système photovoltaïque-réseau électrique est une des alternatives envisagées pour augmenter le taux d'énergie renouvelable et d'améliorer la qualité de l'énergiedans les réseaux électriques. La stabilité, la synchronisation et la qualité de l'énergie d'un système photovoltaïque-réseau électriqueest fortement sensible aux variations des paramètres et de puissance venant des charges ou des sources d'énergie.Toutefois, des contraintes techniques principalement liées à ces performances soulèvent des problèmes difficiles sur la fiabilité du système de production décentralisée.

Dans ce travail de recherche, l'objectif principal est d'aborder les différentes topologies et stratégies de commande des systèmes de productions décentraliséesphotovoltaïques-réseaux électriquesbasée sur des convertisseurs statiques de puissance DC-DC entrelaceset des onduleurs à quarte bras en vue d'injecter la puissance et d'améliorer la qualité de l'énergie dans les réseaux électriques à quatre fils.

Afin d'intégrée la production décentralisée dans les réseaux électriques à quatre fils de forte puissance, les systèmes de productions décentralisées photovoltaïques-réseaux électriques basée sur les convertisseurs multiniveaux et les structures mises en parallèle des convertisseurs statiques de puissance seront également abordées dans ce travail de recherche.

Une sélectivité dans la commande de ce type de système de production décentralisée photovoltaïque-réseaux électriqueet une solution pour le problème du courant de circulation dans les structures mises en parallèle des convertisseurs statiquesseront introduites, pour optimiser le nombre de convertisseurs statiques en service en fonction de la puissance de réseau électrique à quatre fils.

Pour améliorer les performances de ces systèmes de productions décentralisées photovoltaïques-réseaux électriques des techniques de commande avancéesseront introduites. Il s'agira de la commande non-linéaire adaptative, de la commande par 3DSVPW et d'autres commandes intelligentes. Ces commandes ont fait preuve d'efficacité du point de vue destabilité, synchronisation, qualité d'énergie et de la prise en compte du problème de la variation desparamètres et de puissance venant des charges ou des sources d'énergie.

Mots clés :

Système photovoltaïque,Onduleur à quarte bras à deux niveaux,Courant de circulation, Qualité d'énergie, Commandesavancées et intelligentes.

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Chapter 4: Active Disturbance Rejection Control method for PVG grid connected parallel four leg inverters system

LIST OF ABBREVIATIONS

Abbreviation	Full Form
ABC	Artificial Bee Colony
AC	Alternating Current
ACO	Ant Colony Optimization
ADRC	Active Disturbance Rejection Control
ANN	Artificial Neural Network
APF	Active Power Filter
AV	Active Vector
CCM	Continuous Conduction Mode
CIGS	Copper Indium Gallium Selenide
CS	Cuckoo Search
DC	Direct Current
DDBC	DC-DC Boost Converter
DDSRF-PLL	Decoupled Double Synchronous Reference Frame PLL
DG	Distributed Generation
DQ0	Direct-Quadrature-Zero (reference frame)
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
ESO	Extended State Observer
ESR	Equivalent Series Resistance
FFT	Fast Fourier Transform
FL	Fuzzy Logic
FOSM	First-Order Sliding Mode
FPGA	Field-Programmable Gate Array
GA	Genetic Algorithm
GaAs	Gallium Arsenide
GMPP	Global Maximum Power Point
GWO	Grey Wolf Optimizer
HOSM	High-Order Sliding Mode
IC	Incremental Conductance
ICPSO	Incremental Conductance based Particle Swarm Optimization
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
LADRC	Linear Active Disturbance Rejection Control
LC	Inductor-Capacitor (filter)
LFHC	Low-Frequency Harmonic Component
LPF	Low-Pass Filter
LTD	Lumped Total Disturbance

Abbreviation	Full Form
MIMO	Multi-Input Multi-Output
MPC	Model Predictive Control
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NREL	National Renewable Energy Laboratory
P&O	Perturb and Observe
PCC	Point of Common Coupling
PCE	Power Conversion Efficiency
PD	Phase Detector
PI	Proportional-Integral (controller)
PIQRC	PI-Quasi-Resonant Controller
PLL	Phase-Locked Loop
PN	P-type N-type (junction)
PSO	Particle Swarm Optimization
PV	Photovoltaic
PVG	Photovoltaic Generator
PWM	Pulse Width Modulation
RER	Renewable Energy Resource
RPLL	Robust PLL
RSPLLU	Robust Synchronization PLL Unit
SAPF	Shunt Active Power Filter
SAPSS	Standalone Active Power Supply System
SD	Single-Diode (model)
SEFC	State Error Feedback Controller
SMC	Sliding Mode Control
SOGI-PLL	Second-Order Generalized Integrator PLL
SPWM	Sinusoidal Pulse Width Modulation
SRF-PLL	Synchronous Reference Frame PLL
STC	Standard Test Conditions
STSMO	Super-Twisting Sliding Mode Observer
SVM	Space Vector Modulation
3D-SVM / 3DSVPWM	Three-Dimensional Space Vector Modulation / PWM
THD	Total Harmonic Distortion
TOSM	Third-Order Sliding Mode
VCO	Voltage-Controlled Oscillator
VOC	Voltage-Oriented Control
VSI	Voltage Source Inverter
ZS	Zero-Sequence

Abbreviation	Full Form
ZSC	Zero-Sequence Current
ZSCC	Zero-Sequence Circulating Current
ZSDR	Zero-Sequence Duty Ratio
ZSV	Zero-Sequence Voltage
ZV	Zero Vector
4LI	Four-Leg Inverter
αβ0	Alpha-Beta-Zero (reference frame)

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Publications and communications under this Phd Thesis

1- Al-Dwa, A. A. M., Chebabhi, A., Ziane, D., Barkat, S., Ihammouchen, S., Rekioua, T., Alhejji, A. Real-time implementation of a new modified 3DSVPWM control method for eliminating zero-sequence circulating current in parallel three-phase four-leg source voltage inverters. *IEEE Access*, *12*, 101121-101138, 2024

2- Chebabhi, A., Al-dwa, A. A. M., Defdaf, M., Kessal, A. New modeling and enhanced control strategy for grid-connected four-leg inverter without phase-locked loop and park's transformation. *Revue Roumaine des Sciences Techniques—Serie Électrotechnique et Énergétique*, *68*(2), 121-126, 2023.

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General Introduction

Conventional energy sources such as coal, oil, peat, and natural gas continue to play a strategic role in electricity generation. However, the global energy demand is rising rapidly by approximately 4% annually posing a significant challenge for the near future. This trend points toward a looming global energy shortage, further exacerbated by the steady depletion of fossil fuel reserves, which poses a serious risk for future generations [1–3]. Moreover, the extraction and use of these conventional energy sources contribute heavily to environmental degradation, particularly through greenhouse gas emissions. In response to growing climate concerns, international efforts such as the Kyoto Protocol (1997), the Durban Conference (2001), the Bali Action Plan (2007), and the Cancun Agreements (2010) have laid the groundwork for limiting the use of fossil fuels [1, 4]. As a result, the global focus has increasingly shifted toward clean, renewable, and non-polluting sources of energy. These alternatives are now seen not only as environmentally necessary but also as critical for long-term energy security and sustainability [5].

Decentralized renewable energy production, particularly photovoltaic (PV) systems, has emerged as a leading solution to address growing energy demands, fossil fuel depletion, and environmental concerns. PV energy is especially promising due to its clean and silent operation. However, the unpredictable nature of sunlight necessitates the use of power electronics to effectively harness this energy and meet grid connection requirements. A typical grid-connected PV system comprises two conversion stages [6]. The first stage uses a DC-DC converter, often a boost converter, to maximize power output from the PV generator and increase voltage for the DC bus. The second stage employs a DC-AC voltage inverter to inject energy into the grid while meeting connection standards.

Although conventional PV systems commonly employ three-phase, three-leg voltage source inverters due to their simplicity, cost-effectiveness, and ease of control, this topology presents several significant limitations. Designed primarily for balanced three-wire systems, the three-leg VSI lacks a dedicated neutral conductor, which restricts its ability to supply single-phase loads and handle unbalanced or nonlinear conditions that are the scenarios frequently encountered in standalone and distributed energy systems [7, 8]. Additionally, these inverters exhibit limited performance in mitigating common-mode voltage and harmonic distortion, leading to compromised power quality and accelerated aging of connected equipment. Their voltage regulation also suffers under dynamic

load variations, and they offer limited scalability for medium- and high-power applications when compared to more advanced inverter architectures [9].

To address these challenges, researchers have proposed enhanced inverter topologies and control strategies, among which the four-leg inverter has emerged as a highly effective solution. By incorporating an additional leg, this topology provides a dedicated path for neutral current, allowing stable and efficient operation under unbalanced loading conditions and enabling the simultaneous supply of single-phase and three-phase loads. The four-leg design also enhances voltage regulation, minimizes neutral point fluctuations, and supports independent control of each phase voltage, which is particularly beneficial in low-voltage distribution networks with prevalent single-phase residential and commercial loads [10, 11].

Compared to three-leg inverters, four-leg converters significantly improve neutral current handling by eliminating the reliance on split DC-link capacitors, which are prone to voltage imbalance. Recent developments have also explored series and parallel combinations of four-leg inverters to increase current capacity, improve modularity, and enhance system reliability [12]. However, these advanced configurations introduce new technical challenges, such as voltage balancing in series-connected modules and circulating currents in parallel setups. Despite these complexities, four-leg DC-AC converters continue to gain traction for grid-interfacing applications, offering superior power quality, better control of individual phase voltages and currents, and reduced total harmonic distortion (THD), especially under unbalanced or nonlinear load conditions [13].

Another significant benefit of four-leg converters is their flexibility. The independent control of the neutral point voltage allows for various grounding schemes and simplifies the integration of both single-phase and three-phase loads within the same system [14]. This flexibility is particularly valuable in decentralized power systems where load characteristics can vary widely. Additionally, four-leg converters can operate with smaller DC-link capacitors compared to three-leg topologies, which typically require larger capacitors to manage neutral current. This reduction in capacitance can result in cost and space savings for the overall system [15].

From a reliability perspective, the fourth leg introduces a level of redundancy, increasing fault tolerance. This redundancy allows the system to continue operating under certain fault conditions, thereby enhancing overall system reliability. Moreover, four-leg converters can achieve higher AC voltage output for a given DC-link voltage, improving system efficiency. This is especially important in renewable energy systems, where maximizing energy yield is a key priority [16].

In grid-connected photovoltaic (PV) systems, a single four-leg inverter is often employed due to its ability to supply both balanced and unbalanced loads, making it especially suitable for low-voltage distribution networks. However, despite this versatility, using a single four-leg inverter poses several limitations, particularly in medium- and high-power applications [2]. One of the main challenges is its restricted power capacity, limited by the current and voltage ratings of individual components. As the power demand increases, thermal stress on the inverter intensifies, potentially reducing both its efficiency and operational lifespan. Additionally, the centralized design introduces a single point of failure; a fault in the inverter can result in the total shutdown of the system. Maintenance in such setups is also more complex and often requires full system downtime. Furthermore, the lack of modularity limits scalability and flexibility, making system expansion difficult without significant redesign [17, 20].

To address these challenges, the parallel connection of multiple four-leg inverters sharing a common DC bus has emerged as a promising solution. In this architecture, several inverters operate in parallel on the AC side while drawing power from the same DC link. This modular design increases the overall power capacity by allowing additional inverter modules to be integrated as needed. It also enhances system reliability; if one unit fails, the remaining inverters can continue operation, ensuring uninterrupted power supply. Maintenance is simplified, as faulty units can be serviced or replaced independently without affecting the entire system. Moreover, the power and thermal stresses can be distributed more evenly across all inverter modules, leading to better efficiency, improved performance, and extended component lifespan [21-23].

This architecture is particularly advantageous in large-scale PV installations and microgrid applications, where modularity, redundancy, and flexibility are critical. Examples include rural microgrids powering residential and agricultural equipment, industrial parks with mixed single- and three-phase loads, and commercial campuses with dynamic load profiles. In such contexts, the ability to independently regulate each phase and maintain stable operation under unbalanced loading conditions is crucial. In mission-critical environments such as hospitals, data centres, and telecom infrastructure powered by solar energy, the redundancy offered by parallel four leg inverters-based PV grid connected systems ensures high availability and system resilience.

Despite its advantages, the parallel operation of four-leg inverters introduces specific technical challenges that must be addressed to ensure stable and efficient performance. A major concern is the emergence of circulating currents between four leg inverter modules, often caused by mismatches in output voltage magnitudes, phase angles, or output filter inductances. These mismatches can result in unequal voltage drops and phase shifts, promoting the flow of undesired inter-module currents. Furthermore, imbalances in filter parameters and unequal current sharing between inverters when some units may be overloaded while others are underutilized can also results circulating currents between four leg inverter modules. These circulating currents can cause significant issues, including waveform distortion, reduced overall system efficiency, increased conduction and switching losses, localized component overheating, and accelerated aging of power semiconductors [24-27]. In severe cases, these circulating currents can generate electromagnetic interference (EMI) and harmonic distortion, degrading power quality and potentially disrupting sensitive electronic equipment.

To mitigate these problems, various control strategies have been proposed. While many studies have examined circulating current suppression in parallel three-leg inverter systems, there is comparatively limited research on circulating current mitigations in parallel-connected four-leg inverter architectures. These topologies, which share both common DC and AC bus connections, are particularly useful in controlling zero-sequence currents and minimizing voltage fluctuations at the point of common coupling (PCC). However, their complex interactions demand carefully designed control schemes to ensure stable parallel operation and high-quality power delivery.

This thesis explores the parallel operation of multiple four-leg inverters sharing a common DC bus in decentralized PV systems. The focus is on applications involving harmonic compensation and reactive power support under nonlinear single-phase loads and linear load conditions. The proposed system architecture surpasses the power limitations of single four-leg inverter configurations while enhancing efficiency, reliability, and flexibility. A core contribution of this work is the development of a coordinated control strategy specifically designed to suppress circulating currents resulting from imbalances in filter parameters and unequal current sharing among the inverters. This strategy ensures

stable system performance, balanced power distribution, and improved output power quality. By effectively eliminating circulating currents, the proposed system achieves superior scalability, reduced waveform distortion and current asymmetry, enhanced efficiency, minimized conduction and switching losses, lower component temperatures, and decreased EMI, ultimately increasing the robustness and lifespan of the PV power conversion system.

The first chapter of this thesis focuses on the modeling and linear control of a standalone power supply system based on a PV generator (PVG) coupled with a DC-DC boost converter. The chapter begins with an introduction to semiconductor fundamentals, followed by a detailed explanation of the operating principles and classifications of PV cells. In the second section, the structural configurations and mathematical models of PV modules are discussed, covering both single-diode and two-diode models. This section also includes an analysis of PV cell characteristics and the different series and parallel connection types. The third section of this chapter presents the current and voltage models of the PV module, along with a detailed description of the electrical characteristics of the module. The fourth section extends this modeling to the PVG under investigation as a whole, providing a comprehensive representation of its voltage and current behavior. The fifth section focuses on the control aspects of the PVG when operating in standalone mode in conjunction with a DC-DC boost converter. It begins by outlining the fundamental operating principle of the boost converter and proceeds to the determination and sizing of its input and output passive components, which are essential for ensuring proper energy transfer and system stability. The section also presents the detailed modeling of the converter, capturing its dynamic behavior in terms of input voltage and current. Based on these dynamics, proportional-integral (PI) controllers are then developed to regulate both the input voltage and current of the boost converter, ensuring accurate and stable operation under varying irradiance and temperature conditions.

The second chapter presents the integration of a four-leg inverter topology within a grid-connected PVG system. The chapter begins with an overview of the benefits of employing a four-leg inverter in a PVG grid-connected system. The second section explains the operating principle and modeling of the four-leg inverter in three-dimensional space. Section three provides a comprehensive mathematical model of the grid-connected four-leg inverter, focusing on its dynamic behaviors. This includes the dynamics of both the DC-side input voltage and the AC-side output currents, as well as the relationship between both sides of the inverter. Followed by the design and sizing of its critical components, such as the DC input capacitor and the output inductive filter, which are vital for energy transfer efficiency and overall system stability.

Given that the PVG grid-connected four-leg inverter system is capable of operating in two distinct modes, combined reactive power compensation and harmonic mitigation mode under nonlinear single-phase loads, and only reactive power compensation mode under three-phase linear loads, the chapter introduces a Dual-Loop Voltage Vector Control (DL-VVC) strategy. This control method is tailored to enhance system stability and improve power quality across both modes.

Key control features discussed include:

- Synchronization method using a robust and simplified phase-locked loop (RSPLL),
- DC bus voltage regulation via a PI controller,
- Generation of four leg inverter output current references based on instantaneous reactive power theory,

- Output current regulation and decoupling through PI controllers,
- Pulse-width modulation (PWM) signal generation using Three-Dimensional Space Vector Modulation (3D-SVM).

Simulation studies are conducted in this chapter using MATLAB/Simulink to evaluate system performance in both operational modes. The results demonstrate the effectiveness of the proposed configuration in balancing system active and reactive powers, mitigating harmonics, compensating reactive power, and improving grid current quality under varying irradiance, temperature, and load conditions for both nonlinear single-phase and linear three-phase scenarios.

Chapter 3 presents the original contributions related to the control and elimination of circulating currents in grid-connected PVG systems employing parallel-connected four-leg inverters. The chapter begins with an introduction that outlines the challenges posed by circulating currents in such systems and the need for effective mitigation strategies. A detailed state-of-the-art review follows, summarizing existing circulating currents elimination techniques and highlighting the gap in the literature concerning parallel four-leg inverter systems. The system topology and modeling are then presented, including an equivalent circuit representation of two parallel four-leg inverters in both the abc and dq0 reference frames. The output current dynamics of the parallel system are analyzed to understand the behavior of circulating currents under mismatched output filter inductances and uneven output current's sharing. A dedicated section models the circulating current characteristics and establishes the basis for subsequent control strategies. Two circulating current mitigation approaches are adopted: the first uses an adjusted SPWM modulation strategy, where the reference modulation voltages of one four leg inverter are modified using a PI regulator based on current mitigation feedback to reduce circulating currents; the second introduces a novel method involving adjusted zero-vector duty ratios in the 3D Space Vector PWM (3D-SVPWM) technique. This method specifically addresses the difference in zero-sequence voltages between the four leg inverters using adjusted control variable that governs the zero-vector duty ratio difference using PI regulator to dynamically minimize circulating currents and further improving current balancing between parallel four leg inverters. The chapter concludes with control strategy of the parallel-connected four-leg inverters-based grid-connected PVG system under linear load for reactive power compensation using the adjusted SPWM and 3D-SVPWM techniques. Simulation results demonstrate the effectiveness of the parallel-connected four-leg inverters-based grid-connected PVG system with adjusted 3D-SVPWM technique in power balance, reactive power compensation, grid current improvement, circulating current eliminations, proper current sharing, and improved output currents quality, especially under conditions of mismatched output inductances and unequal output current sharing.

Chapter 4 addresses the critical challenge of achieving robust and high-performance control of parallel four-leg inverter-based PVG grid-connected systems under parametric uncertainties and external disturbances. While the control strategies presented in the previous chapters demonstrate acceptable performance under nominal conditions, their effectiveness can deteriorate significantly when confronted with modeling inaccuracies, DC bus capacitor and output filter parameter variations, irradiance and temperature fluctuations, grid voltage disturbances, and measurement noise. To overcome these limitations, this chapter proposes an Active Disturbance Rejection Control (ADRC) method that provides a systematic framework for real-time disturbance estimation and compensation without requiring an exact mathematical model of the system. The chapter begins by formulating comprehensive uncertainty dynamics for both the DC bus voltage and parallel four-leg inverters'

output currents, accounting for parametric uncertainties, external disturbances, coupling effects, and grid voltage fluctuations. These uncertainties are consolidated into lumped total disturbances that are treated systematically by the ADRC approach. A dual-loop ADRC-based control architecture is then designed, featuring Extended State Observers (ESO) for online disturbance estimation in both the outer DC bus voltage control loop and the inner output current control loops in the dq0 reference frame, combined with State Error Feedback Controllers (SEFC) for voltage and current regulation. Detailed parameter tuning guidelines based on Hurwitz stability criteria and bandwidth selection principles are provided to ensure optimal performance, fast dynamic response, and noise immunity. The proposed ADRC method is integrated with the adjusted 3D-SVPWM technique developed in Chapter 3 to simultaneously achieve DC bus voltage stability, accurate output current tracking, circulating current suppression, proper load sharing among parallel inverters, and reactive power compensation under linear inductive loads. Comprehensive simulation studies validate the superior disturbance rejection capability, robustness against parametric uncertainties, and enhanced control performance of the ADRC-based parallel four-leg inverter system compared to conventional PI-based control approaches, particularly under severe operating conditions involving output filter inductance mismatches, irradiance variations, and grid voltage disturbances.

Finally, a general Conclusions synthesize the key findings, contributions, and outcomes of this doctoral research work. This final section provides a comprehensive summary of the theoretical developments, modeling approaches, control strategies, and simulation results presented throughout the thesis. It highlights the main contributions achieved in each chapter, including the successful modeling and control of the standalone PVG system with DC-DC boost converter, the development and validation of the four-leg inverter-based grid-connected PV system with dual operational modes (harmonic mitigation combined with reactive power compensation under nonlinear single-phase loads, and reactive power compensation under linear three-phase loads), the original contribution of circulating current suppression techniques through adjusted SPWM and novel adjusted 3D-SVPWM methods for parallel four-leg inverter configurations, and the advanced ADRC-based robust control framework that ensures superior performance under parametric uncertainties and external disturbances. The conclusions emphasize how the proposed parallel four-leg inverter architecture with coordinated control strategies successfully addresses the power capacity limitations, reliability concerns, and scalability challenges inherent in single four-leg inverter systems, while maintaining excellent power quality, proper load sharing, and effective circulating current elimination. The chapter also critically evaluates the practical implications of the research findings for large-scale PV installations, microgrids, and mission-critical applications. Finally, it identifies the limitations of the current work and outlines promising directions for future research, including experimental validation of the proposed control strategies, extension to islanded operation modes, integration of energy storage systems, implementation of hardware-in-the-loop testing, investigation of fault-tolerant control strategies, and exploration of artificial intelligence-based optimization techniques for enhanced system performance and adaptability in real-world grid-connected renewable energy applications.

Chapter 1

Overview of PV Systems for Grid-Connected Application and Power Quality Improvement

I.1. Introduction

The rise in global energy consumption presents significant concerns over the issue of global warming caused by greenhouse gas emissions and the degradation of fossil fuel reserves. In the context of this notice, it is essential to focus on economic growth that respects sustainability principles. The modern generation of power systems emphasizes the importance of using abundant, cost-effective, and clean energy resources called “renewable energy resources” (RERs) to produce environmentally friendly energy. Among the numerous forms of renewable energies, solar energy is receiving extensive attention due to its benefits, such as sustainability, availability, and free pollution [1]. The amount of solar energy that falls on the Earth is rated at about 175 petawatts (175×10^{12} KW) [2].

Over the past few years, many distributed generation (DG) systems have been integrated into the electrical grid, mainly aimed at boosting renewable energy production. From the various forms of energy, solar power integration refers to establishing a network that incorporates the sun's electricity into the utility grid. The integration of solar systems into grids is a significant technological advancement. It plays a crucial role in optimizing the energy balance of buildings, enhancing the economy, minimizing operating expenses, and offering additional benefits to consumers and utility providers. A grid-connected photovoltaic system harnesses solar energy using photovoltaic (PV) panels, connects to the utility grid, benefits from energy exchange, and enhances grid stability, promoting sustainable and reliable renewable energy integration [3-5].

I.2. Overview of Semiconductors

I.2.1. Structure of a PN Diode

When a semiconductor material doped with type N impurities (electron-rich) is brought into close contact with a type P doped semiconductor (electron-deficient), a PN junction is formed. At this interface, significant changes occur. Electrons from the N region diffuse into the P region, creating a positively charged area near the junction on the N side due to the loss of electrons [6, 7].

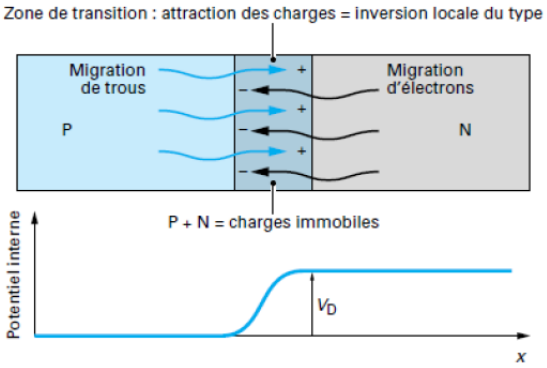


Figure I.1: Formation of the Transition Region in a PN Junction

Conversely, the P region develops a negatively charged zone because of the influx of electrons, as shown in Figure I.1. At equilibrium, an electric field is established across the junction, directed from the P side to the N side, resulting in a built-in potential, denoted as V_D. This electric field plays a crucial role in the operation of solar cells.

I.2.2. I-V Characteristics of the PN Diode

In a semiconductor, mobile electrons originate from the N region (majority carriers) and the P region (minority carriers). To study their behavior, a variable DC voltage V can be applied across the diode in darkness, with the circuit closed through a resistor.

When a forward voltage (positive V) is applied, it reduces the built-in potential barrier, allowing majority carriers to cross the depletion region, resulting in a current I_D from P to N. This current increases with both applied voltage and junction temperature.

In contrast, a reverse voltage (negative V) increases the potential barrier, allowing only minority carriers to contribute to a small current I_0 flowing from N to P. This reverse current also rises with temperature. If the reverse voltage is too high, the junction may break down due to avalanche effects, potentially damaging the diode.

I.2.3. Light Absorption

For an electron in the valence band (bound to its atom) to become free and move to the conduction band under an electric field, it must absorb a minimum amount of energy. This energy can come from photon absorption or thermal excitation. While photons across the solar spectrum may be absorbed, not all of them provide sufficient energy to promote electrons to the conduction band.

In silicon, only photons with wavelengths shorter than 1.1 μm are effective for this purpose. Longer wavelengths mainly contribute to heating the material.

I.2.4. Electron-Hole Pairs

Only electron-hole pairs generated within or near the depletion region can be effectively separated by the internal electric field and contribute to an electrical current. This current, known as the photocurrent and denoted I_{ph} [8], flows from the N region to the P region and is directly proportional to the incident light intensity, as shown in Figure I.2.

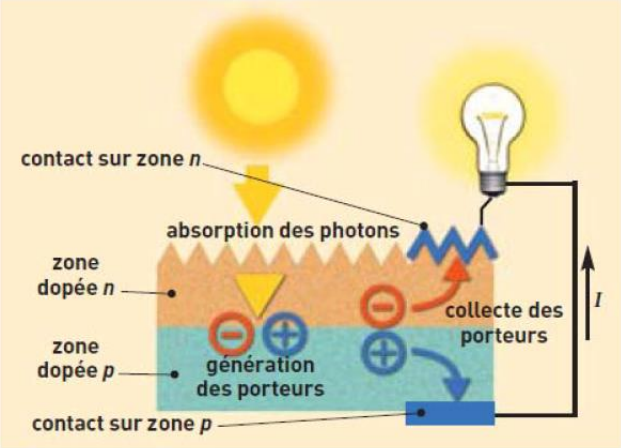


Figure I.2: Light Absorption and Energy Transfer from Photons to Electrons

I.3. Photovoltaic Cells

A photovoltaic cell is essentially a PN junction formed within a silicon substrate. The silicon is doped with elements like boron to create a P-type base and counter-doped with phosphorus on the surface to form an N-type layer. The internal electric field at this junction separates the photo-generated electron-hole pairs, allowing electrons to move toward the cathode and holes toward the anode. Under standard illumination of 1 kW/m², each square centimetre of the cell can produce a voltage around 0.5 V and a current of about 30 mA.

The structure of a solar cell resembles that of a PN diode, and the diode current in darkness is given by the following expression [6]:

$$I_d(V) = I_0(e^{\frac{qV}{nkT}} - 1) \tag{I.1}$$

where

- q: Elementary charge (1.6×10^{-19} C)
- k: Boltzmann constant (1.381×10^{-23} J/K)
- T: Effective temperature of the cell in kelvin
- I_0: Reverse saturation current of the junction, which has two main components:
  - Diffusion current due to minority carriers (electrons in the P region and holes in the N region reaching the depletion zone)
  - Thermally generated current from electron-hole pairs created in the depletion region
- n: Ideality factor (ranging between 1 and 2), accounting for the mechanisms of recombination:
  - n=1 for recombination in the neutral regions (N and P)
  - n=2 for recombination within the depletion zone

Among the possible approaches for harvesting solar energy is the PV process, which involves converting solar radiation into electrical energy. PV energy is a sustainable and environmentally friendly source that does not deplete natural resources. Renewable energy is critical for effectively meeting the world's growing energy demands while mitigating greenhouse gas emissions and reducing pollution.

I.3.1. The PV Cell Working Principle [9]

A PV cell is the fundamental component of a solar energy generation system, directly converting solar radiation into electrical energy without involving a mechanical engine. PV cells are composed of P-N junctions. The presence of negatively charged electrons contributed by impurity elements functioning as donors can be recognized by the term "*n*-type." On the contrary, the designation p-type signifies the presence of positively charged holes generated by acceptor impurity atoms. Stacking an n-type semiconductor layer on top of a *p*-type semiconductor layer forms a PV cell. In addition, a third area, known as a junction, forms between the two surfaces. Eventually, the electric field generated across the junction by the dispersed charges on the surfaces of the n and p-type materials stops the diffusion process. Considering the structure of the photovoltaic cell, light acts as an external energy source to generate an electric current. This description is in accordance with the PV structure depicted in Figure I.3.

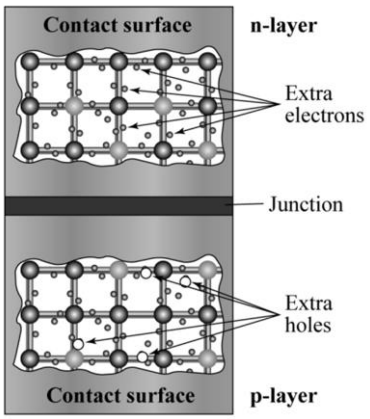


Figure I.3: Photovoltaic cell's P-N junction and N- and P-

I.3.2. Type of PV Cell

A. **Silicon crystalline:** The first generation of solar PV cells comprises crystalline-silicon-based cells, including monocrystalline (m-crystalline) and polycrystalline (p-crystalline) variants (Figure I.4). The brand name given to photovoltaic cells that consist of crystalline silicon derives from their manufacturing process [10]. The monocrystalline cell is widely utilized, with over 80% of the market, and is expected to maintain its dominance until the development of a more efficient and economically competitive photovoltaic technology [11].

(a) **(b)**

Figure I.4: Silicon crystalline PV module: monocrystalline (a), polycrystalline (b)

B. Thin-film: The second generation is Thin-film solar cells, shown in Figure I.5Figure I.5:, which are more cost-effective because they require fewer components and a simpler production process than their crystalline silicon counterparts [12]. The solar cell manufactured using this method is very thin (range of 35 to 260 nm) due to the reduced amount of material used. The main approaches of thin-film technology of PV cells are:

- Amorphous Silicon (a-Si).
- Cadmium Telluride (CdTe).
- Gallium Arsenide (GaAs).
- Copper Indium Gallium Selenide (CIGS).

C. Emerging technologies: Researchers are investigating third-generation photovoltaic technologies as an alternative to silicon solar cells. Third-generation solar cells (such as tandem cells, emerging concepts, dye-sensitized cells, perovskites, shown in Figure I.6, and organic cells) take a wide variety of approaches, ranging from economic low-efficiency systems (such as organic solar cells) to costly high-efficiency systems (such as III-V multi-junction cells) with uses varying from building integration to space exploration [13-15].

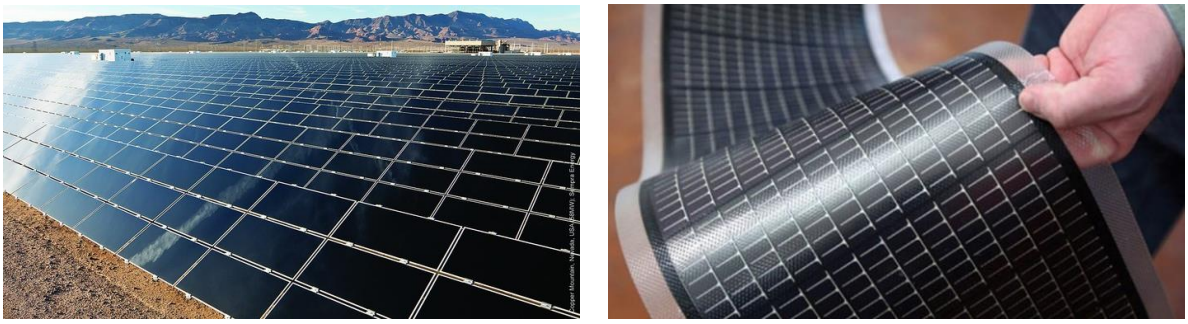


Figure I.5: Thin-film PV module

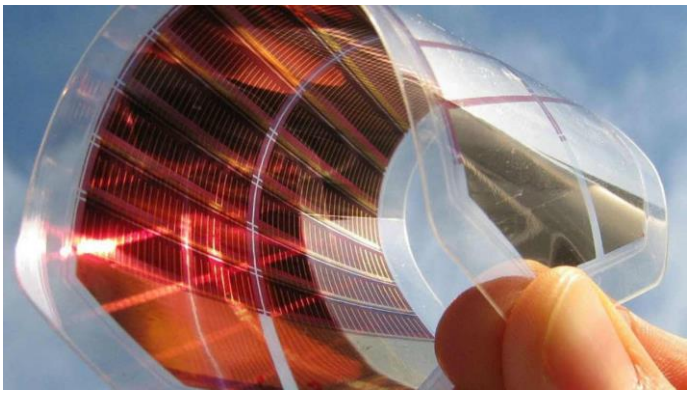


Figure I.6: Perovskites PV solar cell

As depicted in Figure I.7, the power conversion efficiencies (PCEs) of emerging photovoltaic technologies have increased significantly in recent years due to the increased scientific interest in their development.

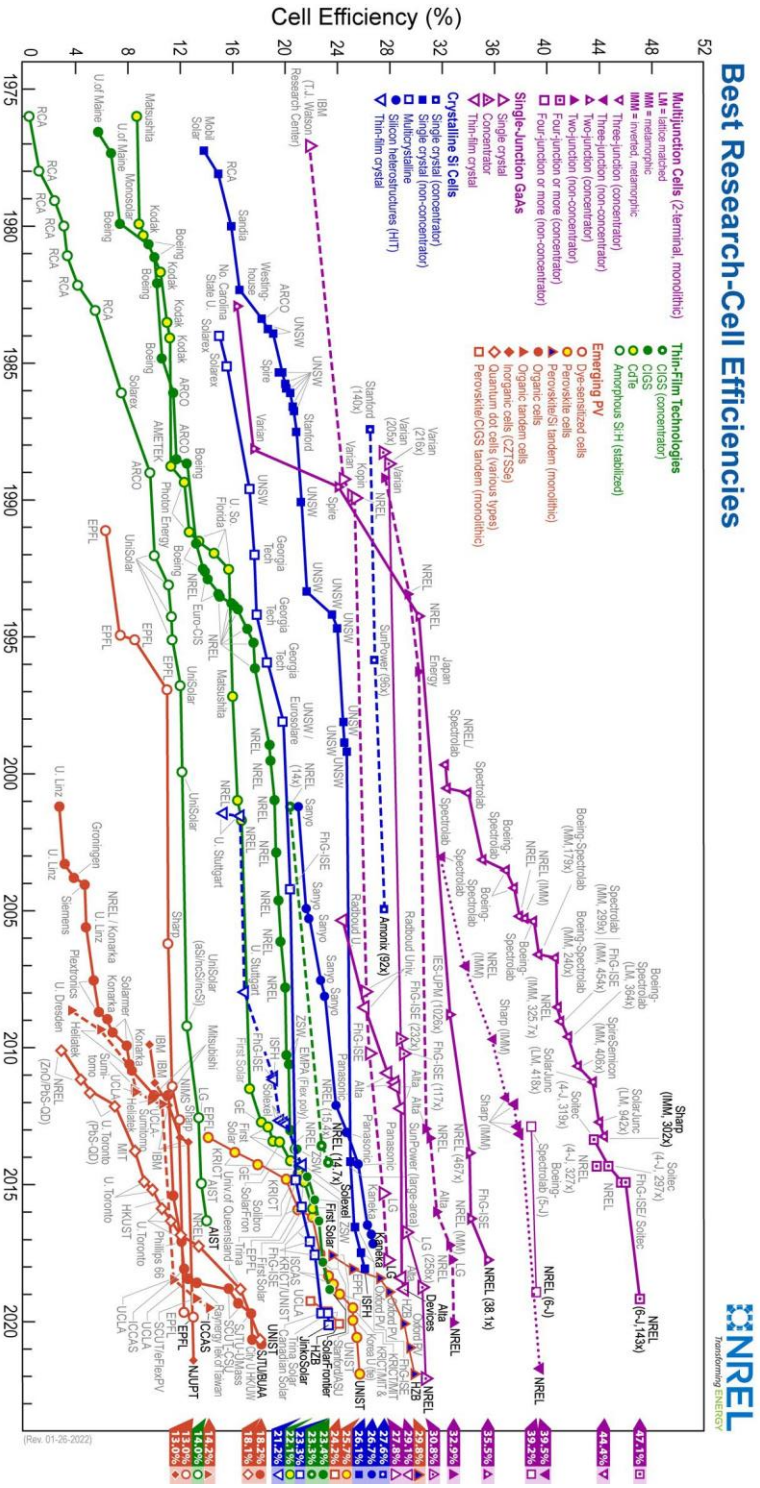


Figure I.7: Chart of best research-cell efficiencies from 1976 to 2022 provided by NRLE [16]

I.3.3. Mathematical Modeling of PV Module

A solar cell can be modeled in various ways in the literature, with each model defined by a mathematical relationship between current and voltage based on the cell's technological parameters. To simulate the nonlinear I-V characteristics of solar PV modules under various operating conditions (irradiance and temperature), numerous equivalent circuits have been presented in the literature [17–22].

I.3.3.1. Two-Diode Model

The equivalent circuit for the two-diode model is shown in Figure I.8. This model closely reflects the actual behavior of a solar cell because it incorporates the mechanisms of charge transport within the cell using two diodes. One exponential term represents the diffusion process, while the second accounts for recombination phenomena occurring in the depletion region [6], [23, 24].

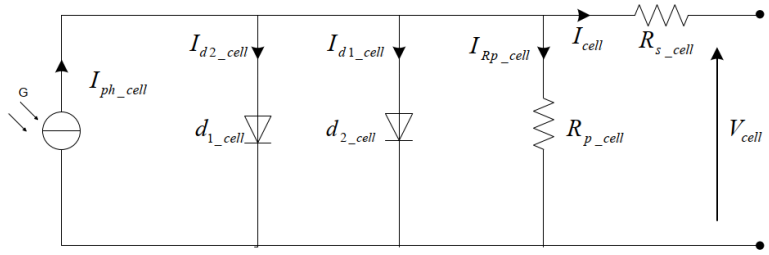


Figure I.8: Equivalent Circuit of the Two-Diode Model for a Photovoltaic Cell

- **Current Source**: This delivers the photocurrent I_{ph_cell}, which corresponds to the light-generated current within the cell.
- **Series Resistance R_{s_cell}**: Represents the internal resistive losses due to electrical contacts within different parts of the cell, specifically the emitter, base, and metallic contacts.
- **Shunt Resistance R_{p_cell}**: Also known as parallel or leakage resistance, this reflects the presence of electrical shunts across the emitter.
- **Diode d_{1_cell}**: Models the diffusion of charge carriers in the emitter and base regions. Its effect becomes more pronounced when the material has a high diffusion length.
- **Diode d_{2_cell}**: Accounts for the generation and recombination of carriers within the depletion zone [25].

By applying Kirchhoff's current law to the equivalent circuit shown in Figure I.8, the mathematical model describing the photovoltaic cell can be derived. The output current of the cell is given by:

$$I_{cell} = I_{ph\_cell} - I_{d1\_cell} - I_{d2\_cell} - I_{Rp\_cell} \tag{I.2}$$

whare

$$\begin{cases} I_{d1\_cell} = I_{01}\left(e^{\frac{V_{cell}+R_{s\_cell}I_{cell}}{n_1 kT/q}} - 1\right) \\ I_{d2\_cell} = I_{02}\left(e^{\frac{V_{cell}+R_{s\_cell}I_{cell}}{n_2 kT/q}} - 1\right) \\ I_{Rp\_cell} = \dfrac{V_{cell}+R_{s\_cell}I_{cell}}{R_{p\_cell}} \end{cases} \tag{I.3}$$

The current within the photovoltaic cell is therefore modelled by the following equation:

$$I_{cell} = I_{ph\_cell} - I_{01}\left[e^{\frac{V_{cell}+R_{s\_cell}I_{cell}}{n_1 kT/q}} - 1\right] - I_{02}\left[e^{\frac{V_{cell}+R_{s\_cell}I_{cell}}{n_2 kT/q}} - 1\right] - \frac{V_{cell}+R_{s\_cell}I_{cell}}{R_{p\_cell}} \tag{I.4}$$

where I_{cell} current delivered by the photovoltaic cell, I_{01} the reverse saturation current of diode d_{1_cell}, and I_{02} the reverse saturation current of diode d_{2_cell}.

I.3.3.2. Single-Diode Model

The single-diode (SD) model is commonly used to simulate the characteristics of solar modules. The SD model consists of several electrical components, as Figure I.9 illustrates. The photo-generated current I_{ph}, which depends on temperature and solar radiation, is modeled as a current source. Furthermore, to simulate the semiconductor P-N junction, researchers employ an ideal diode connected in parallel with the current source. In addition, series and parallel resistors represent the internal cell resistance and the diode leakage current [6].

It is possible to combine diodes d_{1_cell} and d_{2_cell} from the two-diode model into a single equivalent diode, d_{cell}. By selecting an ideality factor n between n_1 and n_2, the resulting configuration corresponds to the one-diode model shown in Figure I.9 [6].

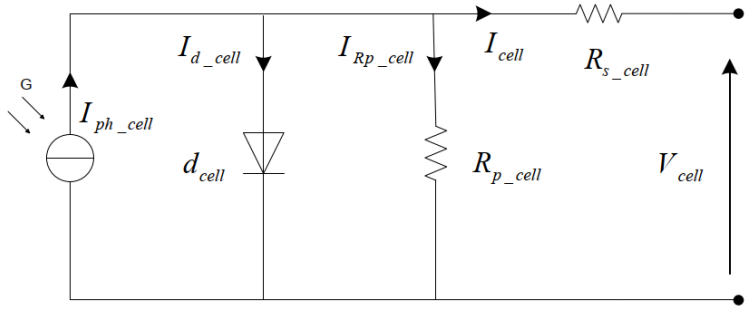


Figure I.9: Equivalent Circuit of the Single-Diode Model for a Photovoltaic Cell

According to the Equivalent Circuit of the Single-Diode Model, the PV cell module output current I_{cell} can be computed using the following equation:

$$I_{cell} = I_{ph\_cell} - I_{d\_cell} - I_{R_p\_cell} \tag{I.5}$$

I_{cell}, $I_{ph-cell}$, I_{d-cell}, and $I_{Rp-cell}$ denote the PV cell module's output current, the cell photo-generated current, the diode cell current, and the PV cell parallel resistor current, respectively. The cell photo-generated current $I_{ph-cell}$ depends on the solar irradiance and temperature and can expressed by [26]:

$$I_{Ph\_cell} = \frac{G}{G_{STC}}\left(I_{Ph-STC} + K_I\left(T - T_{STC}\right)\right) \tag{I.6}$$

Where K_I is the short-circuit current temperature coefficient (A/K), G and G_{STC} = 1000 W/m^2 define the irradiation (W/m²) and its nominal value in the standard test conditions (STC). T and T_{STC} = 25 °C are the temperature and its nominal value in the STC, respectively. I_{ph-STC} is the photo-generated current in the STC, and its value is approximately equal to the PV module short circuit current in STC.

Equation (I.7) expresses the diode cell current using the Shockley equation [27]:

$$I_{d\_cell} = I_0\left(\exp\left(\frac{V_{cell} + I_{cell}R_{s\_cell}}{\alpha V_t}\right) - 1\right) \tag{I.7}$$

where R_{s-cell} is the series resistor and V_{cell} denotes the cell output voltage. α is the ideality factor of the diode, and V_t is the cell junction thermal potential, which is given by [28]:

$$V_t = \frac{n_s kT}{q} \tag{I.8}$$

n_s is the number of series cells in the PV module. In addition, the value of the saturation current of the diode I_0 related to the solar radiation and cell temperature can be calculated using the following formula [29, 30]:

$$I_0 = \frac{I_{SC-STC} + K_I\left(T - T_{STC}\right)}{\exp\left(\frac{V_{OC-STC} + K_V\left(T - T_{STC}\right)}{\alpha V_t}\right) - 1} \tag{I.9}$$

where I_{OC-STC} is the short circuit current of the cell in STC, V_{OC-STC} $V_{OC\text{-}STC}$ is the open circuit voltage in STC, and K_V is the open circuit voltage temperature coefficient (V/K).

Using Kirchhoff's law, the PV cell parallel resistor current $I_{Rp-cell}$ can be calculated as follows:

$$I_{Rp\_cell} = \frac{V_{cell} + R_{s\_cell} I_{cell}}{R_{p\_cell}} \tag{I.10}$$

Therefore, we can write Equation (I.1) which describes the I-V characteristic of the PV module as:

$$I_{PV} = \frac{G}{G_{STC}}\left(I_{Ph-STC} + K_I(T - T_{STC})\right) - I_{SD}\left(\exp\left(\frac{V_{cell} + R_{s\_cell} I_{cell}}{\alpha V_t}\right) - 1\right) - \frac{V_{cell} + R_{s\_cell} I_{cell}}{R_{p\_cell}} \tag{I.11}$$

Figure I.10 illustrates an example of the electrical characteristics of a PV panel. The figure shows the current-voltage (I-V) and power-voltage (P-V) curves. From the figure, P_{MPP}, V_{MPP}, and I_{MPP} denote the panel's power in the maximum power point (MPP), the voltage in the MPP, and the current in the MPP, respectively.

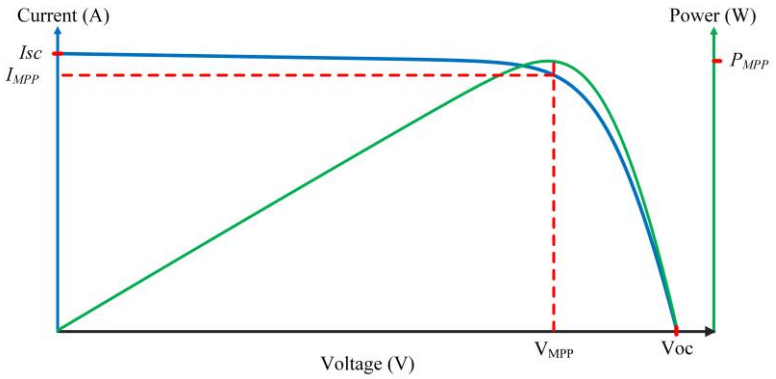


Figure I.10: The electrical characteristic I-V and P-V curves of the PV module

In order to simulate the electrical characteristic of a PV array that consists of parallel and series PV modules, the following equation is used [31]:

$$I_{PV} = I_{Ph}N_{pm} - I_{SD}N_{pm}\left(\exp\left(\frac{V_{PV} + I_{PV}R_S\left(\frac{N_{sm}}{N_{pm}}\right)}{\alpha V_t N_{sm}}\right) - 1\right) - \frac{V_{PV} + I_{PV}R_S\left(\frac{N_{sm}}{N_{pm}}\right)}{R_P\left(\frac{N_{sm}}{N_{pm}}\right)} \quad \text{(I.12)}$$

Figure I.11 shows the I-V and P-V curves of the PV array and compares them with the curves of the PV module.

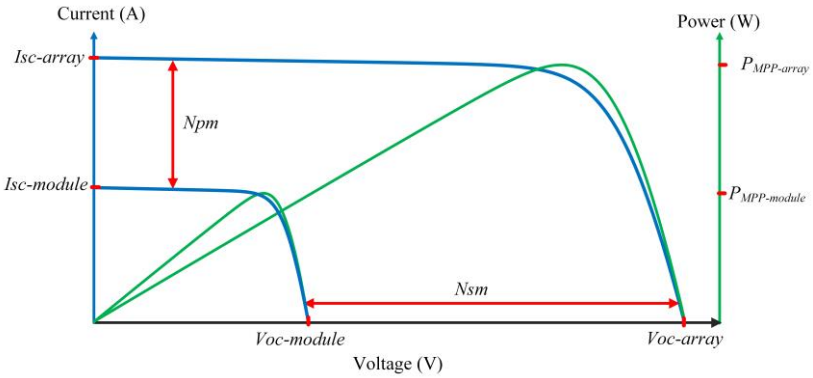


Figure I.11: The electrical characteristic of the PV array

I.3.4. Model including Ohmic Losses

I.3.4.1. Current-Based Model

Assuming the cell parallel resistance is infinite ($R_{p\_cell} = \infty$), the simplified model accounting for ohmic losses is shown in Figure I.12. This version is commonly used in design applications due to its simplicity. However, when high accuracy is required, the two-diode model with parallel components is typically preferred [6], [32].

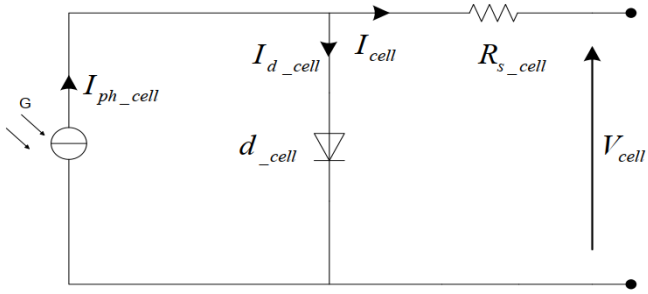


Figure I.12: Equivalent Circuit of the Photovoltaic Cell Model with Ohmic Losses

In this case, the current produced by the cell is expressed by the following equation:

$$I_{cell} = I_{ph\_cell} - I_0\left(\exp\left(\frac{V_{cell} + I_{cell}R_{s\_cell}}{\alpha V_t}\right) - 1\right) \quad \text{(I.13)}$$

I.3.4.2. Voltage-Based Model

The voltage-based model of the cell, as shown in Figure I.12, can be derived from Equation (I.13), resulting in the following expression:

$$V_{cell} = \frac{nkT}{q} \ln\left(\frac{I_{ph\_cell} - I_{cell} + I_0}{I_0} \right) - R_{s\_cell} I_{cell} \tag{I.14}$$

1.3.5. Calculation of Cell Current Under Standard Reference Conditions of Temperature T_{ref} and Irradiance G_0 [6]

1.3.5.1. Calculation of Saturation Current at T_{ref} =298K

The reverse saturation current of the diode is determined at the point where the cell current is zero ($I_{cell} = 0$), while the open-circuit voltage of the cell (V_{oc_cell}) is equal to the module's open-circuit voltage provided by the manufacturer (V_{oc_module}) divided by the number of cells in series (N_S). Thus:

$$\begin{cases} V_{cell} = V_{oc\_cell} = \dfrac{V_{oc\_module}}{N_S} \\ I_{ph\_cell} = I_{sc\_cell}\,|_{T_{ref}} = \dfrac{I_{sc\_module}\,|_{T_{ref}}}{N_p} \end{cases} \tag{I.15}$$

Here, $I_{sc\_module|Tref}$ is the short-circuit current of the module under reference conditions, as specified by the manufacturer. The reverse saturation current at T_{ref} is derived from Equations (I.13) and (I.15) as follows:

$$I_0\,|_{T_{ref}} = \frac{I_{sc\_cell}\,|_{T_{ref}}}{\left(e^{\frac{V_{sc\_cell}}{nkT_{ref}/q}} - 1 \right)} \tag{I.16}$$

1.3.5.2. Calculation of Series Resistance at T_{ref}

The series resistance of the cell is determined at the point where $V_{cell} = V_{oc\_cell} = \frac{V_{oc\_module}}{N_s}$, by evaluating the slope of the I–V curve at the open-circuit voltage point V_{oc_module}. This involves deriving Equation (I.13) and rearranging it to solve for R_{s_cell} [33, 34].

The derivative of Equation (I.13) gives:

$$dI_{cell} = 0 - I_0\,|_{T_{ref}} \frac{dV_{cell} + R_{s\_cell} dI_{cell}}{nkT_{ref}/q} \left(e^{\frac{V_{cell} + R_{s\_cell} I_{cell}}{nkT_{ref}/q}} \right) \tag{I.17}$$

From Equation (I.17), the series resistance can then be written as:

$$R_{s\_cell} = \frac{nkT_{ref}/q}{\left(e^{\frac{V_{cell} + R_{s\_cell} I_{cell}}{nkT_{ref}/q}} \right)} - \frac{dV_{cell}}{dI_{cell}} \tag{I.18}$$

Finally, evaluating this Equation under open-circuit conditions, i.e., when $V_{cell} = V_{oc\_cell}$ and $I_{cell} = 0$, yields:

$$R_{s\_cell} = \frac{nkT_{ref} / q}{\left(e^{\frac{V_{oc\_cell}}{nkT_{ref}/q}} \right) I_0 |_{Tref}} - \frac{dV_{cell}}{dI_{cell}} |_{V_{oc\_cell}} \quad \text{(I.19)}$$

Where $\frac{dV_{cell}}{dI_{cell}} |_{V_{oc\_cell}}$ represents the slope of the I–V curve at $V_{cell} = V_{oc\_cell}$, which is calculated from the I–V curve provided in the module's datasheet and then divided by the number of cells connected in series. $\frac{dV_{cell}}{dI_{cell}} |_{V_{oc\_cell}} = \frac{\frac{dV_{module}}{dI_{module}} |_{V_{oc\_module}}}{N_s}$ and the value of $\frac{dV_{module}}{dI_{module}} |_{V_{oc\_module}}$ are given by the manufacturer.

I.3.6. Calculation of Cell Current at any Temperature *T* and Irradiance *G*

The previous equations are only valid under standard operating conditions. To extend the model to various irradiance and temperature levels, a method is used to shift the reference I–V curve to new conditions.

I.3.6.1. Calculation of Short-Circuit Current at Any Temperature and Irradiance

The change in a cell's short-circuit current with temperature is described by [35-37]:

$$I_{sc\_cell} |_T = I_{sc\_cell} |_{T_{ref}} \left[1 + a\left(T - T_{ref} \right) \right] \quad \text{(I.20)}$$

where

$I_{sc\_cell} |_{T_{ref}} = \frac{I_{sc\_Module} |_{T_{ref}}}{N_p}$ and $I_{sc\_cell} = \frac{I_{sc\_Module}}{N_p}$ are given by the manufacturer. The current $I_{sc\_Module} |_{T_{ref}}$ is measured under the irradiance of 1 kW/m^2 and a temperature T_{ref} = 298K, (25°C).

α the temperature coefficient of the short-circuit current

The short-circuit current $I_{sc\_cell} = \frac{I_{sc\_Module}}{N_p}$ varies proportionally with irradiance according to the following relation:

$$I_{sc\_cell} |_G = I_{sc\_cell} |_{G_0} \frac{G}{G_0} \quad \text{(I.21)}$$

$I_{sc\_cell}|_{G0}$ the Short-circuit current under standard conditions (T_{ref}, G_0)

Based on Equations (I.20) and (I.21), the variation of short-circuit current with any given temperature and irradiance is expressed as:

$$I_{sc\_cell}\mid_{T,G} = I_{sc\_cell}\mid_{T_{ref},G_0} \frac{G}{G_0}\left[1+a\left(T-T_{ref}\right)\right] \tag{I.22}$$

I.3.6.2. Calculation of Saturation Current at Any Temperature

The variation of the diode's reverse saturation current with temperature is determined using the following expression [36-38]:

$$I_o\mid_T = I_o\mid_{T_{ref}} \left(\frac{T}{T_{ref}}\right)^3 e^{\frac{-qE_g}{nk}\left(\frac{1}{T}-\frac{1}{T_{ref}}\right)} \tag{I.23}$$

where E_g is the Bandgap energy and $I_o\mid_{T_{ref}}$ denotes the reverse saturation current at the reference temperature, as given by Equation (I.16)

Accordingly, to compute the current produced by the cell, it is necessary to solve the nonlinear characteristic equation (I.13). This is typically done using the Newton-Raphson method, described as follows:

$$x_{n+1} = x_n \frac{f\left(x_n\right)}{f^{'}\left(x_n\right)} \tag{I.24}$$

where $f^{'}\left(x_n\right)$ the derivative of $f\left(x_n\right)$, x_n the actual value of x, and x_{n+1} the new value of x.
By applying this method to Equation (I.13), we obtain:

$$\begin{cases} f\left(I_{cell}\right) = I_{sc\_cell}\mid_T - I_{0\_cell}\mid_T \left(e^{\frac{V_{cell}+R_{s\_cell}I_{cell}}{nkT/q}}\right) - I_{cell} \\ f^{'}\left(I_{cell}\right) = 0 - I_0\mid_T \frac{R_{s\_cell}}{nkT/q}\left(e^{\frac{V_{cell}+R_{s\_cell}I_{cell}}{nkT/q}}\right) - 1 \end{cases} \tag{I.25}$$

Using the Newton-Raphson method as described in Equation (I.24) makes it possible to compute the current value at any given temperature and irradiance (T, G) for each iteration (j). Thus:

$$I_{cell}[j] - \frac{I_{sc\_cell}\mid_{T,G} - I_o\mid_T \left(e^{\frac{V_{cell}[j]+R_{s\_cell}I_{cell}[j]}{nkT/q}} - 1\right) - I_{cell}[j]}{-I_o\mid_T \frac{R_{s\_cell}}{nkT/q}\left(e^{\frac{V_{cell}[j]+R_{s\_cell}I_{cell}[j]}{nkT/q}}\right) - 1} \tag{I.26}$$

I.3.7. Characteristics of a PV Cell

The primary characteristic of a solar cell is its current-voltage (I-V) curve, which illustrates how the cell responds to various load conditions under specific solar radiation and temperature levels, as shown in Figure I.13 [6].

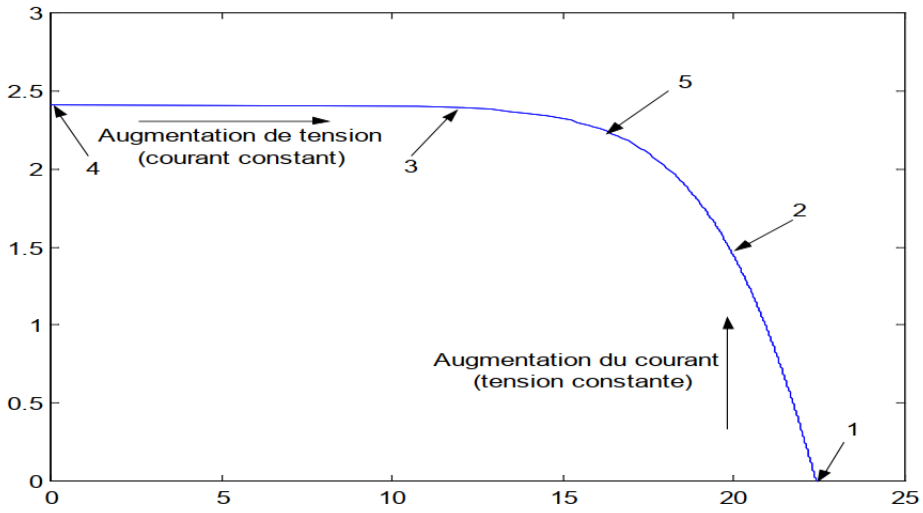


Figure I.13: Typical I-V Characteristic Curve of a Solar Cell

There are three key points on this curve:

- The **maximum power point (MPP)**, where the cell delivers its peak power output (Point 5);
- The **short-circuit point**, where voltage is zero and current is at its maximum (Point 4);
- The **open-circuit point**, where current is zero and voltage is at its maximum (Point 1).

The I-V characteristic curve can also be divided into three distinct regions:

- A region where the cell behaves primarily as a **voltage source** (between Points 1 and 2);
- A region where the cell acts mainly as a **current source** (between Points 3 and 4);
- A **transition region** (between Points 2 and 3), where neither voltage nor current remains constant.

I.3.7.1. Open-Circuit Voltage

When a solar cell is exposed to a constant light source with no electrical load connected across its terminals, it generates a direct voltage known as the open-circuit voltage. This voltage may slightly vary depending on the cell technology and the level of illumination. It corresponds to the threshold voltage of a diode, reinforcing the analogy between a solar cell and a PN junction. To obtain a higher output voltage from a module, multiple cells must be connected in series.

I.3.7.2. Short-Circuit Current

Conversely, when the solar cell is short-circuited (i.e., the voltage is zero), it delivers its maximum current, referred to as the short-circuit current. The photocurrent generated is directly proportional to both the intensity of the incident light and the surface area of the solar panel. Therefore, increasing either of these factors leads to a higher current output. To boost the overall current from the module, several cells need to be connected in parallel.

I.3.7.3. Power-Voltage Characteristic

The maximum power delivered by a solar cell, P_{max_cell}, occurs at the point with coordinates (V_{mp_cell}, I_{mp_cell}), and is calculated as the product of voltage and current at that point:

$$P_{\max\_cell} = V_{mp\_cell} \times I_{mp\_cell} \tag{I.27}$$

I.3.7.4. Fill Factor of a PV Cell

The fill factor (*FF*) is defined as the ratio of the maximum power output to the product of the open-circuit voltage and short-circuit current:

$$FF = \frac{P_{\max\_cell}}{V_{oc\_cell} \times I_{sc\_cell}} \tag{I.28}$$

I.3.7.5. Efficiency

The efficiency of a photovoltaic cell is the ratio of the maximum electrical power output to the incident solar power, which is the product of irradiance G and the effective surface area S_e of the cell:

$$\eta_{pv} = \frac{P_{\max\_cell}}{S_e \times G} \tag{I.29}$$

where S_e is the effective surface area in square meters (m^2).

I.3.8. Connection of Cells

High-power applications with high voltage and/or current require a high-power source. PV strings or PV arrays are PV systems that consist of multi-PV panels, allowing high electrical power generation.

I.3.8.1. Series Connection of Cells

PV string is a number of PV panels wired in a series set. The aim of establishing a PV string is to raise the voltage of the PV system. The string's voltage is the sum of the PV panels voltage and has the same current. When identical cells are connected in series (as illustrated in Figure I.14a), the current remains constant across the branch, but the total voltage increases proportionally to the number of cells [39]. Equations (I.30) and (I.31) formulate the PV string voltage and current:

$$V_{PV-string} = V_{PV} N_{sm} \tag{I.30}$$

$$I_{PV-string} = I_{PV} \tag{I.31}$$

N_{sm}: number of series PV modules.

I.3.8.2. Parallel Connection of Cells

When identical cells are connected in parallel (as shown in Figure I.14b), the voltage remains equal to that of a single cell, but the total current increases with the number of cells in parallel [6].

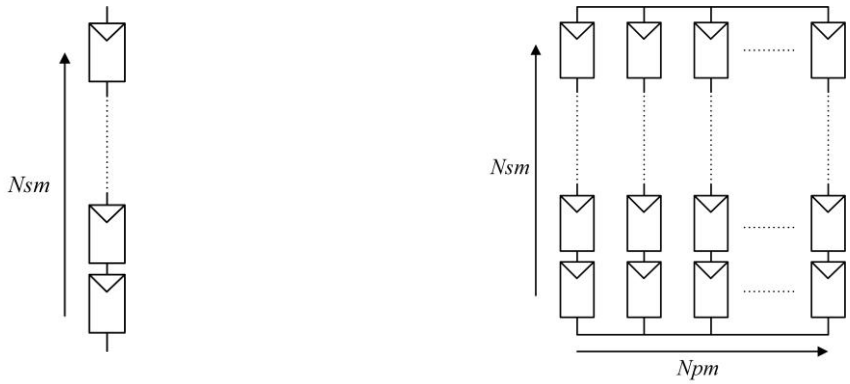


Figure I.14: PV system configuration: string (a), array (b)

I.3.8.3. Series-Parallel Connection of Cells (PV Array)

To achieve higher PV power outputs, multiple modules need to be connected in series and/or parallel, as illustrated in Figure I.15. The resulting performance curve of such a series-parallel configuration resembles that of a single photovoltaic cell but with modified electrical parameters. It's important to note that, just like with individual cells, only identical modules should be combined in series or parallel configurations [40].

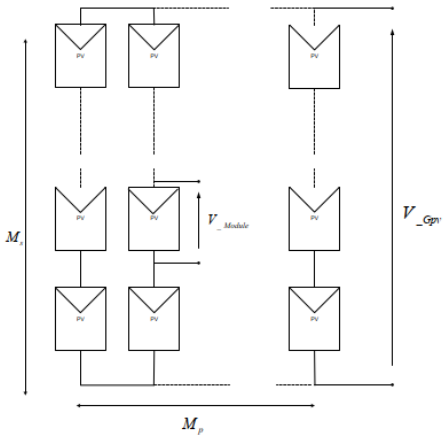


Figure I.15: Photovoltaic modules connected in series and parallel

A PV array is a number of PV panels connected in series and parallel. Its voltage is equal to the sum of the voltage of series panels, and its current is equal to the sum of parallel PV panels current as expressed in the following equation:

$$V_{PV-array} = V_{PV} N_{sm} \tag{I.32}$$

$$I_{PV-array} = I_{PV} N_{pm} \tag{I.33}$$

N_{pm} the number of parallel PV modules.

I.4. Photovoltaic Module (Panel)

A PV module, illustrated in Figure I.16, consists of a set of elementary photovoltaic cells connected in series and/or in parallel to achieve the desired electrical characteristics, such as power, short-circuit current, or open-circuit voltage.

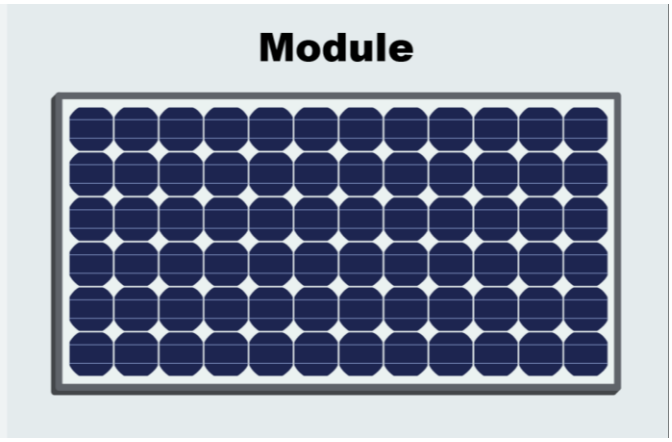


Figure I.16: Photovoltaic Module

I.4.1. Modeling of Photovoltaic Module

I.4.1.1. Current Model

The model developed for a single cell can be applied to the case of connecting cells in series and parallel to obtain the model of a photovoltaic module (assuming all these cells inside the module are identical) [6]. Figure I.17 shows the equivalent model of a photovoltaic module.

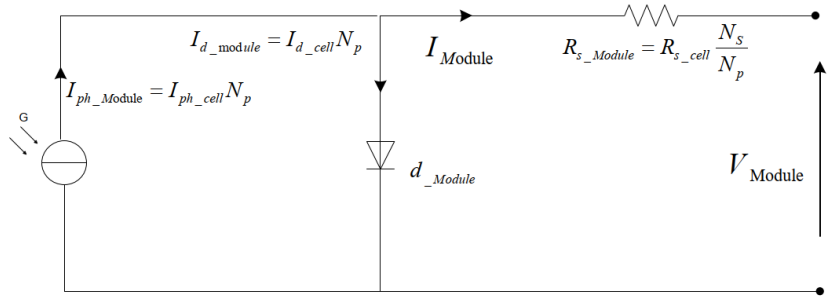


Figure I.17: Equivalent circuit of a photovoltaic module (panel) model.

According to this figure and if we assume that the photovoltaic module contains N_s cells in series and N_p cells in parallel, the current model of the module is based on the following equation [41]:

$$I_{Module} = I_{ph\_Module} - I_{d\_Module} \tag{I.34}$$

where

$$\begin{cases} I_{ph\_Module} = I_{ph\_cell} N_p = I_{sc\_cell} \mid_T N_p \\ I_{d\_Module} = I_{d\_cell} N_p = I_0 \mid_T \left(e^{\frac{V_{cell} + R_{s\_cell} I_{cell}}{nkT/q}} - 1 \right) N_p \end{cases} \tag{I.35}$$

Thus, the current model of a photovoltaic module is written by:

$$I_{Module} = I_{ph\_Module} - N_p I_0 \mid_T \left(e^{\frac{V_{cell} + R_{s\_cell} I_{cell}}{nkT/q}} - 1 \right) \tag{I.36}$$

I.4.1.2. Voltage Model

The voltage model of the module shown in Figure I.17 can be deduced from equation (I.36) by making the following changes [6]:

$$\begin{cases} V_{cell} = \dfrac{V_{Module}}{N_s} \\ I_{cell} = \dfrac{I_{Module}}{N_p} \end{cases} \tag{I.37}$$

By substituting Equation (I.37) into Equation (I.36), the voltage of the PV module can be deduced as follows:

$$V_{Module} = N_s \left[nkT/q \ln\left(\frac{I_{ph\_Module} - I_{Module}}{N_p I_o \mid_T} \right) - R_{s\_Module} \frac{I_{Module}}{N_s} \right] \tag{I.38}$$

where R_{s_Module} represents the series resistance of the module, which is given by $(R_{s\_Module} = R_{s\_cell} \dfrac{N_s}{N_p})$

.

For our case, based on the voltage model of the cell described by (I.14), we can directly calculate the module voltage at any temperature *T*:

$$V_{Module} = N_s V_{cell} = N_s \underbrace{\left[nkT/q \ln\left(\frac{I_{ph\_cell} \mid_T - I_{cell} + I_o \mid_T}{I_o \mid_T} \right) - R_{s\_cell} \mid_T I_{cell} \right]}_{V_{cell}} \tag{I.39}$$

I.5. Electrical Characteristics of a PV Module

In our thesis, we adopted the BP SX 150 photovoltaic module from BP Solar. The SX series from BP Solar provides cost-effective photovoltaic power for general use, either for directly operating DC loads or AC loads in systems with inverters. The module is composed of 72 multi-crystalline silicon solar cells connected in series to produce a maximum power of 150W. The electrical characteristics of this photovoltaic module are provided by the manufacturer (BP Solar's SX series) in table (I.1).

Electrical Characteristics[1]

	SX 150	SX 140[2]
Maximum power (P_{max})[3]	150W	140W
Voltage at P_{max} (V_{mp})	34.5V	34.0V
Current at P_{max} (I_{mp})	4.35A	4.11A
Warranted minimum P_{max}	140W	130W
Short-circuit current (I_{sc})	4.75A	4.5A
Open-circuit voltage (V_{oc})	43.5V	42.8V
Temperature coefficient of I_{sc}	(0.065±0.015)%/°C	
Temperature coefficient of voltage	-(160±20)mV/°C	
Temperature coefficient of power	-(0.5±0.05)%/°C	
NOCT[5]	47±2°C	
Maximum series fuse rating	20A (U version) 15A (S, L versions)	
Maximum system voltage	600V (U.S. NEC rating) 1000V[4] (TÜV Rheinland rating)	

Table I.1: Electrical Characteristics of the BP SX 150 PV Module

The current-voltage (I-V) characteristic shown in Figure I.18 describes the behavior of the photovoltaic module under specific weather conditions (irradiance G=1000 W/m² and ambient temperature T=25°C) [39].

The I-V curve of the photovoltaic module passes through three important points, which are:

- The short-circuit current I_{sc_Module} at point C.
- The open-circuit voltage V_{oc_Module} at point S.
- The maximum power P_{max} at point M.

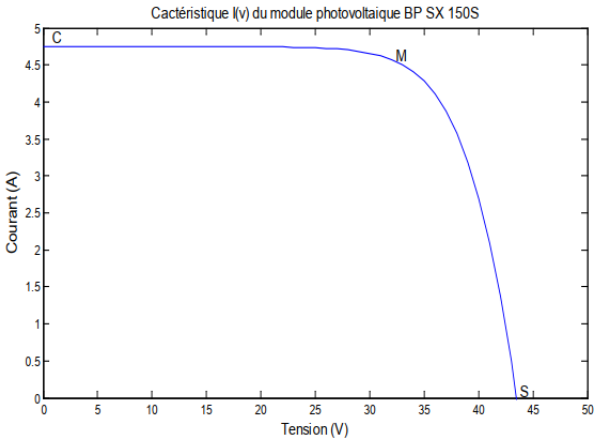
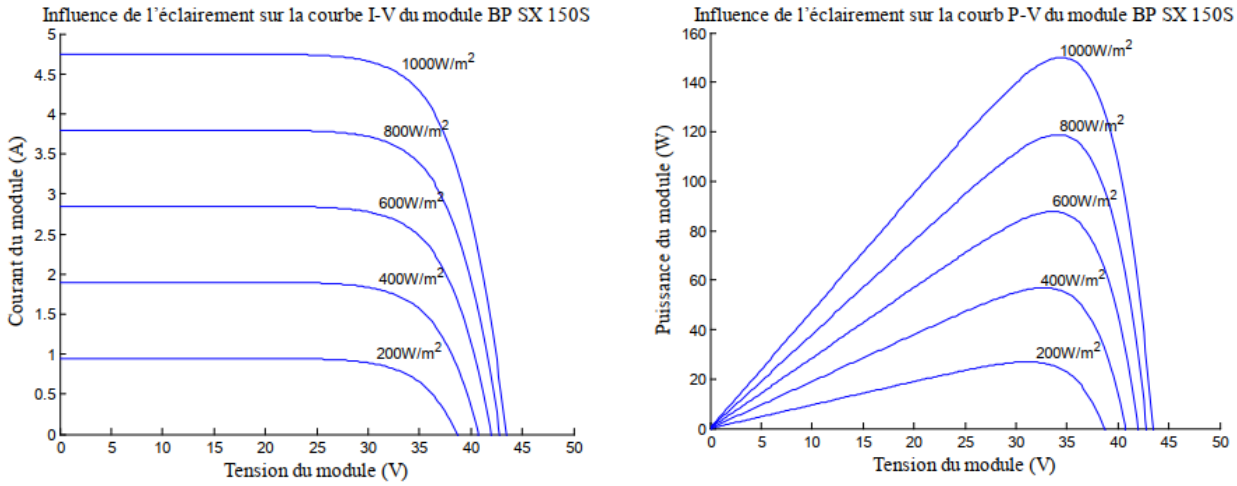


Figure I.18: Current-Voltage Characteristic of a Photovoltaic Module

I.5.1. Effect of Solar Irradiance on I_{sc_Module}, V_{oc_Module}, and P_{max}

Figures I.19 (a and b) illustrate how current and power vary with voltage under different irradiance levels while keeping the temperature constant. It can be observed that the short-circuit current

increases proportionally with the intensity of solar radiation [42]. However, the open-circuit voltage does not exhibit the same sensitivity to irradiance changes, which remains nearly constant even under low sunlight conditions [6].

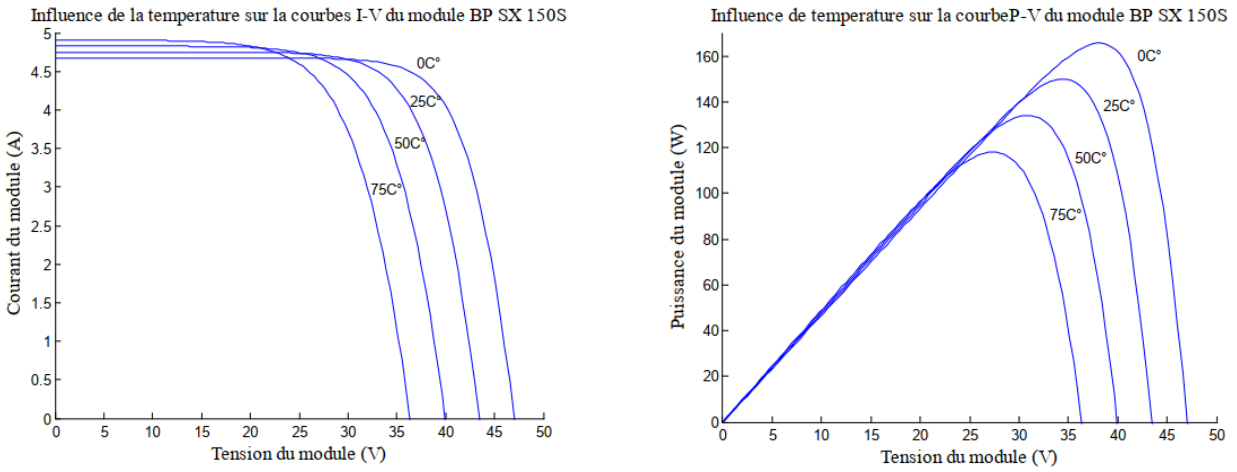


(a) (b)

Figure I.19: I-V and P-V curves of a panel under varying sunlight conditions. (a) I-V curves, (b) P-V curves

I.5.2. Effect of Temperature on I_{sc_Module}, V_{oc_Module}, and P_{max}

Figures I.20 (a and b) show the I-V and P-V curves of a photovoltaic module at different operating temperatures, under constant irradiation. It is observed that temperature has little impact on the short-circuit current. However, the open-circuit voltage decreases noticeably with rising temperature by about 2 mV per degree [43]. This temperature increase also causes a drop in the maximum available power, typically around 0.35% per degree [43]. Therefore, when designing a photovoltaic system, it's crucial to account for local temperature variations.

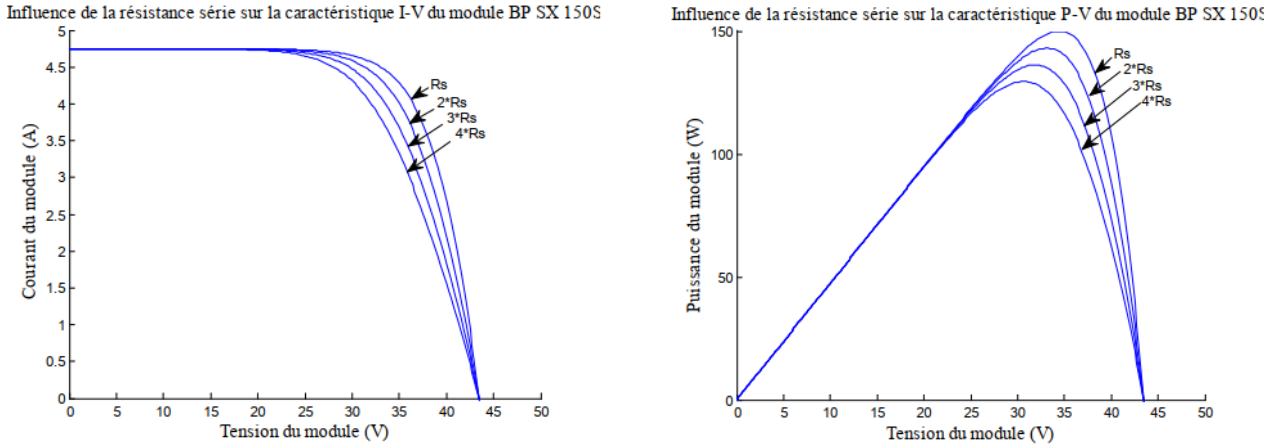


(a) (b)

Figure I.20: I-V and P-V Curves of a Photovoltaic Module at Various Temperatures (G = 1000 W/m²)

I.5.3. Impact of Series Resistance

Figure I.21(a) illustrates how the series resistance affects the I-V characteristic curve of a photovoltaic module. An increase in series resistance leads to a reduced slope in the I-V curve and results in a drop in the output power of the module, as depicted in Figure I.21(b).



(a) (b)

Figure I.21: Effect of Series Resistance on the I-V and P-V Characteristic of a PV Module.

I.5.4. Partial shading influence on PV system's electrical characteristics

Partial shading significantly affects the efficiency of solar panels. It reduces the amount of power generated, increases the mismatch losses, and can result in permanent damage, contributing to the panels' destruction over time [44-46]. Various factors influence the severity of these impacts, including the shading area, the arrangement of shaded panels within the array, the connections between panels, and the geometry of the shading [47]. Global maximum power point tracking, PV module reconfiguration, and bypass diodes are solutions proposed to mitigate the impact of partial shading. Figure I.22 shows the I-V and P-V curves during partial shading.

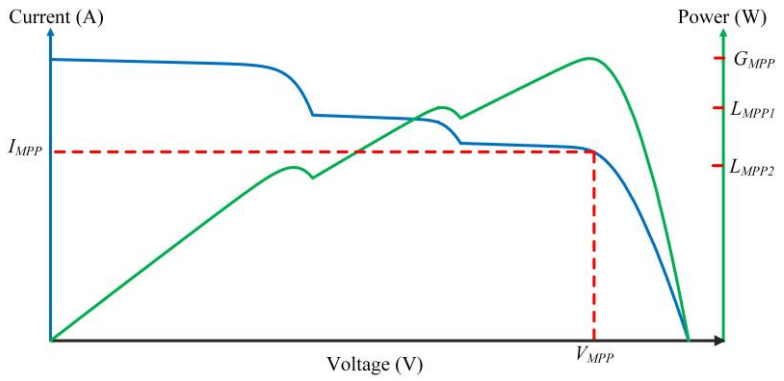


Figure I.22. Partial shading impact on I-V curve (a), P-V curve (b)

I.6. Photovoltaic Generator structure and Modeling

I.6.1. Structure of a PV Generator

To achieve higher power outputs, it is necessary to connect several photovoltaic modules in series and/or parallel, as shown in Figure I.23. The resulting I-V characteristic of a series-parallel connection of modules resembles that of a single solar cell, but with different electrical parameters, such as voltage and current. Specifically, in a series-parallel arrangement, the current produced by the system

remains the same as that of an individual cell connected in parallel, while the voltage increases proportionally based on the number of modules connected in series. Similarly, when modules are connected in parallel, the voltage remains constant, but the current increases according to the number of modules [6].

It is crucial to ensure that only identical modules are connected in series and parallel to maintain the performance and reliability of the photovoltaic generator. Just like for individual cells, combining non-matching modules could lead to performance issues and electrical imbalances within the system [31].

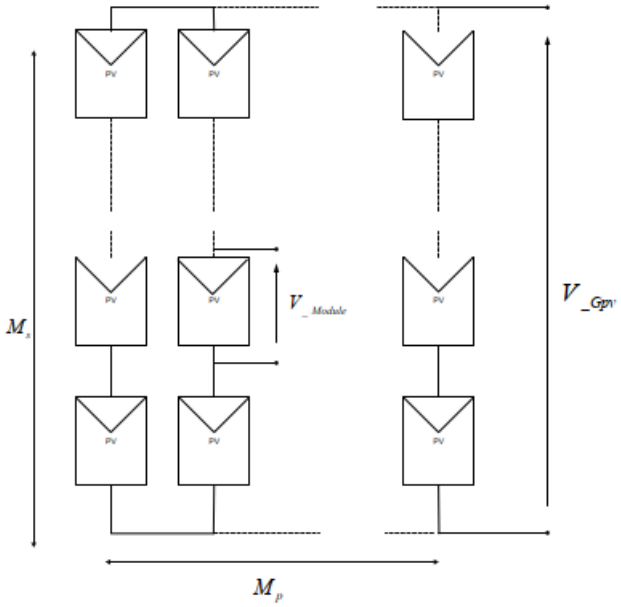


Figure I.23: Photovoltaic modules connected in series and parallel.

I.6.2. Modeling of a PV Generator

I.6.2.1. PVG current model

The model of a PVG can be represented by the equivalent circuit shown in Figure I.24 [6], [48].

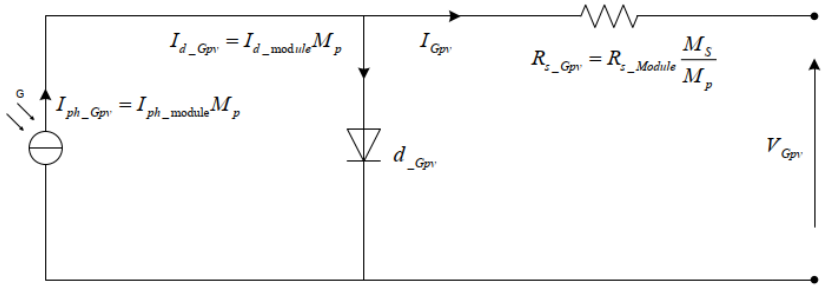


Figure I.24: Equivalent circuit of a PVG

According to the figure, and when we assume that the PVG contains M series-connected modules and M_p parallel-connected modules, with each module consisting of N_s series-connected cells and N_p parallel-connected cells, the mathematical model can be developed in the same way as for the PVG module. Indeed, the current delivered by the photovoltaic generator is given by:

$$I_{Gpv} = I_{ph\_Gpv} - I_{d\_Gpv} \tag{I.40}$$

According to these, the relationships between the generator quantities and those of the module are:

$$\begin{cases} I_{ph\_Gpv} = I_{ph\_Module} M_p \\ I_{d\_Gpv} = I_{d\_Module} M_p \end{cases} \quad (I.41)$$

On the other hand, the relationships between the module quantities and those of the cell are expressed by equation (I.35). By substituting (I.35) into (I.41), we obtain:

$$\begin{cases} I_{ph\_Gpv} = I_{sc\_cell}\,|_T \; N_p M_p \\ I_{d\_Gpv} = I_o\,|_T \left(e^{\frac{V_{cell} + R_{s\_cell} I_{cell}}{nkT/q}} - 1 \right) N_p M_p \end{cases} \quad (I.42)$$

By substituting the first and second equations of (I.42) into (I.40), we obtain the mathematical current model of the PVG as follows:

$$I_{Gpv} = I_{sc\_cell}\,|_T \left(N_p M_p \right) - \left(N_p M_p \right) I_o\,|_T \left(e^{\frac{V_{cell} + R_{s\_cell} I_{cell}}{nkT/q}} - 1 \right) \quad (I.43)$$

I.6.2.2. PVG voltage model

The PVG voltage model, represented in Figure I.24, can be deduced from equation (I.43) by applying the following changes [6]:

$$\begin{cases} V_{cell} = \dfrac{V_{Module}}{N_s} = \dfrac{V_{Gpv}}{N_s M_s} \\ I_{cell} = \dfrac{I_{Module}}{N_p} = \dfrac{I_{Gpv}}{N_p M_p} \end{cases} \quad (I.44)$$

By substituting Equation (I.44) into Equation (I.43), we obtain:

$$I_{Gpv} = I_{sc\_cell}\,|_T \left(N_p M_p \right) - \left(N_p M_p \right) I_o\,|_T \left(e^{\frac{\frac{V_{Gpv}}{N_S M_S} + R_{S\_cell} \frac{I_{Gpv}}{N_p M_p}}{nkT/q}} - 1 \right) \quad (I.45)$$

This leads to:

$$V_{Gpv} = \left[\left(N_s M_s \right) nkT/q \ln \left(\frac{I_{sc\_cell}\,|_T \left(N_p M_p \right) - I_{Gpv}}{I_o\,|_T \left(N_p M_p \right)} + 1 \right) - R_{s\_Gpv} I_{Gpv} \right] \quad (I.46)$$

Where R_{s_Gpv} represents the series resistance of the PVG, which is given by $(R_{s\_Gpv} = R_{s\_Module} \frac{M_S}{M_p})$.

I.7. PVG-based standalone power supply system

A PVG can operate over a wide range of output voltages and currents, but it can only deliver maximum power at specific values of voltage and current. It is well known that a PVG exhibits nonlinear I-V characteristics with one or more maximum power points (MPPs). These characteristics depend, among other factors, on solar irradiance and cell temperature. Additionally, depending on the load characteristics connected to the PVG, there may be a significant mismatch between the potential

power of the PVG and the power actually delivered to the load in a direct connection setup. To extract the maximum available power from the PVG at any moment and transfer it to the load, the most common approach is to insert a power adaptation stage between the generator and the load, as shown in Figure I.25. This stage acts as an interface between the PVG and DC load, using a control strategy to ensure that the power delivered by the PVG closely approaches the maximum available power P_{max} [49].

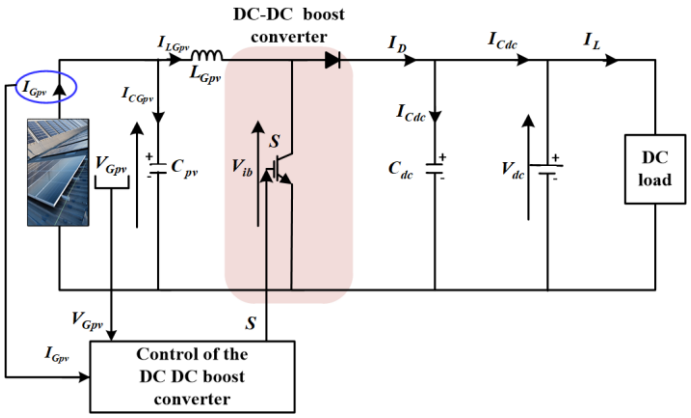


Figure I.25: Schematic diagram of the PVG DC-DC boost converter-based standalone power supply system.

Through specific control, the adaptation stage enables the PVG to supply its maximum power, denoted $P_{max}=I_{opt}V_{opt}$, where V_{opt} and I_{opt} represent the optimal voltage and current of the PVG for a given I-V curve), while also ensuring that the voltage or current matches the load's requirements.

To keep the PVG operating as often as possible in its optimal power region, the commonly adopted solution is to use a power converter that acts as a source-load adapter.

I.7.1. DC-DC Converters

The DC-DC converters are power converters that transform a fixed DC voltage into a variable DC voltage. They consist of capacitors, inductors, and power switches. Under ideal conditions, these components consume no power, which is why DC-DC converters are known for their high efficiency. Typically, the switch is a MOSFET transistor operating in either cut-off or saturation mode. When the switch is off, its current is zero, and it dissipates no power. When it is saturated, the voltage drops across it is nearly zero, resulting in minimal power loss. The switch S is controlled using a PWM (Pulse Width Modulation) signal with a fixed switching frequency f_s and a variable duty cycle D [6].

I.7.2. Types of DC-DC Converters

There are several DC-DC converter topologies, generally classified as isolated or non-isolated. Isolated topologies use a high-frequency isolation transformer and are commonly found in switched-mode power supplies. The most well-known of these topologies include flyback, half-bridge, and full-bridge converters.

In photovoltaic applications, especially in islanded mode and grid-connected systems, isolated topologies are often used when electrical isolation is required for safety reasons [50].

Non-isolated topologies do not use isolation transformers. They are typically employed in DC motor drive systems. These are further classified into three categories, Buck converters, Boost converters, and Buck-Boost converters [51].

The buck topology is used for applications requiring lower output voltage. In PV systems, buck converters are commonly used for battery charging and in water pumping applications [52].

The boost topology is used to increase voltage. Energy production systems often employ boost converters to raise the PVG output voltage to service levels before the inverter stage. Finally, there are converters capable of both stepping up and stepping down the voltage, such as the buck-boost converter [52].

In this section, we will focus specifically on the DC-DC boost converter, which is widely known for its voltage-boosting capability.

I.7.2.1. Boost Converter

In a boost converter-based PVG, as illustrated in Figure I.26, the average output voltage is higher than the input voltage, which is why it is also called a step-up converter. This topology requires a controlled switch for turning on and off (such as a MOSFET or IGBT) and a diode that switches on and off automatically [52].

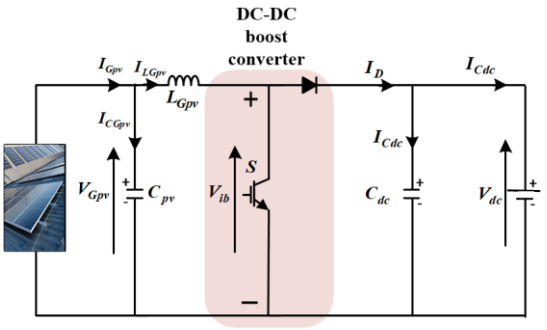


Figure I.26: Electrical circuit of a DC-DC boost converter-based PVG.

I.7.2.2. Operating Principle of a boost converter

The operating principle of a boost converter is based on the position of its switch *S*, whether it is open or closed. During the time interval $T_{ON}=D\cdot T_s$, where D is the duty cycle, the closed switch connects the input (through the inductor) to ground. As a result, energy is stored in the inductor due to the increasing current flowing through it. During this phase, the diode is reverse-biased (blocked), so no current flows to charge the output DC voltage source, as shown in Figure I.27 [53].

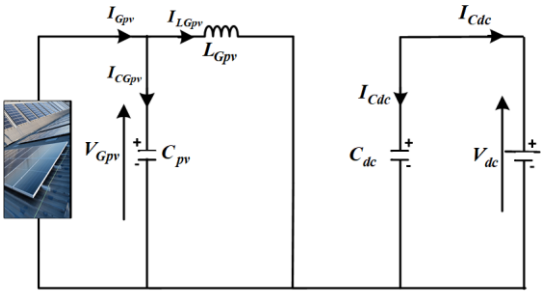


Figure I.27: Equivalent circuit of the boost converter when the switch *S* closed.

In the second phase when the switch *S* is open during the interval $T_{OFF}=(1-D)T_s$, as illustrated in Figure I.28, the output output DC voltage source receives energy both from the inductor (previously stored) and directly from the input (the PVG). In steady-state operation, the output capacitor is

assumed to have sufficient capacity to maintain a constant output voltage Vdc (and thus the current flowing through the output capacitor is assumed to be zero) [8].

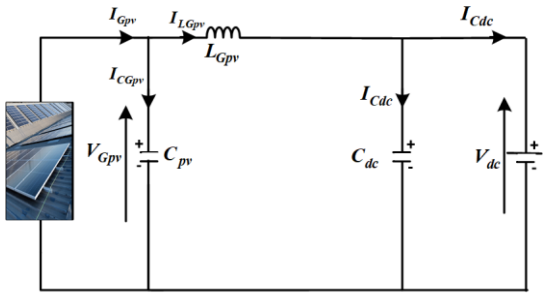


Figure I.28: Equivalent circuit of the boost converter when the switch *S* open.

I.7.2.3. Operation in Continuous Conduction Mode (CCM)

In steady-state, this mode is characterized by a continuous inductor current, meaning $I_{LGpv}>0$ at all times. When the switch is closed, the drop voltage across the inductor V_{LGpv} is given by [6]:

$$V_{LGpv} = V_{Gpv} \tag{I.47}$$

Whereas when the switch *S* is open, applying Kirchhoff's voltage law gives:

$$V_{LGpv} = V_{Gpv} - V_{dc} \tag{I.48}$$

On the other hand, the drop voltage across the inductor V_{LGpv} is given by:

$$V_{LGpv} = L_{Gpv}\frac{dI_{LGpv}}{dt} \tag{I.49}$$

Thus, the inductor current I_{LGpv} is expressed as:

$$I_{LGpv} = \int_0^{DT_s}\frac{V_{LGpv}}{L_{Gpv}}dt + \int_{DT_s}^{T_s}\frac{V_{LGpv}-V_{dc}}{L_{Gpv}}dt \tag{I.50}$$

According to these Equations, the inductor current and the drop voltage across the inductor are shown in Figure I.29.

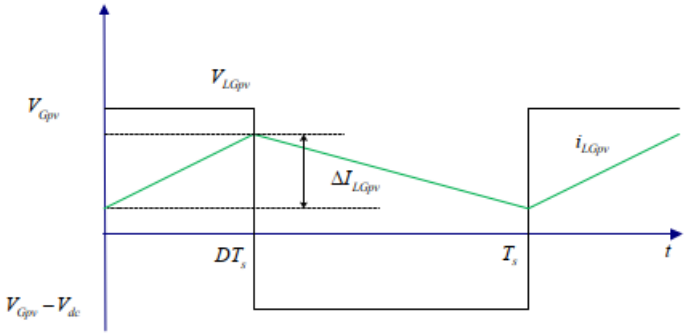


Figure I.29: Operating of boost converter in CCM.

where ΔI_{LGpv} represents the ripple in the inductor current i_{LGpv}.

We will later assume that our MPPT always operates in continuous mode; therefore, it is necessary to ensure that the converter functions in this mode.

Since the average voltage across the inductor is zero in steady-state, it follows that:

$$V_{Gpv}T_{ON} = T_{OFF}\left(V_{dc} - V_{Gpv}\right) \tag{I.51}$$

This leads to:

$$V_{dc} = \frac{1}{1-D}V_{Gpv} \tag{I.52}$$

Using the power balance principle and when we assume that the inductor filter and power converter losses are negligible, we obtain:

$$V_{Gpv}I_{Gpv} = V_{dc}I_{dc} \tag{I.53}$$

According to Equations (I.52) and (I.53), we obtain:

$$I_{dc} = I_{Gpv}\left(1-D\right) \tag{I.54}$$

I.7.2.3.1. Calculation of the input inductance value in CCM

At the limit between continuous and discontinuous mode, the inductor current starts from and returns to zero within one period Ts , as shown in Figure I.30 [6]. In this case, the average current at the limit passing through the input filter inductor can be expressed as in Equation (I.55):

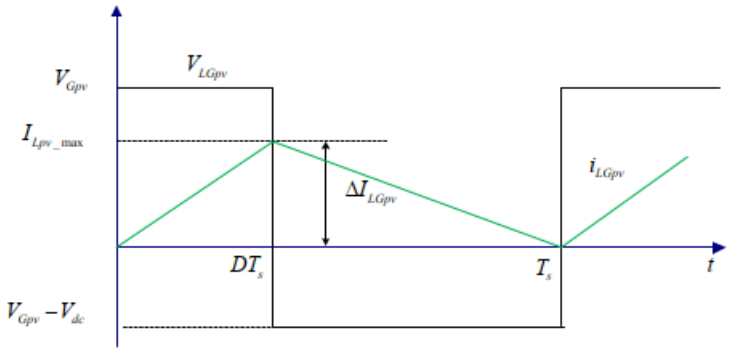


Figure I.30: Limit between continuous and discontinuous modes.

$$I_{LGpv} = \frac{I_{LGpv\_\max}}{2} \tag{I.55}$$

This Equation can be written as:

$$I_{LGpv} = \frac{DT_sV_{Gpv}}{2L_{Gpv}} \tag{I.56}$$

From Equations (I.52) and (I.56), we obtain:

$$I_{LGpv} = \frac{D\left(1-D\right)T_sV_{dc}}{2L_{Gpv}} \tag{I.57}$$

In steady-state, since the average current through the DC-DC boost converter's input capacitor is zero, it yields:

$$I_{Gpv} = I_{LGpv} \tag{I.58}$$

From Equations (I.54), (I.57) and (I.58), we obtain:

$$I_{dc} = \frac{D(1-D)^2 T_s V_{dc}}{2L_{Gpv}} \tag{I.59}$$

When considering that the DC output voltage V_{dc} is constant, it is then possible to plot the evolution of the output current and the inductor current at the limit between continuous and discontinuous mode as a function of the duty cycle, as shown in Figure I.31:

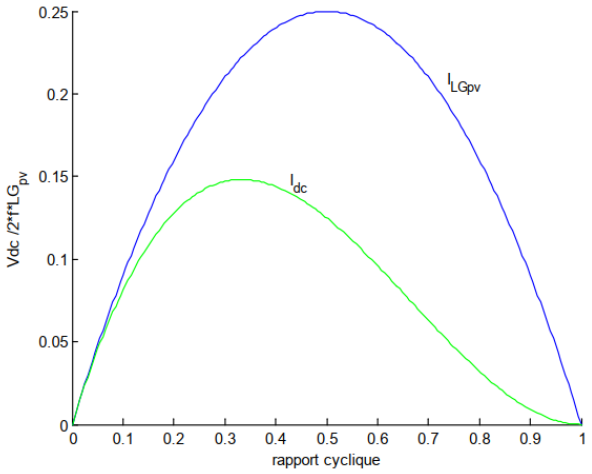


Figure I.31: DC-DC boost converter's output current and inductor current at the limit between continuous and discontinuous modes under constant output DC voltage

Figure I.31 illustrates that for a given duty cycle D with constant DC output voltage, if the average DC-DC boost converter's output current falls below the curve of I_{dc} (or if the average inductor current drops below the curve I_{LGpv}), the boost converter will enter the discontinuous mode. These curves are important as it provides the threshold current for continuous mode, which is the mode in which we aim to operate the DC-DC converter [56].

The derivative calculations of Equations (I.57) and (I.59) allows the determination of the maximum current values I_{dc_max} and i_{LGpv_max}, respectively, at D=1/3 and D=1/2, as follows:

$$I_{dc\_max} = \frac{2T_s V_{dc}}{27L_{Gpv}} \tag{I.60}$$

$$I_{LGpv\_max} = \frac{T_s V_{Gpv}}{8L_{Gpv}} \tag{I.61}$$

Equations (I.60) and (I.61) can be used to calculate the minimum input inductance value that allows the boost converter to operate in CCM. The value of this inductance can be calculated using one of the following two equations:

Using D=1/3:

$$L_{Gpv\_min} = \frac{2T_s V_{dc}}{27I_{dc\_max}} \tag{I.62}$$

Using D=1/2

$$I_{LGpv\_min} = \frac{T_s V_{Gpv}}{8I_{LGpv\_max}} \tag{I.63}$$

Figure I.32 shows the waveforms of the boost converter in CCM.

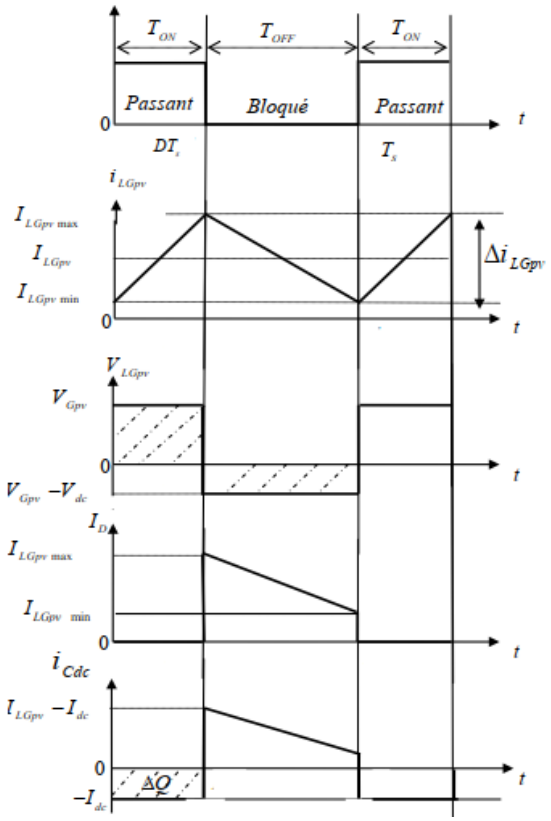


Figure I.32: Current/voltage waveforms of a boost converter in CCM.

According to this figure, the inductor current and output DC voltage ripples are given as follows:

I.7.2.3.2. Inductor current ripple

The inductor current ripple ΔI_{LGpv} satisfies Ohm's law across L_{Gpv} during the time T_{ON}, which can be calculated as follows:

The drop voltage across the inductor is expressed as a function of L_{Gpv} and ΔI_{LGpv} by:

$$V_{LGpv} T_{ON} = L_{Gpv} \Delta I_{LGpv} \tag{I.64}$$

Therefore, the inductor current ripple ΔI_{LGpv} is expressed by:

$$\Delta I_{LGpv} = \frac{V_{Gpv} D}{L_{Gpv} f_s} \tag{I.65}$$

I.7.2.3.3. Output DC voltage ripple

From the Current/voltage waveforms in Figure I.32, the output DC voltage ripple can be calculated as follows [56]:

$$\Delta V_{dc} = \frac{\Delta Q}{C_{dc}} = \frac{I_{dc} D T_s}{C_{dc}} \tag{I.66}$$

According to Equations (I.62) and (I.66), we obtain:

$$\Delta V_{dc} = \frac{I_{Gpv} D(1-D)}{f_s C_{dc}} \tag{I.67}$$

I.7.2.4. Sizing of DC-DC boos converter components

I.7.2.4.1. Sizing of DC-DC boost converter's input inductor

In a DC-DC boost converter-based PVG interface, the filter inductor plays a fundamental role in enabling the voltage conversion process. Its primary function is to store energy during the switch's T_{ON} period. When the switch S is closed, the inductor is connected directly to the PVG voltage source, and a current begins to flow through it. This current creates a magnetic field, allowing the inductor to accumulate energy. During this period, the output is isolated, and no energy is delivered to the load from the PVG.

When the switch opens (T_{OFF} period), the magnetic field within the inductor collapses, and the stored energy is released. This energy combines with the PVG output voltage and is transferred to the output capacitor and the load through the diode. This mechanism is what allows the converter to increase the output voltage above the input voltage.

Additionally, the inductor helps regulate and smooth the current flow from the PVG. By limiting rapid changes in current (di/dt) (reducing the current ripple), it reduces electromagnetic interference (EMI) and stress on the components. This smoothing effect is particularly important when aiming to maintain CCM, where the inductor current never falls to zero. Operating in CCM generally results in higher efficiency and better performance. Proper selection and sizing of the inductor are therefore essential for stable, efficient, and reliable boost converter operation. Using Equation (I.65), the inductance value can be determined based on a specified ripple in the inductor current as follows:

$$L_{Gpv} = \frac{DV_{Gpv}}{\Delta I_{LGpv} f_s} \tag{I.68}$$

From Figure I.26, the boost converter is powered by the PVG output voltage, which corresponds to the voltage of a single module at the maximum power point multiplied by the number of modules connected in series (M_s). Since the inductor current ripple reaches its maximum when the duty cycle D equals 1/2. For an example of $M_s = 10$, $V_{Gpv} = 345V$, $I_{LGpv} = 4.35A$, $f_s = 50kHz$, and with an inductor current ripple $\Delta I_{LGpv} = 1\%$ of I_{LGpv}, it results the inductor value of $L_{Gpv} = 0.08H$.

The minimum inductance value required to maintain CCM is determined using either Equation (I.62) or (I.63). The calculation yields a value of $L_{Gpv\_\min} = 1.99\times10^{-4}H$.

I.7.2.4.2. Sizing of DC-DC boost converter's output capacitor

The output capacitor in a DC-DC boost converter plays a crucial role in maintaining stable and efficient operation. Its primary function is to smooth the output voltage by filtering out the ripple caused by the high-frequency switching of the boost converter's semiconductor components. During the switching cycle, especially when the switch is off (T_{OFF} period) and the inductor transfers its stored energy to the load, the output capacitor supplies current to ensure a steady voltage at the output. This helps prevent sudden voltage fluctuations during load transients and improves the converter's dynamic response. Additionally, the output capacitor acts as a low-pass filter, reducing high-frequency noise and EMI in the system. A properly sized output capacitor also supports CCM, which enhances overall converter efficiency and performance. Using equation (I.67), the value of the output capacitor C_{dc} can be determined based on the specified voltage ripple across its output, as follows:

$$C_{dc} = \frac{I_{Gpv\_moy} D(1-D)}{f_s \Delta V_{dc}} \tag{I.69}$$

The voltage ripple reaches its peak when the duty cycle D=0.5. By setting the allowable ripple ΔV_{dc} to 5% of V_{dc} , and using the values I_{Gpv}=4.35A, f_s=50 kHz, V_{Gpv}=345 V, and V_{dc}=(1−D)V_{Gpv}, the minimum required value for the output capacitor is found to be C_{dc}=6.5×10^{-7}F. For the purposes of this study, the chosen value is C_{dc}=3.5×10^{-6} F.

I.7.2.4.3. Sizing of DC-DC boost converter's input capacitor

In PV applications, the input capacitor in a DC-DC boost converter plays several essential roles. First and foremost, it acts as an energy buffer between the PVG and the boost converter. It helps to smooth out the voltage supplied by the PV panels, which can fluctuate due to changes in solar irradiance or temperature. By doing so, the input capacitor ensures a more stable voltage at the boost converter's input, which improves the overall performance and reliability of the power conversion system. Additionally, the input capacitor reduces high-frequency noise and voltage ripples caused by the fast switching of the boost converter's semiconductor components. This not only helps to protect the PV generator from stress but also minimizes EMI, which can affect other nearby electronic systems. Furthermore, by stabilizing the input voltage, the input capacitor contributes to the efficiency of the used MPPT algorithm. A more stable input allows the MPPT controller to better track and extract the maximum available power from the PV source. According to [57], the input capacitor's value can be determined using the following expression:

$$C_{Gpv} = \frac{DI_{Gpv\_moy}}{\Delta V_{Gpv} f_s} \tag{I.70}$$

In this, the PV output voltage ripple reaches its peak when the duty cycle D=0.5. By setting the allowable ripple ΔV_{Gpv} to 5% of V_{Gpv}, and using the values I_{Gpv}=4.35A, f_s=50 kHz, and V_{Gpv}=345 V, the minimum required value for the input capacitor is found to be C_{Gpv}=2.5×10^{-6}F. For the purposes of this study, the chosen value is C_{Gpv}=6.5×10^{-6} F.

I.8. Pulse Width Modulation (PWM) Principle

In DC-DC converters, the output voltage must be regulated to remain constantly equal to a desired reference voltage, due to the fact that the supply voltage and load characteristics can vary [6]. A method for regulating the output voltage to obtain a fixed average voltage consists of continuously adjusting the duty cycle D without modifying Ts. This method, which involves varying the width of the switch control pulses, is called Pulse Width Modulation (PWM) approach. The control signal for switch S must be developed by comparing the duty cycle D with a sawtooth voltage. When $D > V_{DS}$: S = 1, switch S is commanded to close (ON state). When $D < V_{DS}$: S = 0, switch S is commanded to open (OFF state).

I.9. Maximum Power Point Tracking Algorithms

Maximum Power Point Tracking (MPPT) algorithms have become popular in PVG systems to optimize the energy extraction from solar panels [58, 59]. The MPPT achieves a continuous adjustment of the aspects of the operation of the PVG system through electronic converters to ensure operation at its maximum power point (MPP). The MPP refers to the specific operating point of a solar panel where it produces the highest amount of electrical power, considering changing conditions

such as solar radiation intensity and temperature. There are many MPPT methods, each with different benefits and drawbacks. The following are many popular MPPT algorithms:

I.9.1. Perturb And Observe

The Perturb and Observe (P&O) algorithm represents a fundamental and frequently employed approach for achieving MPPT in PV systems. Its foremost advantage lies in its inherent simplicity, rendering it a cost-efficient choice for implementation [60]. The P&O method continually adjusts the operational parameters of a solar panel by perturbing its operating point and subsequently monitoring the resultant variations in power output. It proceeds in the direction of enhanced power output when such enhancement is observed, while altering the direction in the presence of power output reduction [61]. This iterative procedure facilitates its convergence toward the MPP.

Nonetheless, the P&O algorithm has certain limitations. Notably, there is a compromise concerning the step size and tracking speed [62]. An increase in step size enhances the tracking speed but causes an amplification in the ripples of the voltage close to the MPP and decreases the accuracy. Conversely, the reduced step size can decrease oscillations but slow tracking speed and increase power loss. Furthermore, tracking the maximum power point (MPP) is limited to only one direction, either during voltage increase or decrease. This constraint may lead to inaccurate monitoring and the possibility of missing the global maximum power point (GMPP) in cases where the P-V curve exhibits multiple peaks, particularly in partial shading [63]. Figure I. 33 provides the flow chart of the conventional P&O algorithm.

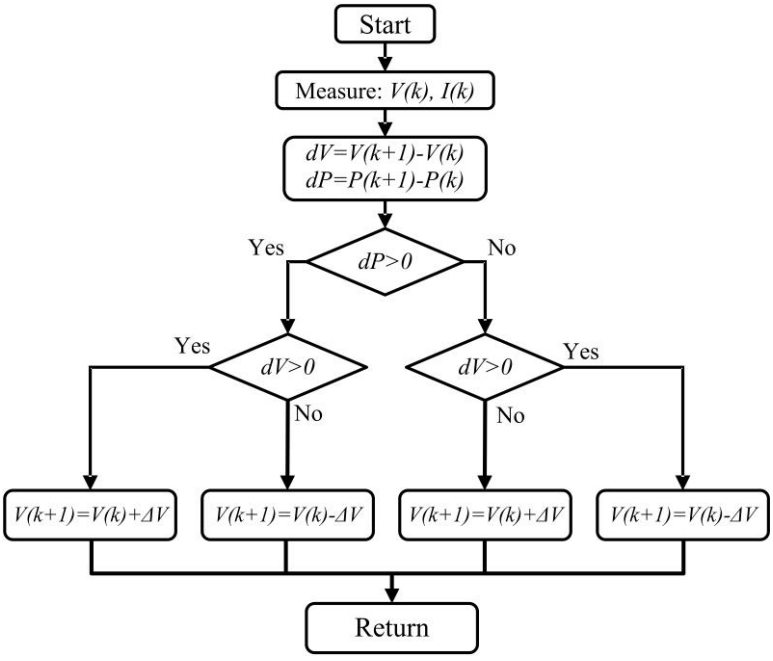


Figure I.33: Conventional P&O flow chart

Various papers have proposed enhancements to improve the performance of the P&O algorithm. Altwallbah et al. [64] present an improved adaptive P&O algorithm that effectively and precisely tracks the GMPP in partial shading conditions. The algorithm overcomes the drawbacks of conventional P&O by employing variable step sizes and appropriate comparison sequences. In [65], Taibi et al. propose a variable step size P&O algorithm, which is determined using a fuzzy logic controller. The proposed algorithm performs better than the conventional P&O during changed climatic conditions.

I.9.2. Incremental Conductance

Hussain et al. proposed the Incremental Conductance (IC) algorithm in 1995 [66]. Its functionality principle depends on the relationship between a solar panel's incremental conductance (*dI/dV*) and instantaneous conductance (I/V). By comparing these two parameters, the IC is able to track the MPP voltage across increasing or decreasing the operating voltage of the solar panel, as shown in Figure I.33Figure. The main equations express the IC algorithm given as follows:

$$\frac{dI}{dV} = -\frac{I}{V} \text{ Operating at the MPP} \tag{1.71}$$

$$\frac{dI}{dV} > -\frac{I}{V} \text{ Operating at the left side of MPP} \tag{1.72}$$

$$\frac{dI}{dV} < -\frac{I}{V} \text{ Operation at the right side of MPP} \tag{1.73}$$

The main benefits of the IC include efficiency, robustness, and ease of implementation. Nonetheless, the main criticism of the IC algorithm lies in the challenging task of the optimal step size [67, 68]. This choice involves finding a balance between the steady-state oscillation and the speed at which the system can accurately follow the desired tracking point. Moreover, the algorithm fails to track the GMPP during partial shading [69].

In this context, several papers propose improved IC algorithms to overcome the conventional IC drawbacks [70-73]. In order to tackle issues related to accuracy and tracking speed, the authors in reference [74] suggest employing an IC algorithm with variable step sizes. Their approach involves dividing the I-V curve into four distinct sections and assigning a specific step size to each section. Mahmoud et al. introduce a variable step size IC algorithm that utilizes a fuzzy logic controller to adapt the step size [72]. An IC algorithm-based particle swarm optimization (ICPSO) proposed in [73] aims to track the GMPP. The ICPSO algorithm shows a fast response and accurately tracks the GPMM during the partial shading condition.

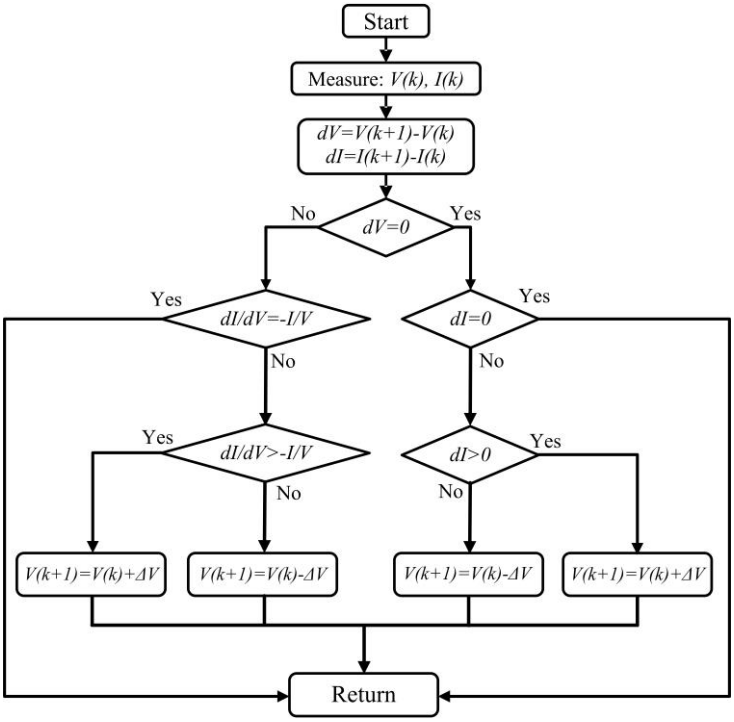


Figure I.34: The flow chart of the incremental conductance algorithm

I.9.3. Sliding Mode MPPT Algorithm

Due to its notable characteristics, the sliding mode control (SMC) is a widely used nonlinear control technique. These include fast dynamic response, robustness, system order reduction, effective disturbance rejection, and ease of implementation. In the context of PV systems, SMC is frequently employed as an MPPT algorithm in standalone and grid-connected PV systems configuration [75-78].

Yatimi and Aroudam [79] introduced a first-order sliding mode (FOSM) MPPT algorithm. It is a principle based on observing the power derivative concerning the voltage (dP/dV) equals zero at the MPP. Consequently, they select the sliding surface to force the system output to reach zero and optimize the power output. However, the first-order SMC suffers from the chattering phenomena, which causes an oscillation around the MPP [80], as shown in the example in Figure I.35.

In order to mitigate the drawback of FOSM, several papers propose a high-order sliding mode (HOSM) [77, 78]. Kantas et al. suggest a third-order sliding mode control (TOSM) for harvesting the MPP applied on a standalone PV system [78]. The results show the TOSM algorithm's superiority over the conventional FOSM in terms of maximum power output, reduced chattering, accuracy, and less fluctuation in the voltage and current.

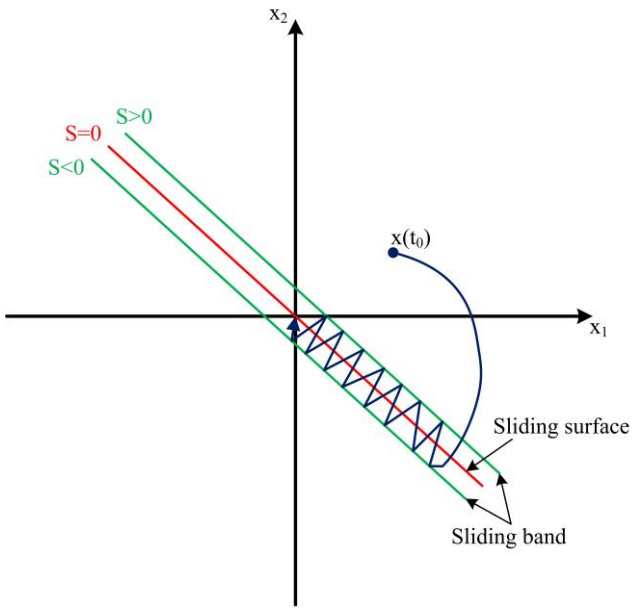


Figure I.35: Phase portrait of a first-order sliding mode controller

I.9.4. Artificial Neural Network MPPT

Artificial neural networks (ANNs) are promising techniques that draw inspiration from the human brain's structure and operation. Recently, ANN has become an attractive solution adopted in PV systems [81]. It effectively addresses the limitations of the conventional iterative MPPT algorithm, including slow tracking speed, oscillation around the MPP, and accuracy tracking it during rapidly changing weather conditions or partial shading [82-84]. The MPPT based on ANNs provides the V_{MPP} at its output. At the same time, various papers use different parameters in the input, such as PV voltage and current, temperature, irradiance, open circuit voltage, short circuit current, or a combination thereof [85-87].

However, the training of ANNs necessitates an extensive amount of data, which may not be accessible or accurate for some PV systems [81]. Moreover, ANNs can show poor performance during extreme conditions or noisy input. In addition, high computational costs and memory requirements may increase the implementation cost. Figure I.36 shows an example of the structure of ANNs-based MPPT with two inputs (irradiance and temperature), one hidden layer, and one output (V_{MPP}).

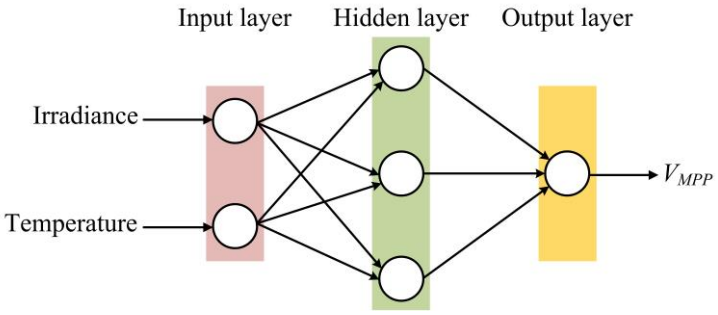


Figure I.36: Example of the structure of ANNs-based MPPT

I.9.5. Fuzzy Logic Controller

Fuzzy logic (FL) is an extension of artificial intelligence specifically designed to manage inaccuracy and uncertainty by applying linguistic rules and fuzzy sets. The FL comprises three

fundamental steps [88], as depicted in Figure I. 37. The first step is fuzzification, which converts the real input values into linguistic terms through the membership function. The second step is the inference process, which applies the fuzzy rules to the fuzzified inputs and obtains the fuzzy output. The last step is defuzzification, which converts the fuzzy output values into real output values using the membership function defined for each output.

Fuzzy MPPT [89] adjusts the PV system's duty cycle or voltage to generate the peak power output in response to changing environmental factors such as temperature and solar irradiance. Unlike other MPPT techniques, fuzzy MPPT provides several benefits, including simplicity, robustness, fast convergence, and low oscillation [72].

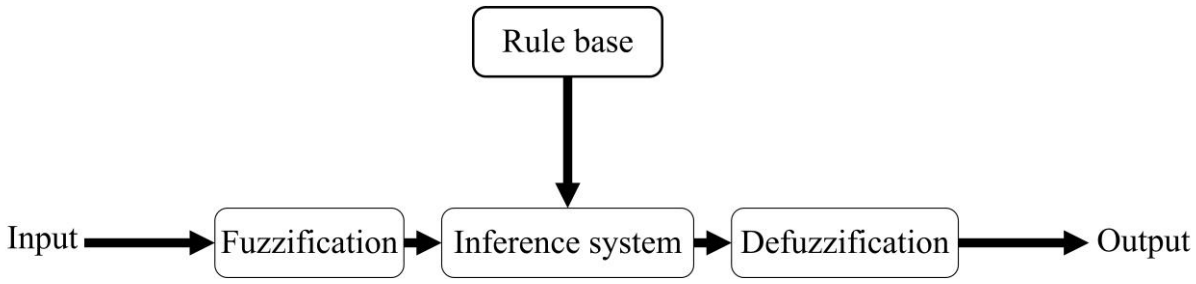


Figure I.37: Fuzzy logic controller's block diagram

I.9.6. Meta-Heuristic and Bio-Inspired Techniques

Meta-heuristic and bio-inspired techniques are optimization methods used to track the MPP. These are practical solutions to track the GMPP under partial shading conditions. In this context, various MPPT algorithms inspired by nature, such as Particle swarm optimization [90], Genetic Algorithm [91], Grey wolves optimization [92], Ant colony optimization (ACO) [93], Artificial bee colony (ABC) [94], Cuckoo Search (CS) [95].

Particle swarm optimization (PSO) is an optimization technique developed in 1995 by Kennedy and Eberhart [96]. They were inspired by the collective behavior of bird flocking and the schooling activities of fish. PSO allows the PV system to operate at the GMPP among all the MPPs, particularly when they encounter challenges such as partial shading or multiple peaks in the P-V curve [97].

PSO utilizes a population of possible solutions represented as particles. These particles can take the form of duty cycles or PV voltages. Each particle has two fundamental properties: position and velocity. The particle properties are updated in each iteration based on the particle's best position and the swarm's global best position, and some random elements are introduced. Figure I.38Figure shows the process of particle movement toward the best solution.

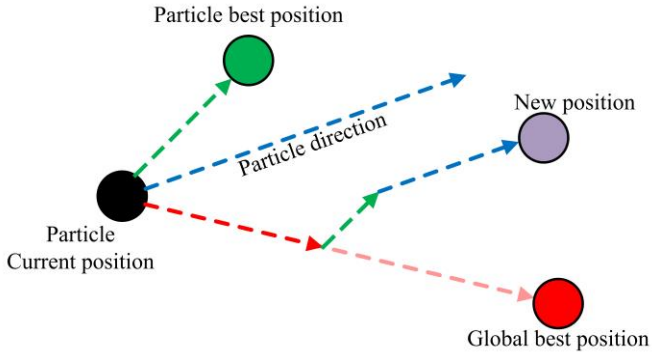


Figure I.38: Particle swarm optimization algorithm

The genetic algorithm (GA) is an optimization algorithm that mimics the process of natural evolution (Figure I.39); its fundamental principle involves the creation and improvement of a population of possible solutions, guided using rules inspired by biology [98]. The main steps in the GA include initialization, evaluation, selection, crossover, mutation, and replacement [99].

Initially, the GA generates a random population, represented in binary form (in our case, this relates to PV voltage levels). Each binary element of the individual is called a gene. The evaluation step is pivotal, as it guarantees the survival of the fittest individual within the population. In this stage, the entire population is evaluated using a fitness function, which, in our context, aims to maximize power output. The selection process follows, where individuals are picked based on probability, and the fittest individuals closer to the optimal solutions have a greater chance of being selected. Subsequently, the crossover procedure creates new individuals by combining several of the selected parent's genes. Finally, the generation update is done using the replacement process, which uses techniques such as elitism (preserving the best individuals), generational (replacing all individuals), or steady-state (replacing few individuals). This process continues iteratively until a specific stopping condition is satisfied. Common stopping criteria include reaching a predefined maximum number of iterations or discovering an optimal solution.

The MPPT based on GA performs better than the conventional algorithm, especially during partial shading conditions [91].

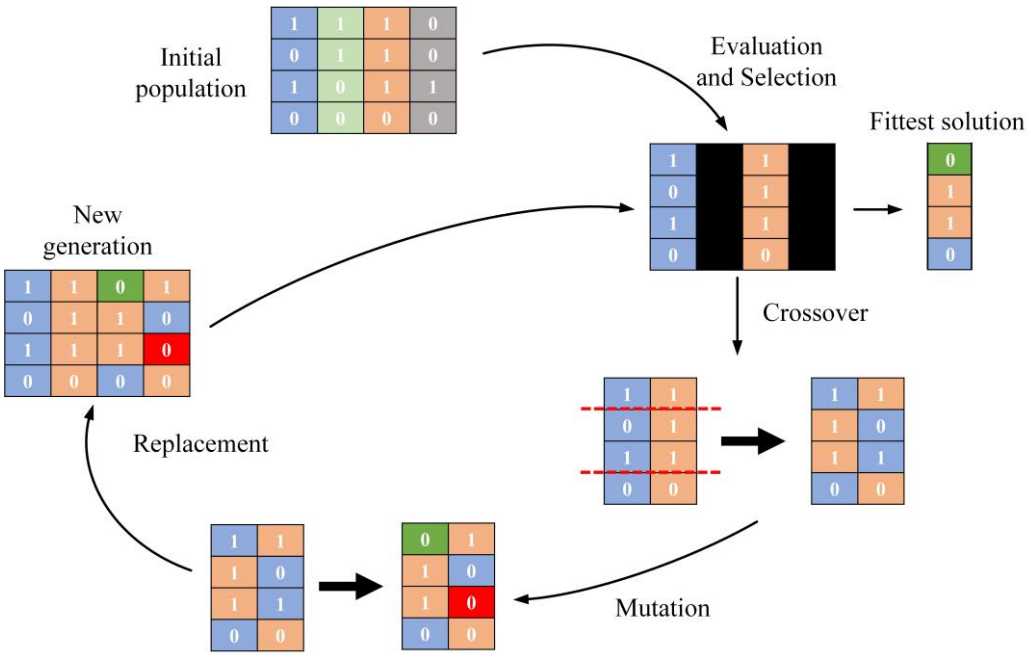


Figure I.39: The main steps of the genetic algorithm

The Grey Wolf Optimizer (GWO) is an optimization algorithm designed to emulate the hierarchical leadership structure and hunting behavior of grey wolves (Canis lupus) proposed by Mirjalili et al. in 2014 [100]. The GWO algorithm contains four different types of wolves, each possessing unique roles inside the pack. The alpha wolf is the dominant leader of the pack, and it is the best solution to the optimization problem. In contrast, the beta wolf is the subordinate of the alpha wolf, and its value presents the second-best solution. The delta (δ) is the third class in the pack and presents the third-best solution. The remaining candidate solutions are the omega (ω) wolves. The

wolves exhibit cooperative behavior by effectively coordinating their actions to hunt their prey. The hunting process guides the alpha, beta, and delta, while the remaining omega wolves follow those three wolves.

In the GWO algorithm, three mathematical models emulate the hunting behaviors of wolves: encircling the prey, hunting the prey, and attacking the prey [101]. The alpha, beta, and delta wolves change their location using the encircling behavior based on the best solution discovered. The utilization of hunting behavior determines the calculation of the distance between each wolf and the prey. The attack behavior is employed to modify the position of each wolf by directing their movement towards the prey, utilizing a random coefficient.

Several papers propose an MPPT algorithm based on GWO to gather the GMPP of a PV system under partial shading. The technique performs better than conventional methods such as P&O, IC, PSO, and GA [102, 103].

I.10. Linear Control of the Boost Converter

The MPPT techniques have been introduced to determine the reference voltage at each instant of current and voltage measurement at the output of the PVG, as illustrated in Figure I.40. This reference voltage allows the PVG to operate at the maximum power point.

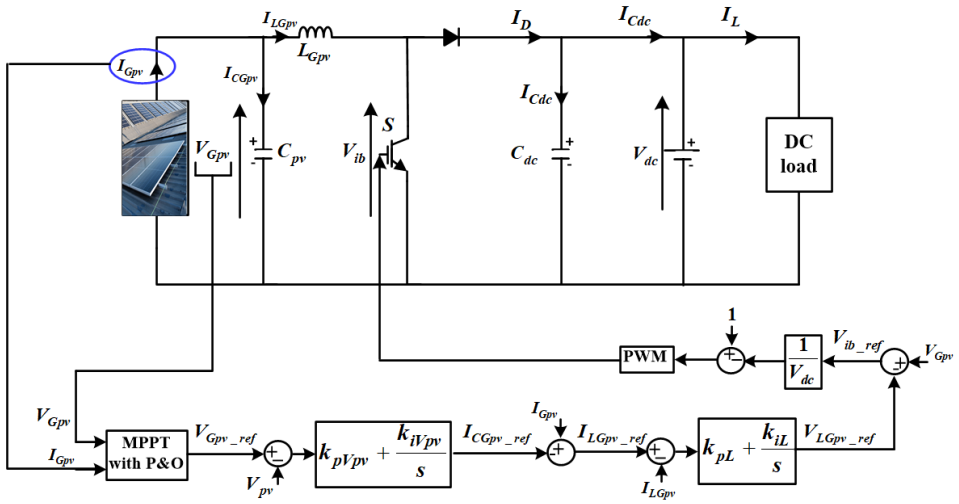


Figure I.40: Schematic diagram of the PI control of DC-DC boost converter-based standalone power supply system.

The figure shows a boost converter with a PV (photovoltaic) array input and a detailed control scheme. The upper part shows the power circuit of the boost converter with:

- PVG on the left side
- DC-DC boost converter's input capacitor (C_{Gpv})
- DC-DC boost converter's input Inductor (L_{Gpv})
- DC-DC boost converter's power switch (S), likely an IGBT or MOSFET
- Diode D_{pv}
- DC-DC boost converter's output capacitor (C_{dc})

The lower part shows the cascaded control system with:

1. **MPPT Controller**: Takes V_{Gpv} and I_{Gpv} as inputs to outputs the reference voltage (V_{Gpv_ref}) used in the Outer Voltage Control Loop and to operate at MPP
2. **Outer Voltage Control Loop** : Compares PVG output voltage reference (V_{Gpv_ref}) with actual V_{Gpv} using PI controller to outputs the DC-DC boost converter's input inductor current reference (I_{LGpv_ref}).
3. **Inner Current Control Loop**: Compares DC-DC boost converter's input inductor current reference I_{LGpv_ref} with actual current I_{LGpv} using PI controller to outputs the input inductor drop voltage reference (V_{LGpv_ref}) used in the determination of the PWM modulation voltage reference V_{m_ref} after the compensation of the PVG output voltage disturbances (V_{Gpv}).
4. **PWM Generation**: The final modulation voltage reference is compared with a carrier signal to generates PWM switching signals for the power switch (S).

This is a typical cascaded control structure for PV systems with:

- Outer loop: MPPT tracking and voltage regulation;
- Inner loop: Current control for fast dynamic response;
- PWM generator: Converts control signals to switch commands.

The dual-loop control approach provides:

- Better dynamic performance ;
- Stable operation across various conditions ;
- Protection against overcurrents ;
- Ability to track the maximum power point of the PV array.

The control system uses feedback from both voltage and current sensors to continuously adjust the duty cycle (D) of the boost converter to maintain optimal operation regardless of changes in irradiance or load conditions.

I.10.1. Synthesis of the PI controller for the PVG output voltage

The PI controller for the PVG output voltage in the outer voltage control loop serves several critical functions within the DC-DC boost converter's control system. It precisely regulates the PVG output voltage (V_{Gpv}) to match its reference (V_{Gpv_ref}) determined by the MPPT algorithm, ensuring optimal power extraction from the PVG. By processing the error between the reference and actual measured PVG output voltage, it continuously works to minimize this difference while generating the reference current (I_{LGpv_ref}) needed for the regulation of the input inductor current in the inner current control loop. This controller enhances system stability and dynamic response during changing environmental conditions or load variations, effectively rejecting disturbances that might affect the PVG output voltage. The proportional component provides immediate response to changes, while the integral component eliminates steady-state errors, collectively ensuring that the PVG system consistently operates at its MPP for optimal energy harvesting efficiency.

According to (18), and by applying Kirchhoff's laws to the equivalent schematic diagram in Figure I.40, we derive the dynamics of both the PV output voltage (V_{Gpv}) and input inductor current (I_{LGpv}) as follows:

$$\frac{dV_{Gpv}}{dt} = \frac{1}{C_{Gpv}} I_{CGpv} = \frac{1}{C_{Gpv}} \left(I_{Gpv} - I_{LGpv}\right) \quad \text{(I.74)}$$

$$\frac{dI_{LGpv}}{dt} = \frac{1}{L_{Gpv}} \left(V_{Gpv} - V_{dc} + SV_{dc}\right) \quad \text{(I.75)}$$

Figure I.41 illustrates the PVG's output voltage regulation loop implemented using a PI controller.

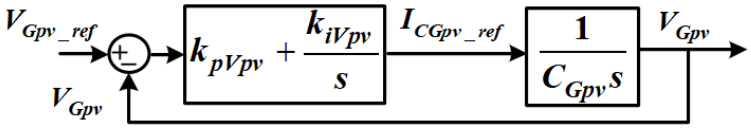


Figure. I. 41: Schematic diagram of the PI-based PVG output voltage regulation

Based on the diagram in Figure I.41 and using the poles placement method, the gain k_{pVpv} and k_{iVpv} are given by:

$$\begin{cases} k_{pVpv} = 2\xi_{Vpv}\omega_{nVpv}C_{Gpv} \\ k_{iVpv} = C_{Gpv}\omega_{nVpv}^2 \end{cases} \quad \text{(I.76)}$$

where ξ_{Vpv} and ω_{nVpv} represent the damping factor and the natural frequency of the PVG output voltage system, respectively

I.10.2. Synthesis of the PI controller for input inductor current

In a DC-DC boost converter-based PVG system, the regulation of the DC-DC boost converter's input inductor current using PI controller plays a critical role, which is essential for maintaining stable and efficient operation. One of its primary functions is to ensure that the inductor current accurately tracks a reference value typically generated by the regulation of the PVG output voltage, thereby allowing the system to extract the maximum available power from the PV array under varying environmental conditions. This regulation also stabilizes the input current dynamics, minimizing fluctuations caused by changes in irradiance, temperature, or load. This stabilization helps preserve CCM, which is desirable for reducing current ripple and improving efficiency. Additionally, the regulation of the DC-DC boost converter input inductor current enhances the system's dynamic response, with the proportional term providing fast correction of errors and the integral term eliminating steady-state errors. This precise regulation not only contributes to improved energy conversion efficiency but also protects system components by preventing overcurrent conditions. Overall, the PI controller is a key element in ensuring the reliable and optimal performance of PVG systems using DC-DC boost converters.

Figure I.42 illustrates the DC-DC boost converter's input inductor current regulation loop implemented using a PI controller.

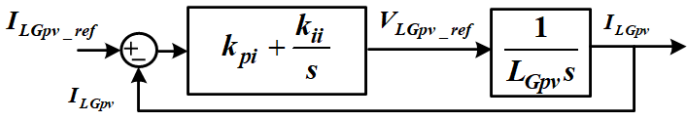


Figure. I. 42: Schematic diagram of the PI-based DC-DC boost converter's input inductor current regulation

Based on the diagram in Figure I.42 and using the poles placement method, the gain k_{pi} and k_{ii} are given by:

$$\begin{cases} k_{pi} = 2\xi_{ipv}\omega_{nipv}L_{Gpv} \\ k_{ii} = L_b\omega_{ipv}^2 \end{cases} \quad \text{(I.77)}$$

where ξ_{ipv} and ω_{nipv} represent the damping factor and the natural frequency of the DC-DC boost converter's input inductor system, respectively

I.11. Conclusion

This chapter provided a comprehensive overview of photovoltaic (PV) systems and their role in grid-connected power applications aimed at improving energy quality and sustainability. It began by emphasizing the importance of renewable energy sources, particularly solar energy, as a clean and inexhaustible alternative to fossil fuels. The fundamental principles of semiconductor physics and the operation of the PN junction were reviewed to explain how photovoltaic cells convert solar radiation into electrical energy.

Various types of PV technologies, monocrystalline, polycrystalline, thin-film, and emerging generations such as perovskite and organic cells, were analyzed in terms of their structure, performance, and efficiency evolution. Mathematical models of PV cells and modules, including single- and two-diode equivalent circuits, were presented to describe the nonlinear I–V characteristics under different operating conditions of irradiance and temperature.

The chapter also discussed the influence of factors such as series resistance, temperature, and partial shading on PV module performance. To achieve higher output power, the configuration of PV cells into modules, strings, and arrays was detailed, along with the modeling of photovoltaic generators (PVGs). Furthermore, the integration of DC-DC converters, particularly the boost converter, was introduced as a key element in adapting PV voltage and ensuring maximum power transfer to the load.

Finally, the importance of Maximum Power Point Tracking (MPPT) algorithms, such as Perturb and Observe, Incremental Conductance, Sliding Mode, Fuzzy Logic, Artificial Neural Networks, and bio-inspired optimization methods, was highlighted. These algorithms play a critical role in maximizing energy extraction efficiency under varying environmental conditions. The chapter concluded by presenting the linear control approach based on PI regulators for voltage and current control, forming the foundation for advanced control strategies in subsequent chapters.

While this chapter has focused on the standalone PVG system interfaced with a DC-DC boost converter for optimal power extraction under varying environmental conditions, practical grid-connected applications require an additional power conversion stage to enable seamless integration with the utility network. In grid-connected PV systems, a DC-AC inverter serves as the critical interface that converts the DC power from the PVG into AC power compatible with the electrical grid. Traditional three-leg voltage source inverters (VSIs), though widely used due to their simplicity and cost-effectiveness, exhibit inherent limitations when interfacing with three-phase four-wire distribution systems that include a neutral conductor. These limitations become particularly evident when the system must handle unbalanced loads, supply single-phase loads, manage zero-sequence currents, or provide harmonic compensation and reactive power support under nonlinear loading conditions. To address these challenges and enhance power quality in modern distribution networks where mixed residential and commercial loads are prevalent, four-leg inverter (4LI) topologies have emerged as a superior alternative. The fourth leg, connected to the system neutral point, enables

independent control of the neutral voltage, allowing the inverter to effectively manage unbalanced conditions, inject or absorb neutral current, actively compensate for harmonic distortion, and provide flexible reactive power support. These capabilities make the 4LI particularly suitable for grid-connected PV systems operating in low-voltage distribution networks characterized by phase imbalances, nonlinear single-phase loads, and stringent power quality requirements. Therefore, the next chapter will present a comprehensive study of the modeling, control strategies, and performance evaluation of a PVG grid-connected four-leg inverter system, focusing on its dual operational modes: combined harmonic mitigation and reactive power compensation under nonlinear single-phase loads, and dedicated reactive power compensation under linear three-phase loads, thereby establishing the foundation for enhanced grid integration and improved power quality delivery.

Chapter 2

Modeling and control of PVG grid connected four leg inverter system

II.1. Introduction

Due to the growing need for electrical energy and increasing environmental concerns (pollution, greenhouse gas emissions, nuclear energy exploitation risks), decentralized renewable energy production is gaining significant importance worldwide. PVG energy has become one of the most promising energy sources due to its numerous advantages (no fuel cost, simple maintenance, conversion without moving parts, and noise-free operation). However, PVG energy is known for its intermittency, relatively low conversion efficiency, and non-linear electrical characteristics. For this reason, power converters have become essential for exploiting PV energy. Today, decentralized PVG production systems have become one of the most widespread applications.

A decentralized PV system is typically composed of two conversion stages. The first stage is a DC-DC converter, often of the boost type, responsible for forcing the PV generator to operate at its maximum power point and increasing its DC output voltage. The second stage is a DC-AC converter, usually a voltage inverter, enabling connection to the distribution grid. Nevertheless, the DC-AC conversion must comply with standard norms (voltage, frequency, power factor, energy injection quality, IEEE 519-2 Standard). Moreover, the system control must also ensure robustness against disturbances such as climate condition variations and load changes.

In grid-connected PVG systems, inverters serve as the essential interface that converts the DC output of solar panels into AC power compatible with utility networks. Traditionally, three-leg voltage source inverters (VSIs) have been widely used in three-phase PV systems due to their simplicity, cost-effectiveness, and well-established control strategies. However, these inverters are inherently limited when it comes to handling unbalanced and nonlinear loads or interfacing with four-wire distribution systems that include a neutral conductor.

To overcome these limitations, four-leg inverters (4LIs) have emerged as an advanced alternative. The fourth leg, connected to the system neutral, allows the inverter to independently control the neutral point voltage, enabling precise handling of unbalanced loads, zero-sequence currents, and harmonic compensation. This feature makes 4LIs particularly suitable for grid-connected PV systems supplying mixed or residential loads, where phase imbalances and harmonics are common.

Compared to three-leg inverters, four-leg configurations offer several key advantages [16], [131]:

Neutral Current Management: 4LIs can inject or absorb neutral current, effectively mitigating the impact of unbalanced loads and improving power quality.

Enhanced Power Quality: By actively compensating for zero-sequence and harmonic components, 4LIs reduce total harmonic distortion (THD) and improve voltage and current waveform quality.

Improved Reliability in Four-Wire Systems: Their ability to provide a stable neutral point makes them ideal for interfacing with standard low-voltage distribution networks.

Advanced Control Flexibility: With the added leg, control algorithms can be extended to manage asymmetrical voltage sags/swells, islanding scenarios, and fault ride-through conditions more effectively.

II.2. Modeling and operating principle of the 4LI [133]

II.2.1. Operating principle of the 4LI

The three-phase 4LI is composed of eight bidirectional current switches, as shown in Figure II.1. These switches are implemented using controllable semiconductors (typically IGBTs) connected in anti-parallel with a diode. This configuration prevents a short circuit of the DC source at the input of the inverter or the disconnection of the AC load at the output.

For this structure, the following constraints must be respected:

- At any given time, only one switch in the same leg should conduct to avoid a short circuit of the voltage source.
- The line current must always have a possible path, hence the anti-parallel diode configuration for the switches.

II.2.1.1. Output voltages of the 4LI

The switches in each leg of the 4LI operate in a complementary manner. Specifically, when the upper switch in a leg is conducting, the lower switch is blocked (the upper switch is "closed" and the lower switch is "open".

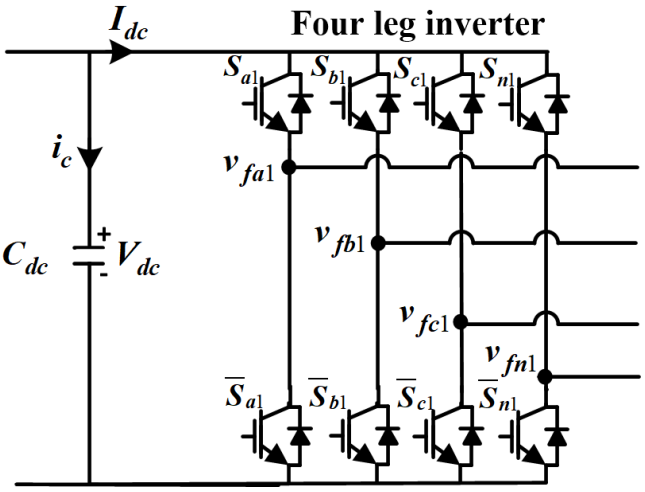


Figure II.1: Circuit of the three-phase 4LI.

The switching functions, representing the states of the upper switches of the inverter, are denoted as S. A value of 1 indicates that the corresponding switch is closed, and a value of 0 indicates that it is open.

$$F_j = \begin{cases} 1 \text{ if } T_j \text{ is closed} \\ 0 \text{ if } T_j \text{ is open} \end{cases}$$

The switching states for the 4LI in Figure II.1 are presented in Table II.1. These states are derived using the following expressions:

The output voltages (v_{1o}, v_{2o}, v_{3o}, v_{no}) relative to the reference of the DC source (o) can be expressed as:

$$\begin{cases} v_{f1o} = v_{f1} = F_1.V_{dc} \\ v_{f2o} = v_{f2} = F_2.V_{dc} \\ v_{f3o} = v_{f3} = F_3.V_{dc} \\ v_{fno} = v_{fn} = F_4.V_{dc} \end{cases} \quad \text{(II.1)}$$

Where V_{dc} is the DC supply voltage of the inverter and F_j represents the switching state.

The three-phase output voltages (v_{f1}, v_{f2}, v_{f3}) relative to the neutral point (n) can be expressed as:

$$\begin{cases} v_{f1n} = v_{1o} - v_{no} = (F_1 - F_4)V_{dc} \\ v_{f2n} = v_{2o} - v_{no} = (F_2 - F_4)V_{dc} \\ v_{f3n} = v_{3o} - v_{no} = (F_3 - F_4)V_{dc} \end{cases} \quad \text{(II.2)}$$

The line-to-line voltages (v_{12}, v_{23}, v_{31}) between the phases are given by:

$$\begin{cases} v_{12} = v_{1o} - v_{2o} = (F_1 - F_2)V_{dc} \\ v_{23} = v_{2o} - v_{3o} = (F_2 - F_3)V_{dc} \\ v_{31} = v_{3o} - v_{1o} = (F_3 - F_1)V_{dc} \end{cases} \quad \text{(II.3)}$$

The DC input current of the inverter is expressed as:

$$i_{dc} = F_1 i_{f1} + F_2 i_{f2} + F_3 i_{f3} - F_4 i_{fn} \quad \text{(II.4)}$$

Voltage Vectors	Switching State				The output voltages in the abc reference frame		
	F_1	F_2	F_3	F_4	v_{f1}	v_{f2}	v_{f3}
v_0	0	0	0	0	0	0	0
v_1	1	0	0	0	V_{dc}	0	0
v_2	0	1	0	0	0	V_{dc}	0
v_3	1	1	0	0	V_{dc}	V_{dc}	0
v_4	0	0	1	0	0	0	V_{dc}
v_5	1	0	1	0	V_{dc}	0	V_{dc}
v_6	0	1	1	0	0	V_{dc}	V_{dc}
v_7	1	1	1	0	V_{dc}	V_{dc}	V_{dc}
v_8	0	0	0	1	$-V_{dc}$	$-V_{dc}$	$-V_{dc}$
v_9	1	0	0	1	0	$-V_{dc}$	$-Vdc$
v_{10}	0	1	0	1	$-V_{dc}$	0	$-V_{dc}$
v_{11}	1	1	0	1	0	0	$-V_{dc}$
v_{12}	0	0	1	1	$-V_{dc}$	$-V_{dc}$	0
v_{13}	1	0	1	1	0	$-V_{dc}$	0
v_{14}	0	1	1	1	$-V_{dc}$	0	0
v_{15}	1	1	1	1	0	0	0

Table II.1 Switching states and corresponding voltage vectors in the abc reference frame

II.2.1.2 Representation Vectorial of the 4LI

Considering the vector $\vec{v}_f$ corresponding to the voltages of the 4LI, the 16 possible cases of the vector $\vec{v}_f$, after transformation into the (αβ0) reference frame, are shown in Figure II.2. The voltage vector $\vec{v}_f$ of the 4LI is represented by:

$$\vec{v}_f = v_{f\alpha}\vec{i} + v_{f\beta}\vec{j} + v_{fo}\vec{k} \quad \text{(II.5)}$$

Where $v_{f\alpha}, v_{f\beta}$ and v_{fo} are the projections of the vector in the (αβ0) reference frame. This gives:

$$\begin{bmatrix} v_{f\alpha} \\ v_{f\beta} \\ v_{f0} \end{bmatrix} = \sqrt{\frac{2}{3}} v_{dc} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_{f1} \\ v_{f2} \\ v_{f3} \end{bmatrix} \quad \text{(II.6)}$$

The switching states of the 4LI in the αβ0 frame are presented in Table II.2.

Voltage Vectors	***Commutation states***				***The output voltages in the αβ0 reference frame***		
	F_1	F_2	F_3	F_4	$v_{f\alpha}$	$v_{f\beta}$	v_{f0}
v_0	0	0	0	0	0	0	0
v_1	0	0	0	1	0	0	$-3V_{dc}/\sqrt{3}$
v_2	0	0	1	0	$-V_{dc}/\sqrt{6}$	$-V_{dc}\sqrt{2}/2$	$V_{dc}/\sqrt{3}$
v_3	0	0	1	1	$-V_{dc}/\sqrt{6}$	$-V_{dc}\sqrt{2}/2$	$-2V_{dc}/\sqrt{3}$
v_4	0	1	0	0	$-V_{dc}/\sqrt{6}$	$V_{dc}\sqrt{2}/2$	$V_{dc}/\sqrt{3}$
v_5	0	1	0	1	$-V_{dc}/\sqrt{6}$	$V_{dc}\sqrt{2}/2$	$-2V_{dc}/\sqrt{3}$
v_6	0	1	1	0	$-V_{dc}\sqrt{2}/\sqrt{3}$	0	$2V_{dc}/\sqrt{3}$
v_7	0	1	1	1	$-V_{dc}\sqrt{2}/\sqrt{3}$	0	$-V_{dc}/\sqrt{3}$
v_8	1	0	0	0	$V_{dc}\sqrt{2}/\sqrt{3}$	0	$V_{dc}/\sqrt{3}$
v_9	1	0	0	1	$V_{dc}\sqrt{2}/\sqrt{3}$	0	$-2V_{dc}/\sqrt{3}$
v_{10}	1	0	1	0	$V_{dc}/\sqrt{6}$	$-V_{dc}\sqrt{2}/2$	$2V_{dc}/\sqrt{3}$
v_{11}	1	0	1	1	$V_{dc}/\sqrt{6}$	$-V_{dc}\sqrt{2}/2$	$-V_{dc}/\sqrt{3}$
v_{12}	1	1	0	0	$V_{dc}/\sqrt{6}$	$V_{dc}\sqrt{2}/2$	$2V_{dc}/\sqrt{3}$
v_{13}	1	1	0	1	$V_{dc}/\sqrt{6}$	$V_{dc}\sqrt{2}/2$	$-V_{dc}/\sqrt{3}$
v_{14}	1	1	1	0	0	0	$3V_{dc}/\sqrt{3}$
v_{15}	1	1	1	1	0	0	0

Table II.2 Switching states and corresponding voltage vectors in the (αβ0) reference frame

Table 2.2 presents, for each combination of variables T_1, T_2, T_3, and T_4, the corresponding voltage vector in the αβ0 frame. Since these variables are binary for the 4LI, there are 24 = 16 different phase level sequences. The table illustrates the correspondence between each phase level sequence and the voltage vector. Notably, two different phase level sequences (0, 0, 0, 0) and (1, 1, 1, 1) generate the same null voltage vector. The complete set of voltage vectors produced by a 4LI is represented by a hexagonal prism, as shown in Figure II.2.

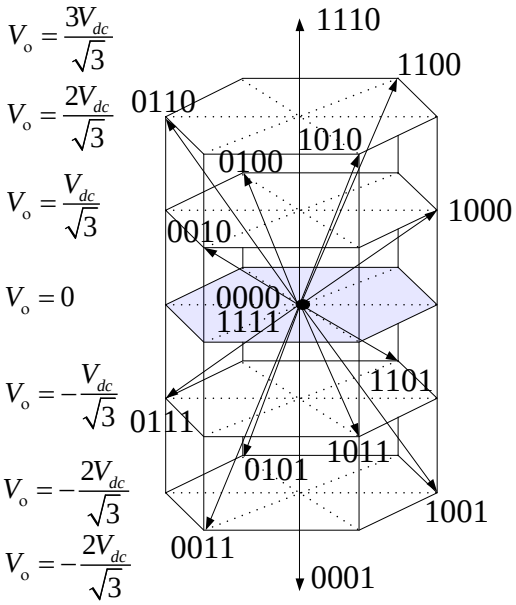


Figure II.2: Vectorial representation of the 4LI output voltages.

II.3. Description and Modeling of a PVG Grid-Connected 4LI

The integration of PVG systems into modern power grids is increasingly essential for enhancing sustainability and energy efficiency. Among the various topologies used for grid interfacing, the 4LI has gained significant attention, particularly in low-voltage, three-phase four-wire systems. This topology not only facilitates the injection of active power generated by PV panels but also enhances power quality by addressing issues commonly encountered in practical load conditions [7].

When supplying nonlinear loads, which are known to introduce current harmonics and degrade power quality, the PV grid-connected 4LI can operate as both a harmonic filter and a reactive power compensator. In this dual-function mode, it ensures that the grid current remains sinusoidal and within acceptable harmonic limits while also supporting reactive power compensation to maintain voltage stability.

Conversely, under linear load conditions, the primary concern shifts from harmonic distortion to reactive power flow. In such cases, the 4LI primarily functions as a reactive power compensator, contributing to power factor correction and voltage regulation without the need for harmonic filtering. The schematic diagram of the PVG grid connected 4LI is shown in Figure II.3 [132, 133].

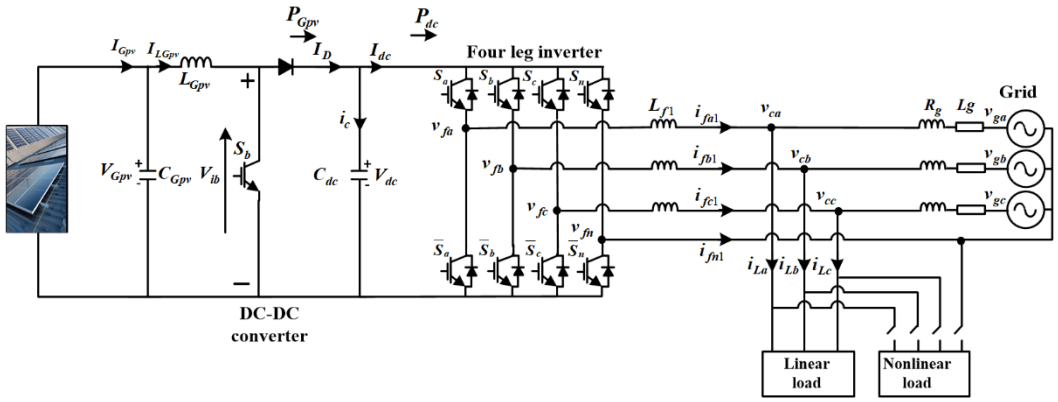


Figure II.3: Schematic diagram of the PVG grid connected 4LI.

II.3.1. Modelling of the PVG grid connected 4LI

II.3.1.1. Model of the PVG

The detailed descriptions of the PVG model and the DC-DC boost converter model can be found in Sections (I.5.1.1) and (I.5.1.2).

II.3.1.2. Model of the grid connected 4LI

In this section, we present the dynamic models of both side of the 4LI, the dynamic model of the AC side (output currents) and the dynamic model of the DC side (input DC voltage). These dynamics are essential in the synthesising the control of the grid connected 4LI.

II.3.1.1.1. Four leg inverter output current dynamics

A- Current dynamics in the three-phase (abc) reference frame [131]

Determining the grid current dynamics is essential in the control of PV grid-connected inverters, as it directly influences the system's ability to deliver stable and high-quality power. Accurate knowledge of current dynamics enables precise tracking of reference currents, which represent the desired active and reactive power exchange with the grid. This is crucial for maintaining system stability, achieving fast dynamic response, and ensuring compliance with grid codes. Furthermore, it allows for effective mitigation of power quality issues such as current harmonics and unbalanced loads, particularly when the inverter operates as a harmonic filter or reactive power compensator. An accurate dynamic model also supports advanced control strategies, such as predictive, adaptive, or model-based controllers by providing the necessary foundation for optimizing inverter performance under varying operating conditions. Overall, understanding grid current dynamics is a key requirement for designing robust control systems capable of ensuring efficient and reliable integration of PV systems into the grid. The basic schematic used for this modeling is shown in Figure II.3. By applying Kirchhoff's law to the AC side of the system, the dynamic models of the grid currents in the stationary three-phase (abc) reference frame can be expressed as follows:

$$\begin{cases} \dfrac{di_{fa}}{dt} = \dfrac{v_{fa}}{L_f} - \dfrac{v_{ca}}{L_f} \\ \dfrac{di_{fb}}{dt} = \dfrac{v_{fb}}{L_f} - \dfrac{v_{cb}}{L_f} \\ \dfrac{di_{fc}}{dt} = \dfrac{v_{fc}}{L_f} - \dfrac{v_{cc}}{L_f} \end{cases} \quad \text{(II.7)}$$

Here, v_{ca}, v_{cb} and v_{cc} denote the voltages at the point of common coupling (PCC), while i_{fa}, i_{fb}, and i_{fc}, along with v_{fa}, v_{fb}, and v_{fc}, correspond to the currents and voltages on the AC side of the 4LI, respectively.

B- Current dynamics in the stationary frame (αβo)

By applying the direct Concordia transformation as defined in Equations (II.8) and (II.9) into the system of Equations (II.7), the three-phase reference frame can be converted into the stationary αβo frame. The mathematical representation of the four-leg active power filter in the αβo stationary frame is then expressed as in Equation (II.10): [131]

• ***For the current equations:***

$$\begin{bmatrix} i_{f\alpha} \\ i_{f\beta} \\ i_{fo} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \cdot \begin{bmatrix} i_{f1} \\ i_{f2} \\ i_{f3} \end{bmatrix} \quad \text{(II.8)}$$

• ***For the PCC voltage equations:***

$$\begin{bmatrix} v_{c\alpha} \\ v_{c\beta} \\ v_{co} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \cdot \begin{bmatrix} v_{c1} \\ v_{c2} \\ v_{c3} \end{bmatrix} \quad \text{(II.9)}$$

Using equations (II.7) and (II.8), we obtain the 4LI output current dynamics as follows:

$$\begin{cases} \dfrac{di_{f\alpha}}{dt} = \dfrac{v_{f\alpha}}{L_f} - \dfrac{v_{c\alpha}}{L_f} \\ \dfrac{di_{f\beta}}{dt} = \dfrac{v_{f\beta}}{L_f} - \dfrac{v_{c\beta}}{L_f} \\ \dfrac{di_{f0}}{dt} = \dfrac{v_{f0}}{L_f} - \dfrac{v_{c0}}{L_f} \end{cases} \quad \text{(II.10)}$$

C- Current dynamics in thesynchronous Reference Frame

The rotating reference frame (dq0) is derived by applying a rotational transformation to the stationary frame (αβo) through an angle ωt, where ω represents the angular frequency of the gride voltages. This transformation, known as the Park transform and defined by Equation (II.11), converts sinusoidal variables oscillating at the same angular frequency into steady values within the new frame. Additionally, in this reference frame, the d- and q-axis components are directly associated with the flow of active and reactive power in the system. The dynamic models of the 4LI output currents in the synchronous reference frame (dq0) are expressed as in Equation (II.12).

$$\begin{bmatrix} x_d \\ x_q \\ x_o \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) & 0 \\ -\sin(\omega t) & \cos(\omega t) & 0 \\ 0 & 0 & 1 \end{bmatrix} . \begin{bmatrix} x_\alpha \\ x_\beta \\ x_o \end{bmatrix} \tag{II.11}$$

$$\begin{cases} \dfrac{di_{fd}}{dt} = \dfrac{v_{fd}}{L_f} - \dfrac{v_{cd}}{L_f} - \omega i_{fq} \\ \dfrac{di_{fq}}{dt} = \dfrac{v_{fq}}{L_f} - \dfrac{v_{cq}}{L_f} + \omega i_{fd} \\ \dfrac{di_{f0}}{dt} = \dfrac{v_{f0}}{L_f} - \dfrac{v_{c0}}{L_f} \end{cases} \tag{II.12}$$

where v_{fdq0}, v_{cdq0} and i_{fdq0} are the 4LI output voltages, the PCC voltages, and the 4LI output currents in the dq0 frame, respectively, obtained using Park transformation. ω is the grid voltage angular frequency.

The dq0 reference frame provides significant benefits over the abc frame in controlling 4LI output currents. By transforming the three-phase time-varying signals into a rotating reference frame aligned with the grid voltage vector, the dq0 transformation converts sinusoidal AC signals into DC quantities under steady-state conditions. This simplification allows for easier and more precise control using conventional PI controllers, which are naturally suited for regulating DC variables. Additionally, it decouples active and reactive power control, with the d-axis typically associated with active power and the q-axis with reactive power, enabling independent and more efficient regulation of both. Moreover, the dq0 frame improves the dynamic response and stability of the control system, especially under unbalanced or distorted grid conditions. In contrast, the abc frame deals with sinusoidal variables directly, requiring more complex control algorithms and often resulting in slower and less robust performance.

II.3.1.1.2. DC bus voltage dynamic

The DC bus voltage dynamic is a fundamental aspect of controlling PV grid-connected 4LIs, as it ensures the reliable and efficient transfer of power from the PVG to the grid. The DC bus voltage serves as the intermediate link between the PVG and the AC output of the 4LI, and its stability directly affects the performance and safety of the entire system. By accurately modeling the DC bus voltage dynamic, the controller can regulate the energy balance between the input (from the PVG) and the inverter's output (to the grid), preventing overvoltage or undervoltage conditions that could damage components or trigger protective shutdowns. This dynamic information is also essential for implementing MPPT, where the controller must adjust the operating point of the PVG without causing instability in the DC link. Moreover, during transient events such as load changes, irradiance

fluctuations, or grid disturbances, understanding the DC bus dynamics allows the controller to maintain voltage within desired limits, ensuring continuous and smooth operation. By applying Kirchhoff's law to the DC side of the 4LI, the dynamic model of the DC voltage can be expressed as follows [133-135]:

$$\frac{dV_{dc}}{dt} = \frac{1}{C_{dc}} I_C = \frac{1}{C_{dc}} (I_D - I_{dc}) \quad \text{(II.13)}$$

The variable I_C represents the current flowing through the DC capacitor, while I_D denotes the output current from the DC-DC boost converter. Additionally, I_{dc} symbolizes the input current to the 4LI.

II.3.1.1.3. Relationship between AC and DC sides of the 4LI

When the 4LI system operating in steady-state conditions, if we consider the 4LI and its output filter to have negligible losses, then the AC input power (P_{AC}) becomes approximately equal to the DC side output power (P_{dc}). Based on the principles of instantaneous power theory described in [136], we can express the relationship between the AC and DC sides of the 4LI using Equation (II.14).

$$v_{cd} i_{fd} + v_{cq} i_{fq} = V_{dc} I_{dc} \quad \text{(II.14)}$$

Based on the principles of Voltage Oriented Control in the dq0 reference frame, when the d-axis PCC voltage is aligned with the PCC voltage vector, the d component of the PCC voltage (v_{cd}) becomes equal to the magnitude of the PCC voltage vector (V_{cmax}), while the q component (v_{cq}) is reduced to zero, as explained in references [136-139]. As a result, Equation (II.14) can be simplified to:

$$v_{gd} i_d = V_{dc} I_{dc} \quad \text{(II.15)}$$

From this equation, the 4LI's input DC current can be expressed as in Equation (II.16).

$$I_{dc} = \frac{v_{cd}}{V_{dc}} i_{fd} \quad \text{(II.16)}$$

where the ration ($\frac{v_{cd}}{V_{dc}}$) can guarantee the power balance between both sides of the 4LI.

According to the Equations (II.13) and (II.16), we obtain:

$$i_{fd} = \frac{V_{dc}}{v_{cd}} (I_D - I_C) \quad \text{(II.17)}$$

This equation is the basic of degerming the 4LI's output current reference used in the regulation of the active power, guarantying the power balance between both sides of the 4LI.

Equation (II.17) demonstrates that the dynamics of the DC-link voltage are fundamentally influenced by the power equilibrium between the front stage (DC-DC boost converter output) and the grid active power, as well as by the grid voltage and the DC capacitor characteristics.

In steady state operation, the PVG grid-connected 4LI system maintains a stable DC-bus voltage by equalizing the output power from the DC-DC boost converter with the grid active power. When the DC-DC boost converter delivers more power than what flows to the grid, the DC-bus voltage increases; alternatively, when grid active power exceeds the boost converter output, the DC-bus voltage decreases. This equilibrium continuously shifts due to changing solar conditions and grid voltage fluctuations. Variations in solar irradiance directly impact the PVG power generation (and subsequently the DC-DC boost converter's output), creating disturbances in the DC voltage. Rapid

increases in irradiance cause the DC voltage to rise, while sudden decreases lead to drops in the DC-bus voltage [133].

Likewise, fluctuations in grid voltage require the 4LI to modify its operation, potentially disrupting the DC-link voltage stability. Abrupt increases or decreases in grid voltage result in corresponding changes to the DC-bus voltage. During these transitional states, the current in the DC capacitor experiences more pronounced fluctuations, potentially jeopardizing system reliability and safety. The capacity of the DC capacitor significantly influences voltage stability. While increased capacitance helps mitigate short-term voltage disruptions and diminish ripple to enhance DC-bus voltage stability, it also results in slower DC bus voltage responses to intentional voltage adjustments, creating a compromise between steady-state performance and dynamic responsiveness. Therefore, developing robust control mechanisms for both the DC-bus voltage and grid currents is essential for optimizing system performance and ensuring reliability.

II.3.1.2. Sizing of 4LI's input and output passive filters [79]

II.3.1.2.1. Sizing of 4LI's input DC capacitor

The use of capacitor banks is effective for small and medium power applications. For high power requirements, superconducting coils are utilized. The selection of voltage (V_{dc}) and capacitance (C_{dc}) of the capacitor influences both the dynamics and compensation quality of the parallel active filter. Higher DC voltage improves the dynamic performance of the 4LI. Moreover, variations in the DC voltage, resulting from 4LI-generated currents and constrained by the selected capacitance, can negatively impact the compensation performance of the 4LI. In addition, the DC bus capacitor plays a critical role in the overall performance of a PVG grid-connected system. Its primary functions include:

- Maintaining a constant DC bus voltage with minimal oscillations during steady-state operation;
- Transferring power generated by the PVG system to the 4LI and providing the necessary reactive energy in the system;
- Serving as reactive energy storage elements to compensate for reactive power differences between the load and the grid.

As shown in Figure II.4, the behavior of the total DC bus voltage depends on the DC-DC boost conveter's output current I_D coming from the DC side of the system and the current 4LI input current I_{dc}. To sizing the DC bus capacitor, we employ a simpler method based on calculating the energy stored in the DC bus [140, 141].

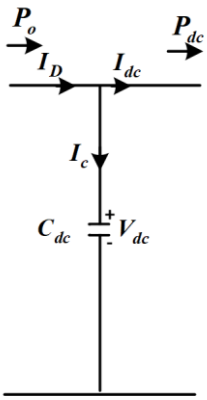


Figure II.4: Four leg inverter's input DC capacitor.

As given in Equation (II.13), the DC voltage dynamics can be expressed by:

$$C_{dc}\frac{dV_{dc}}{dt} = I_D - I_{dc} \quad \text{(II.18)}$$

The energy stored in the DC bus capacitor is given by [79]:

$$W_C = \frac{C_{dc}}{2}V_{dc}^2 \quad \text{(II.19)}$$

The dynamic (variation) of this energy stored can be expreesed by:

$$\frac{dW_C}{dt} = C_{dc}V_{dc}\frac{dV_{dc}}{dt} = P_C \quad \text{(II.20)}$$

When multiplying both terms of Equation (II.19) by the DC bus voltage, we obtain:

$$\frac{dW_C}{dt} = P_C = P_o - P_{dc} \quad \text{(II.21)}$$

where P_C represent the power stored in the DC capacitor, P_o the DC-DC boost converter's output power, and P_{dc} is the 4LI's input DC power.

From Equations (II.19) and (II.21), we obtain the value of the DC bus capacitor as follows:

$$\frac{dW_C}{dt} = C_{dc} \geq \frac{P_C\Delta t}{V_{dc}\Delta V_{dc}} \quad \text{(II.22)}$$

II.3.1.2.2. Sizing of 4LI's output filter inductor

In PVG grid-connected inverters, the inverter output inductor filter plays a critical role in ensuring the quality and reliability of power injection into the grid. Its primary function is to attenuate high-frequency switching harmonics generated by the inverter, thereby reducing total harmonic distortion (THD) and ensuring compliance with grid standards. By smoothing the inverter's pulsed output current into a near-sinusoidal waveform, the inductor helps deliver clean energy to the grid. Additionally, it limits inrush and fault currents, providing protection for both the inverter and grid infrastructure. The inductor filter also aids in decoupling the inverter from grid disturbances, such as voltage sags or transients, which enhances overall system stability. Furthermore, it enables precise control of the inverter output current's phase and amplitude, which is essential for maintaining synchronization with the grid during power injection. Several design criteria for the inductive filter have been presented in [131], [142]. In our case, we selected the approach based on the peak ripple of the output current flowing through the inductive filter.

The peak-to-peak ripple value of the output current is given by [142].

$$\Delta i_f = \sqrt{\frac{2}{3}}\frac{V_{dc}T_{s\_inv}}{4L_f} \quad \text{(II.23)}$$

where T_{s_inv} is the inverter's switching period.

According to Equation (II.23), we obtain the minimal value of the inductor filter as follows:

$$L_f = \sqrt{\frac{2}{3}}\frac{V_{dc}T_{s\_inv}}{4\Delta i_f} \quad \text{(II.24)}$$

II.4. Control of the 4LI-based PVG grid connected on mode harmonic filtrations and reactive power compensation

This section focuses on the analysis of an electrical system composed of a four-wire three-phase PVG grid connected 4LI supplying a nonlinear load, which consists of PVG, three phase grid, three single-phase rectifiers, along with a 4LI-based active filter connected in parallel to the grid, as shown in Figure II.5. In this configuration, the 4LI-based active filter operates as a current source. It is controlled to inject reactive power, harmonics, and zero-sequence current into the grid that are equal in magnitude but opposite in phase to those drawn by the nonlinear load. To achieve effective compensation of all reactive power, harmonics, and zero-sequence current, the control system of the 4LI-based active filter must generate a reference current that accurately reflects the reactive power and harmonic content of the load current. The overall control diagram of the PVG grid connected 4LI-based harmonic eliminations and reactive power compensation is shown in Figure II.5.

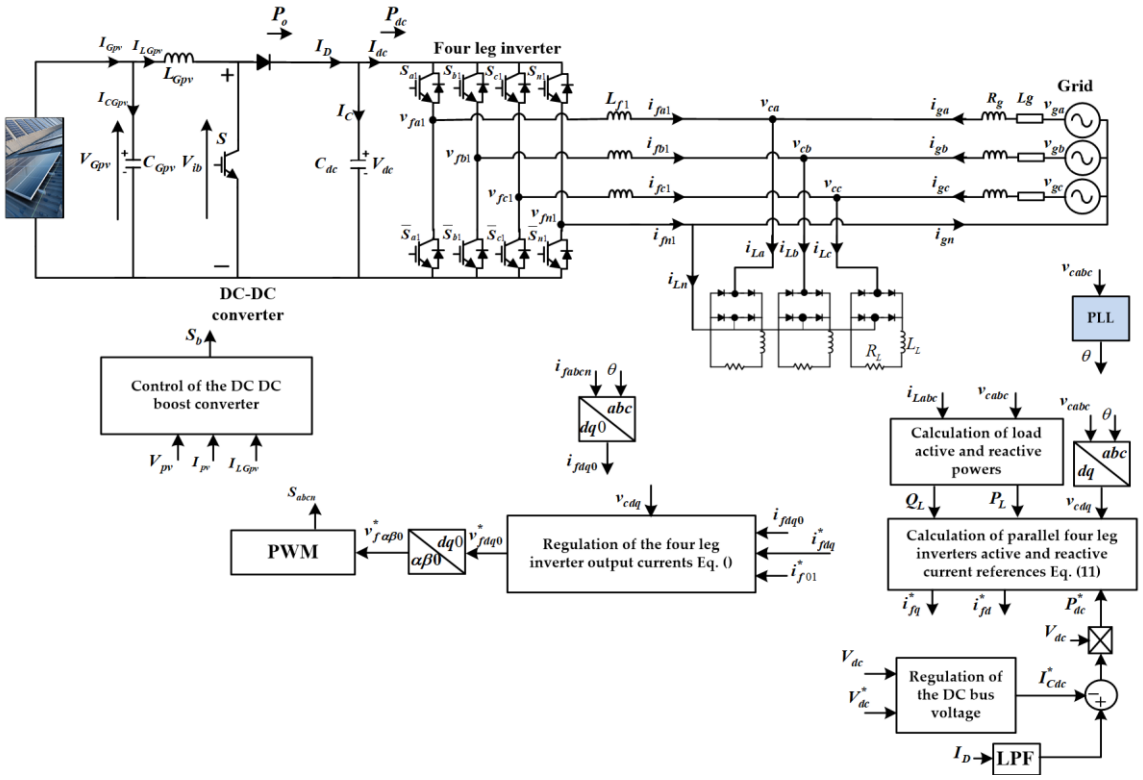


Figure II.5: Overall control diagram of the PV grid-connected 4LI for harmonic and reactive power compensation under nonlinear single phase loads.

The purpose of parallel active filtering is to compensate for harmonics and reactive power injected into the grid by nonlinear loads and to ensure that the grid maintain unit power factor with sinusoidal currents. The first step in the filtering and reactive power compensation process is the detection of

the load current harmonics and reactive power that need to be eliminated so that their counter-components can be injected back into the grid. Effective harmonic and reactive power detection are essential for achieving efficient compensation. Various identification methods have been proposed in the literature, which can generally be categorized into two main groups [131], [142–146].

The first group relies on the Fast Fourier Transform (FFT) to extract the harmonic components of the current. This approach is well-suited for loads where the harmonic content changes slowly over time. It also allows selective compensation by targeting the most dominant harmonics. However, the main drawbacks of this method include its high computational complexity, significant memory requirements, and limited performance during transient conditions [142], [144].

The second group of methods is based on the calculation of instantaneous power in the time domain. Some techniques within this category focus on evaluating the harmonic power content of nonlinear loads, while others are capable of compensating both harmonic currents and reactive power by subtracting the fundamental active component from the total current. Time-domain methods generally offer faster response and require fewer computations compared to frequency-domain approaches. Additionally, other identification strategies have been developed to allow selective compensation of one, several, or all types of disturbing currents. One such method is synchronous detection based on the Park transformation, which has also been proposed. However, this technique demands highly accurate estimation of the fundamental frequency to avoid incorrect harmonic identification [143]. It is worth noting that the most widely used identification technique is the instantaneous real and imaginary power method, which is used in this work.

The second step involves the regulation of the 4LI output currents and the DC bus voltage, which is essential for ensuring stable operation, effective power delivery, and compliance with grid standards. The regulation of output currents typically involves the implementation of a 4LI output currents control loop, often in a synchronous (dq) reference frame where the 4LI output currents track their reference currents derived using first step. This allows precise control over the harmonic and reactive power injected into the grid, and ensures that the grid current maintains a sinusoidal shape with minimal distortion and unit power factor.

Meanwhile, regulating the DC bus voltage is crucial for maintaining the pawer balance between the input (from the PVG) and the 4LI output. A voltage control loop monitors the DC link voltage and adjusts the d component of the output current references accordingly to ensure the bus voltage remains within a desired range, despite load or generation fluctuations. This control loop often works in coordination with the 4LI output currents control loop to maintain system stability. If the DC voltage drops due to load changes, insufficient power generation, or grid voltage sage, the controller reduces the output power demand, and vice versa [133].

Together, these regulation loops ensure that the 4LI can deliver high-quality power, prevent overvoltage or undervoltage conditions on the DC link, and meet dynamic requirements such as rapid changes in grid conditions or load behavior.

The third step involves the synchronization method, which is critical for aligning the 4LI output currents with the grid in terms of frequency, phase angle, and voltage magnitude before and during grid connection. Proper synchronization ensures seamless power transfer, maintains grid stability. Without accurate synchronization, the 4LI could inject power at the wrong phase or frequency, leading to power quality issues or even damaging both the inverter and grid infrastructure.

Synchronization is commonly accomplished using Phase-Locked Loop (PLL), which is a control mechanism that aligns the phase and frequency of the 4LI internal reference (usually the synchronous rotating dq frame) to that of the grid voltage. The PLL continuously monitors the grid voltage and adjusts the 4LI's output accordingly to ensure that the phase difference remains zero or within a very narrow range.

There are several types of PLLs used in practice [147, 148], such as the Synchronous Reference Frame PLL (SRF-PLL) [149, 150], Decoupled Double Synchronous Reference Frame PLL (DDSRF-PLL) [151], Second-Order Generalized Integrator PLL (SOGI-PLL) [152], simple and robust PLL (RPLL) [153]. These systems differ in complexity, dynamic performance, and their ability to deal with distorted or unbalanced grid conditions. For instance, the RPLL is the recommended synchronization method in three-phase systems, which provides robust synchronization even under grid voltage variations, which is used in this work.

The final step in the 4LI control process is the generation of Pulse Width Modulation (PWM) signals, which are used to control the switching devices within the 4LI. This step translates the reference voltages provided by the 4LI output currents control loop, into high-frequency switching commands that shape the inverter's output voltage waveforms.

PWM techniques regulate how long and when each 4LI's switch is turned on or off within a switching cycle, thereby synthesizing an AC output voltages from a DC voltage source. The most commonly used technique in grid-tied 4LI's is Sinusoidal PWM (SPWM) or Offset Voltage Sinusoidal PWM (OVSPWM) [154] involves comparing a sinusoidal reference signal with a high-frequency triangular carrier wave to generate the switching commands [12-16], [133-135]. 3D SVM [131], on the other hand, uses a vector-based approach in the stationary reference frame to optimize voltage utilization and reduce harmonic distortion while generating the switching commands, which is the applied in this work.

II.4.1. Synchronization method

II.4.1.1. Phase-LockedLoop (PLL)

The Phase-Locked Loop(PLL) circuit is widely used for grid voltage phase estimation. Its primary function is to accurately determine and filter the instantaneous phase and amplitude of the equivalent phasor in a three-phase system. The input to this identification process is the three-phase PCC voltage signal. As previously discussed, the grid voltage should ideally be clean (sinusoidal and balanced); otherwise, power-based methods become ineffective. However, because grid voltage is often distorted or unbalanced in practice, the use of a PLL-based control system is suggested for extracting the fundamental component of the voltage, enabling the identification methods to be applied under non-ideal conditions. This is achieved when the estimated phase angle θ matches the actual phase of the grid voltage. In [147, 148], several types of three-phase PLLs are presented. These systems transform the voltage signals from the abc frame into the Park (dq) reference frame, where a well-estimated instantaneous phase results in the direct-axis voltage component v_{cd} becoming zero.

Figure II.6 shows the standard configuration of a three-phase PLL, which generally includes three primary elements: a phase detector (PD), a low-pass filter (LF), and a voltage-controlled oscillator (VCO) [155].

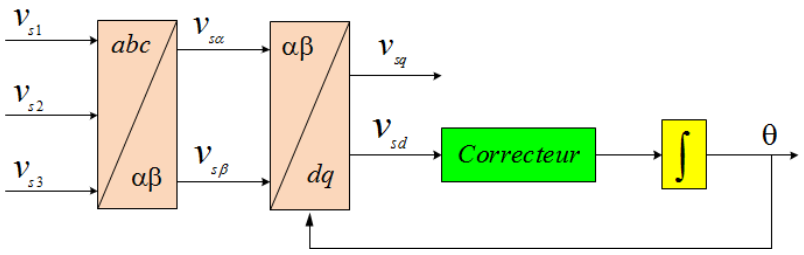


Figure II.6: Schematic of the traditional PLL.

Figure II.7 presents the detailed block diagram of the conventional PLL used in this study. This approach is designed to detect the parameters of the fundamental component of the PCC voltages $(\hat{\theta}, V_{max})$, as described by the following equation:

$$\begin{bmatrix} v_{ca} \\ v_{cb} \\ v_{cc} \end{bmatrix} = V_{max} \begin{bmatrix} cos(\omega_g t) \\ cos(\omega_g t - \frac{2\pi}{3}) \\ cos(\omega_g t + \frac{2\pi}{3}) \end{bmatrix} \quad \text{(II.25)}$$

After transforming these voltages into the $\alpha\beta$ frame, the following expression is obtained:

$$\begin{cases} v_{c\alpha} = \sqrt{\frac{2}{3}}.V_{max}\left[cos(\omega_g t) - \frac{1}{2}cos\left(\omega_g t - \frac{2\pi}{3}\right) - \frac{1}{2}cos(\omega_g t + \frac{2\pi}{3})\right] \\ v_{c\beta} = \sqrt{\frac{2}{3}}.V_{max}\left[\frac{\sqrt{3}}{2}cos\left(\omega_g t - \frac{2\pi}{3}\right) - \frac{\sqrt{3}}{2}cos\left(\omega_g t + \frac{2\pi}{3}\right)\right] \end{cases} \quad \text{(II.26)}$$

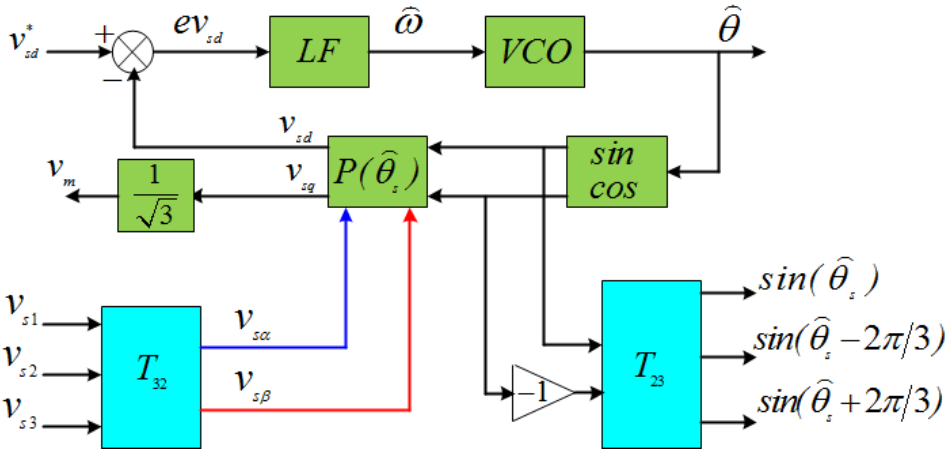


Figure II.7: Schematic detail of the traditional PLL.

After simplifying the previous expressions, the result is:

$$\begin{bmatrix} v_{c\alpha} \\ v_{c\beta} \end{bmatrix} = 3\sqrt{\frac{3}{2}}.V_{\max} \begin{bmatrix} \sin(\omega_g t) \\ -\cos(\omega_g t) \end{bmatrix} \quad \text{(II.27)}$$

And in the synchronous reference frame:

$$\begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} v_{c\alpha} \\ v_{c\beta} \end{bmatrix} \quad \text{(II.28)}$$

where θ represents the estimated angular position of the three-phase PCC voltage vector.

We obtained:

$$v_{cd} = 3\sqrt{\frac{3}{2}}.V_{max}\left[sin\left(\omega_g t\right)cos(\theta) - cos\left(\omega_g t\right)sin(\theta)\right] \quad \text{(II.29)}$$

$$v_{cd} = 3\sqrt{\frac{3}{2}}.V_{max}\, sin(\omega_g t - \theta) \quad \text{(II.30)}$$

Assuming that $(\omega t - \theta)$ is very small, the previous expression can be approximated as:

$$v_{cd} = 3\sqrt{\frac{3}{2}}V_{\max}(\omega_g t - \theta) \quad \text{(II.31)}$$

The estimated angular frequency is given by:

$$\hat{\omega} = H.3\sqrt{\frac{3}{2}}V_{\max}(\omega_g t - \theta) \quad \text{(II.32)}$$

where H is the transfer function of the PI controller-based PLL

$$H = k_{pPLL} + \frac{k_{iPLL}}{s} \quad \text{(II.33)}$$

The angular position of the three-phase PCC voltage vector is given by:

$$\theta = \frac{\hat{\omega}_g}{s} \quad \text{(II.34)}$$

Substituting equations (II.30) and (II.31) into equation (II.29) yields:

$$\theta s = \left(k_{pPLL} + \frac{k_{iPLL}}{s} \right).3\sqrt{\frac{3}{2}}.V_{max}(\omega_g t - \theta) \quad \text{(II.35)}$$

From this, the following transfer function of the system is obtained:

$$\frac{\theta}{\omega_g t} = \frac{\left(k_{pPLL}s + k_{iPLL}\right).3\sqrt{\frac{3}{2}}.V_{max}}{s^2 + \left(k_{pPLL}s + k_{iPLL}\right).3\sqrt{\frac{3}{2}}.V_{max}} \quad \text{(II.36)}$$

All that remains now is to calculate the gains k_{pPLL} and k_{iPLL}, which are given by:

$$k_{iPLL} = \frac{1}{3}\sqrt{\frac{2}{3}}\frac{(2\pi f_c)^2}{V_{\max}} \qquad and \qquad k_{pPLL} = \frac{2\sqrt{2}}{3\sqrt{3}}\frac{2\pi f_c \xi}{V_{\max}} \quad \text{(II.37)}$$

II.4.1.2. Robust synchronization PLL unit

In traditional PVG grid-connected inverters, which interface with the main grid via transmission lines, variations in system states and parameters can significantly affect overall performance. Changes

in inverter output filter and line parameters, voltage fluctuations at the PCC, and the inherent positive feedback introduced by the traditionalPLL structure can cause unwanted transients or even lead to system instability. Additionally, in SAPF configurations, the only voltage accessible is the one measured at the PCC. This voltage often degrades when nonlinear loads draw distorted currents, which introduce current harmonics. Additionally, if the load currents are unbalanced, negative-sequence voltage components may appear at the PCC, potentially leaving residual harmonics in the source current even after compensation [156]. To address these challenges, in this section we introduce an alternative synchronization approach proposed in [153] that replaces the conventional PLL-based synchronization method, as depicted in Figure II.8. This robust synchronization PLL unit (RSPLLU) is analytically examined for scenarios where the 4LI connects to the PCC either directly or through a transmission line. The objective of the RSPLLU method is to accurately follow the frequency of the grid voltages, which may originate from either a stable three-phase sinusoidal source or a time-varying voltage at the PCC. The RSPLLU is formulated with a frequency-focused approach, where its dynamic behavior is described using two key state variables: (a) the phase angle θ, and (b) the scaled frequency deviation $\Delta\omega$. The open-loop behavior of this synchronization framework can be characterized by the following dynamics:

$$\dot{\theta} = \omega_n + l_1 \Delta\omega \tag{II.38}$$

$$\Delta\dot{\omega} = tan^{-1}\left(\frac{v_{cq}}{v_{cd}}\right) - l_2 \Delta\omega \tag{II.39}$$

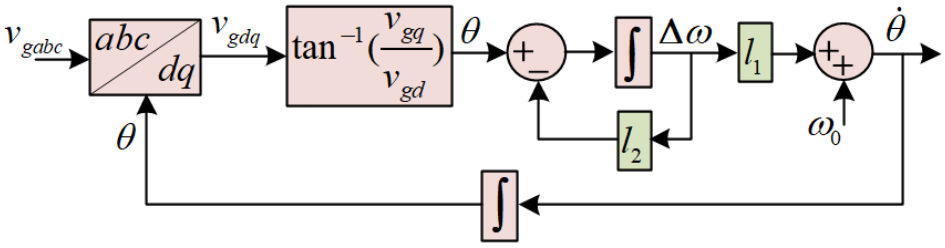


Figure II.8: Schematic detail of the RSPLLU.

The RSPLLU, illustrated in Figure II.8, exhibits notable distinctions compared to conventional PLLs. Unlike standard designs, the phase angle dynamics described in Equation (II.38) do not incorporate any proportional elements linked to the measured voltage. Additionally, a key differentiator lies in how the frequency-related component is managed: it is adjusted solely through a carefully controlled variable, $\Delta\omega$. This contrasts with traditional PLL architectures, where one of the voltage components in the dq frame is typically used as input to a PI controller.

II.4.2. Detection of the 4LI's output current references

II.4.2.1. Instantaneous power theory (pq0)

In this mode, the PVG 4LI system is designed to perform both harmonic current elimination and reactive power compensation under nonlinear single-phase load conditions. The current reference for the 4LI is derived by extracting the undesired components of the nonlinear load current. This process involves measuring the load current and applying either reference currents detection method to decompose the current into its fundamental active, reactive, and harmonic components. The non-fundamental components, comprising both the harmonic and reactive parts are then isolated and used

to generate the 4LI output current references. These components are supplied by the 4LI to prevent their injection into the PCC, thereby ensuring effective harmonic mitigation and reactive power support, which significantly improves overall power quality.

The instantaneous power theory, introduced by [146], utilizes the Concordia transformation of load currents and PCC voltages to compute the instantaneous active, reactive, and zero-sequence powers. This method also enables the conversion of the fundamental component into a DC quantity, while harmonic components are transformed into AC quantities. Such a transformation is essential for easily isolating the DC component of the instantaneous active power (which corresponds to the fundamental component of the load current) using a simple low-pass filter (LPF) [157].

The *pqo* theory was initially formulated for three-phase, four-wire systems with balanced and sinusoidal source voltages. It involves transforming the three-phase system (abc) into the αβo reference frame, simplifying both theoretical analysis and the implementation of active filter control. In this frame, there are two degrees of freedom available for current control [131]. Figure II.9 illustrates the basic concept of this method.

Generally, three-phase voltages and currents can be transformed and expressed in the αβo coordinate system as follows [158, 159].

$$\begin{bmatrix} v_{c\alpha} \\ v_{c\beta} \\ v_{co} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_{ca} \\ v_{cb} \\ v_{cc} \end{bmatrix} \tag{II.40}$$

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \\ i_{Lo} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{II.41}$$

The relationship between the neutral current and the zero-sequence current is defined by the following equations:

$$i_{Ln} = i_{La} + i_{Lb} + i_{Lc} \tag{II.42}$$

$$i_{L0} = \frac{1}{\sqrt{3}}(i_{La} + i_{Lb} + i_{Lc}) = \frac{1}{\sqrt{3}} i_{Ln} \tag{II.43}$$

According to the pq0 theory, the instantaneous load active power p_L, reactive power q_L, and zero-sequence power p_{Lo} are defined as follows:

$$\begin{bmatrix} p_L \\ q_L \\ p_{Lo} \end{bmatrix} = \begin{bmatrix} v_{L\alpha} & v_{L\beta} & 0 \\ -v_{L\beta} & v_{L\alpha} & 0 \\ 0 & 0 & v_{Lo} \end{bmatrix} \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \\ i_{Lo} \end{bmatrix} \tag{II.44}$$

These power components can be represented as the combination of a direct (DC) part and an alternating (AC) part, as shown below:

$$\begin{bmatrix} p_L \\ q_L \\ p_{Lo} \end{bmatrix} = \begin{bmatrix} \bar{p}_L + \tilde{p}_L \\ \bar{q}_L + \tilde{q}_L \\ \bar{p}_{Lo} + \tilde{p}_{Lo} \end{bmatrix} \tag{II.45}$$

Where $\bar{p}_L$ and $\bar{q}_L$ represent the DC components of p_L and q_L, while $\tilde{p}_L$ and $\tilde{q}_L$ represent their AC components.

The calculation of the load current components in αβo reference frame for the different energy terms is possible. The expression is given as follows:

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \\ i_{Lo} \end{bmatrix} = \frac{1}{v_{co}(v_{c\alpha}^2 + v_{c\beta}^2)} \begin{bmatrix} v_{co}v_{c\alpha} & -v_{co}v_{c\beta} & 0 \\ v_{co}v_{c\beta} & v_{co}v_{c\alpha} & 0 \\ 0 & 0 & (v_{c\alpha}^2 + v_{c\beta}^2) \end{bmatrix} \begin{bmatrix} p_L \\ q_L \\ p_{Lo} \end{bmatrix} \tag{II.46}$$

By using equation (II.44), we obtain the following expression for the real and imaginary powers:

$$\begin{bmatrix} p_L \\ q_L \end{bmatrix} = \begin{bmatrix} v_{c\alpha} & v_{c\beta} \\ -v_{c\beta} & v_{c\alpha} \end{bmatrix} \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} \tag{II.47}$$

And

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} = \begin{bmatrix} v_{c\alpha} & v_{c\beta} \\ -v_{c\beta} & v_{c\alpha} \end{bmatrix}^{-1} \begin{bmatrix} p_L \\ q_L \end{bmatrix} = \frac{1}{v_{c\alpha}^2 + v_{c\beta}^2} \begin{bmatrix} v_{c\alpha} & -v_{c\beta} \\ v_{c\beta} & v_{c\alpha} \end{bmatrix} \begin{bmatrix} p_L \\ q_L \end{bmatrix} \tag{II.48}$$

Equation (II.48) can be rewritten in the following form:

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \\ i_{Lo} \end{bmatrix} = \frac{1}{v_{c\alpha}^2 + v_{c\beta}^2} \begin{bmatrix} v_{c\alpha} & -v_{c\beta} & 0 \\ v_{c\beta} & v_{c\alpha} & 0 \\ 0 & 0 & v_{l\alpha}^2 + v_{l\beta}^2 \end{bmatrix} \begin{bmatrix} p_L \\ q_L \\ i_{Lo} \end{bmatrix} \tag{II.49}$$

Depending on the intended function of the 4LI-based APF, it is possible to compensate for both current harmonics and reactive power simultaneously, or just one of the two. For instance, if we aim to compensate both current harmonics and reactive power at the same time, we can remove the DC component of *p* using a simple low-pass filter (LPF).

In the case of simultaneous compensation of current harmonics and reactive power, the reference powers are given by:

$$p^* = \tilde{p}, q^* = q \tag{II.50}$$

In the case of harmonic current compensation only, the reference powers are given by:

$$p^* = \tilde{p}, q^* = \tilde{q} \tag{II.51}$$

The 4LI's output reference currents in the αβo frame are expressed as follows:

$$\begin{bmatrix} i_{f\alpha}^{*} \\ i_{f\beta}^{*} \\ i_{fo}^{*} \end{bmatrix} = \frac{1}{v_{c\alpha}^{2}+v_{c\beta}^{2}} \begin{bmatrix} v_{c\alpha} & -v_{c\beta} & 0 \\ v_{c\beta} & v_{c\alpha} & 0 \\ 0 & 0 & v_{c\alpha}^{2}+v_{c\beta}^{2} \end{bmatrix} \begin{bmatrix} p_{L}^{*} \\ q_{L}^{*} \\ i_{Lo}^{*} \end{bmatrix} \quad \text{(II.52)}$$

where $i_{fo}^{*} = i_{Lo}$

The 4LI's output reference currents in the dq0 frame are calculated using inverseParktransformation as follows:

$$\begin{bmatrix} i_{fd}^{*} \\ i_{fq}^{*} \\ i_{f0}^{*} \end{bmatrix} = \begin{bmatrix} cos(\theta_g) & sin(\theta_g) & 0 \\ -sin(\theta_g) & cos(\theta_g) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{f\alpha}^{*} \\ i_{f\beta}^{*} \\ i_{fo}^{*} \end{bmatrix} \quad \text{(II.53)}$$

The block diagram of the simplified reference determinations method using instantaneous real, imaginary, and zero-sequence power is shown in Figure II.9.

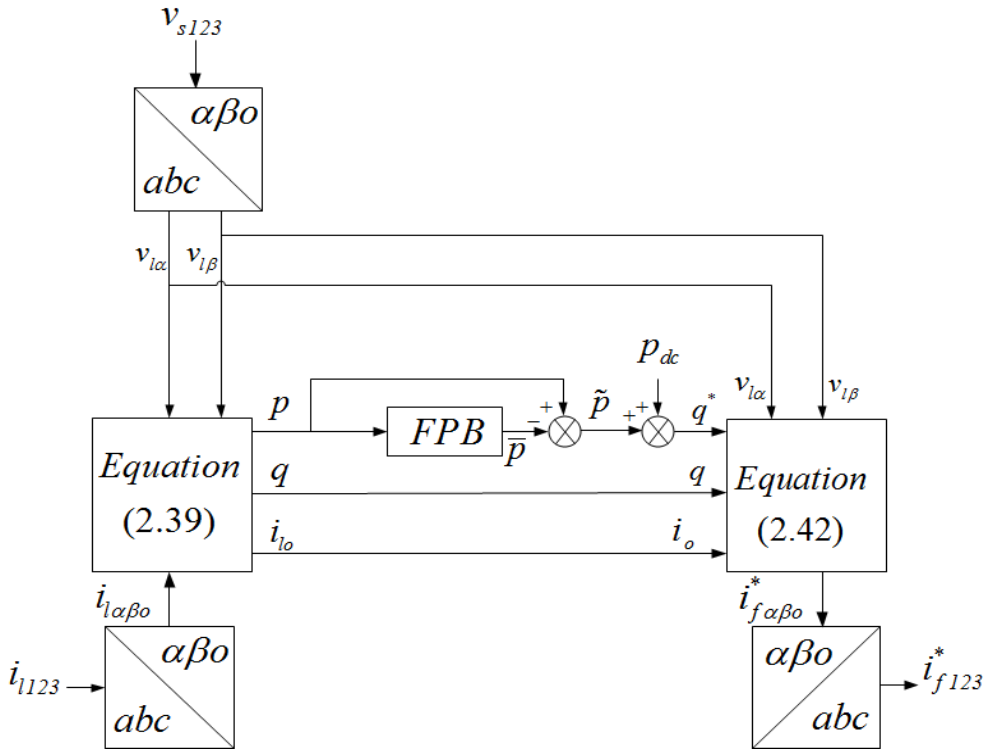


Figure II.9: Block diagram of the simplified reference determinations method using instantaneous real, imaginary, and ZS power

II.4.3. Regulation of the 4LI's input DC voltage

According to the DC voltage dynamics in Equation (13), the DC bus voltage can be performed to provide the DC capacitor reference as follows:

$$I_C^{*} = \frac{k_{pdc}s + k_{idc}}{s}(V_{dc}^{*} - V_{dc}) \quad \text{(II.54)}$$

From this current reference and using the 4LI's input current in Equation (), we obtain the 4LI's input current reference as follows:

$$I_{dc}^{*} = (I_{D}' - I_{C}^{*}) \quad \text{(II.55)}$$

Where I_{D}' is the filter DC -DC boost converter output current using LPF as follows:

$$I_{D}' = \frac{\omega_{cLPF}}{s+\omega_{cLPF}} I_{D} \quad \text{(II.56)}$$

Filtering the output current of the DDBC in the DC voltage control loop is essential for ensuring stable and accurate system performance. The DDBC operates at high switching frequencies, which introduce ripple and high-frequency noise into the output current. If this unfiltered, noisy signal is fed directly into the voltage controller, it can lead to poor control behavior, such as oscillations, instability, or incorrect regulation. By applying a low-pass filter, the high-frequency components are suppressed, allowing only the slow-changing, average current to pass through. This clean signal enables the PI controller to make precise adjustments to the 4LI's output current reference, resulting in smoother 4LI's output current regulation and improved dynamic response. In essence, filtering enhances the reliability and efficiency of the control loop by ensuring it responds only to meaningful variations in the system rather than to noise. In this work, ω_{cLPF} is selected equal 35 *rad/s*.

The block diagram of the DC bus voltage regulation using PI controller is shown in Figure II.10.

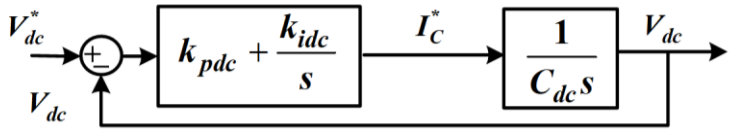


Figure II.10: block diagram of the DC bus voltage regulation using PI controller.

According to this figure and using the pole placement method, we obtain the gains k_{pdc} and k_{idc} as follows:

$$\begin{cases} k_{pdc} = 2\xi_{dc}\omega_{ndc}C_{dc} \\ k_{idc} = C_{dc}\omega_{ndc}^{2} \end{cases} \quad \text{(II.57)}$$

where ξ_{dc} and ω_{ndc} represent thedamping factor andthenatural frequency of the Dc bus voltage system, respectively

The 4LI's input power reference used in the determination of the 4LI's input power reference that also injected into the grid is expressed by:

$$p_{dc}^{*} = I_{dc}^{*}V_{dc} \quad \text{(II.58)}$$

II.4.4. Regulation of the 4LI output currents

As previously described, regulating the output currents of a 4LI is crucial for maintaining stable operation, delivering power effectively, and meeting grid compliance standards. This regulation is typically achieved through a current control loop implemented in the dq0 reference frame, where the inverter's output currents are made to track their respective reference values. The main objective is to compensate for harmonic and reactive power. This control approach enables precise management of the harmonic and reactive components injected into the grid, ensuring that the resulting grid currents remain sinusoidal with minimal distortion and close to a unit power factor. The dynamic behavior of the grid currents in the dq0 frame, originally described by equation (II.16), can be reformulated as follows:

$$\begin{cases} \dfrac{di_{fd}}{dt} = v'_{fd} = \dfrac{v_{fd}}{L_f} - \dfrac{v_{cd}}{L_f} - \omega i_{fq} \\ \dfrac{di_{fq}}{dt} = v'_{fq} = \dfrac{v_{fq}}{L_f} - \dfrac{v_{cq}}{L_f} + \omega i_{fd} \\ \dfrac{di_{f0}}{dt} = v'_{f0} = \dfrac{v_{f0}}{L_f} - \dfrac{v_{c0}}{L_f} \end{cases} \quad \text{(II.59)}$$

Where v'_{fd}, v'_{fq}, and v'_{f0} are the feedback terms that represent the inductor filter voltage drops.

Thus, based on the transformation in Equation (II.59), the coupling between the dynamics of the 4LI's output currents i_{fd} and i_{fq} has been transformed into a decoupled dynamic. As a result, the currents i_{fd} and i_{fq} can be controlled independently by acting respectively on the quantities inductor filter voltage drops v'_{fd} and v'_{fq}.

Using PI controllers, the references of the inductor filter voltage drops can be expressed by:

$$\begin{cases} v'^{*}_{fd} = \left(\dfrac{k_{pi}s + k_{ii}}{s}\right)(i^{*}_{fd} - i_{fd}) \\ v'^{*}_{fq} = \left(\dfrac{k_{pi}s + k_{ii}}{s}\right)(i^{*}_{fq} - i_{fq}) \\ v'^{*}_{f0} = \left(\dfrac{k_{pi}s + k_{ii}}{s}\right)(i^{*}_{f0} - i_{f0}) \end{cases} \quad \text{(II.60)}$$

where i^{*}_{fd}, i^{*}_{fq} and i^{*}_{f0} are the 4LI's output reference currents, which depend on the objective of the system, harmonic compensations only, or reactive power compensation only, or both at the same time.

The schematic diagram of the regulation of the 4LI's output currents in the dq0 reference frame using PI controllers is given in Figure II.11.

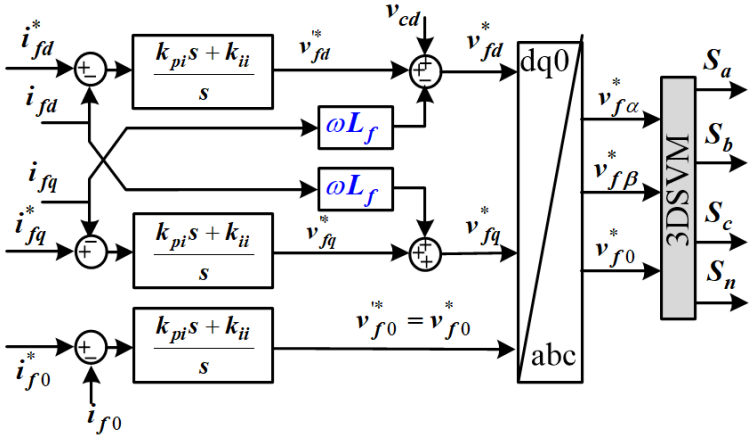


Figure II. 11: Block diagram of the inner 4LI's output currents controlloop in the dq0 reference frame using PI controllers

The block diagram of the 4LI's output current regulations using PI controllers is shown in Figure

II.12.

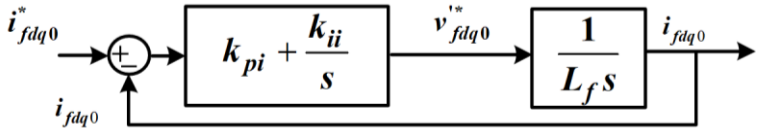


Figure II. 12: Block diagram of the 4LI's output current regulations using PI controllers

According to this figure and using the pole placement method, we obtain the gains k_{pi} and k_{ii} as follows:

$$\begin{cases} k_{pi} = 2\xi_i \omega_{ni} L_f \\ k_{idc} = L_f \omega_{ni}^2 \end{cases} \quad \text{(II.61)}$$

where ξ_i and ω_{ni} represent thedamping factor andthenatural frequency of the 4LI's output current system, respectively

The reference modulation voltages for both 3DSVM in the dq0 reference frame can be determined using the regulation of the 4LI's output currents inEquation () as follows:

$$\begin{cases} v_{fd}^* = v_{fd}'^* + v_{cd} + \omega L_f i_{fq} \\ v_{fq}^* = v_{fq}'^* - \omega L_f i_{fd} \\ v_{f0}^* = v_{f0}'^* \end{cases} \quad \text{(II.62)}$$

II.4.5. PWM generation techniques for 4LI

II.4.5.1. Three-Dimensional Space Vector Modulation (3D SVM)

Three-Dimensional Space Vector Modulation (3D SVM), as proposed by [160], is recognized as the most efficient and widely used among modulation methods. This technique aims to produce symmetrical output voltages for the 4LI, even when supplying unbalanced loads.

Due to the additional leg, a 4LI can achieve sixteen switching states (2^4), which is double the number of states (2^3) of a conventional three-leg two-level inverter.

For 3DSVM, there are 16 possible voltage vectors: fourteen active non-zero vectors and two zero vectors. The 3D space is divided into six prisms and 24 tetrahedrons (Figure II.13). Each prism consists of four tetrahedrons. The 3DSVM is implemented following the sequence shown in Figure II.13.

With the addition of a fourth leg, the 4LI can generate sixteen switching states (2^4), which is twice the number produced by a standard three-leg two-level inverter (2^3). In the context of 3DSVM, these switching states correspond to 16 voltage vectors, comprising fourteen active (non-zero) vectors and two zero vectors.

The 3D space is partitioned into six prisms and 24 tetrahedrons, as illustrated in Figure II.13, with each prism containing four tetrahedrons. The 3DSVM technique is applied by following the sequence depicted in Figure II.13 [131].

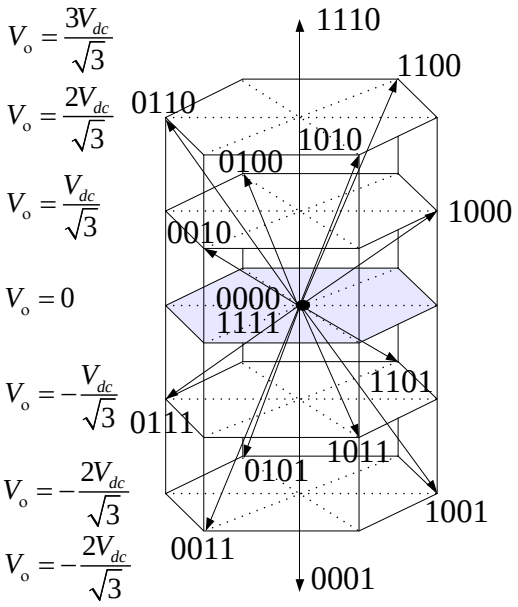


Figure II.13: Vectorial representation of voltages generated by the four-leg two-level inverter.

II.4.5.1.1. Identification of the Prism and Reference Vectors

This process is very similar to sector identification in 2DSVM. It is carried out by projecting the identified reference vectors $v^*_{f\alpha}$ and $v^*_{f\beta}$ into the (αβ0) frame. As shown in Figure II.14, the reference voltage can be located in one of the six prisms numbered 1 to 6 (Figure II.13) in 3D space.

Within the chosen prism, there are six non-zero reference vectors (two vectors, 1110 and 0001, aligned along the 0-axis, and four vectors corresponding to distinct switching states) and two zero vectors [131].

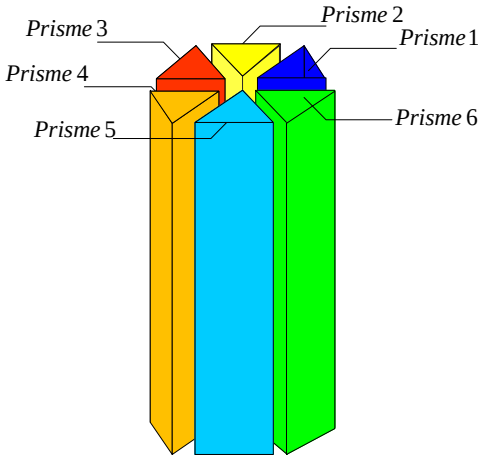


Figure II.14. Representation of different prisms

The prism is identified by analyzing the values of the reference vectors represented in the αβ0 coordinate system. Figure II.15 presents a flowchart that outlines the algorithm used for prism identification and demonstrates the corresponding detection steps [131].

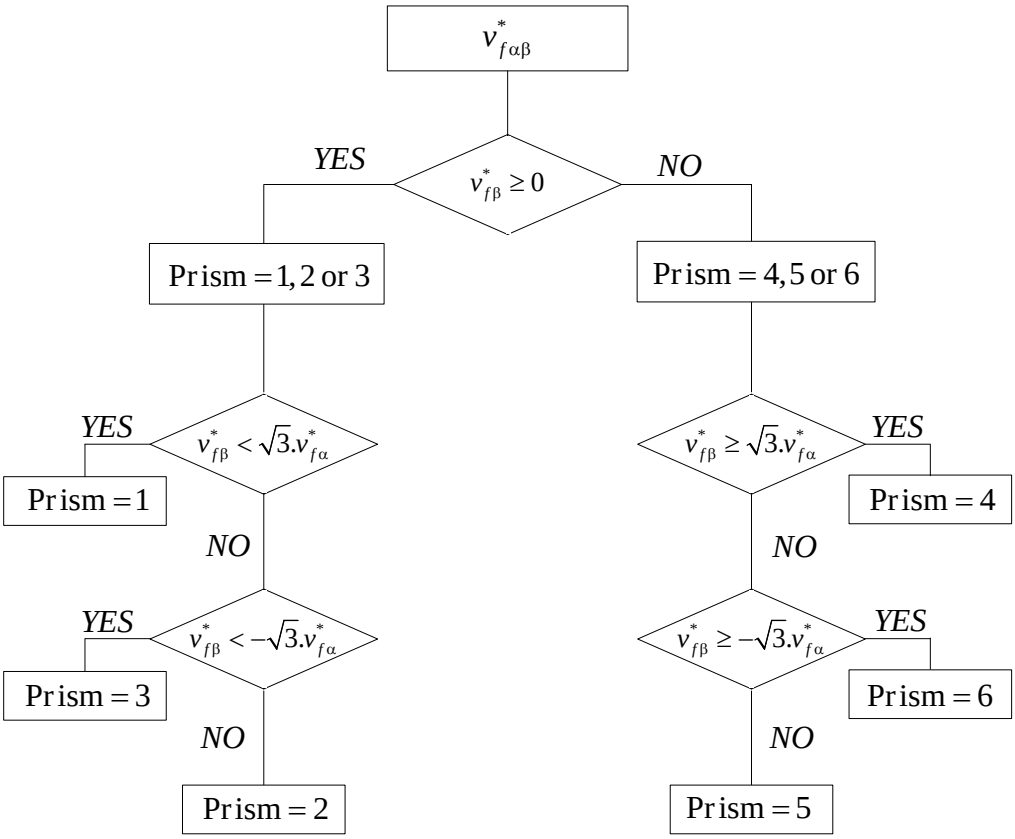


Figure II.15: Flowchart of prism identification operations.

II.4.5.1.2. Identification of Tetrahedrons

The second step is to choose the tetrahedron based on the location of the reference voltage vector. There are four tetrahedrons for each prism, which can be constructed by combining three non-zero switching state vectors and two zero switching state vectors, resulting in a total of 24 tetrahedrons within the hexagonal prism. Figures II.16 shows the four separate tetrahedrons in the 3D representation.

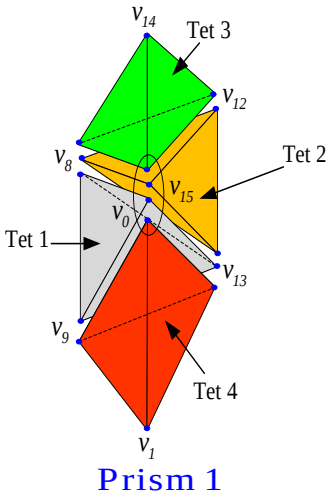


Figure II.16: Representation of the four tetrahedra (Tet1, Tet2, Tet3, Tet4) in prism 1 and the three non-zero state vectors in each tetrahedron [131].

Table 2.3 presents the three non-zero switching state vectors in each tetrahedron [131].

	Tet 1	Tet 2	Tet 3	Tet 4
P 1	v_8 :1000 v_9 :1001 v_{13} :1101	v_8 :1000 v_{12} :1100 v_{13} :1101	v_8 :1000 v_{12} :1100 v_{14} :1110	v_9 :1001 v_{13} :1101 v_1 :0001
P 2	v_{12} :1100 v_{13} :1101 v_4 :0100	v_{13} :1101 v_4 :0100 v_5 :0101	v_{12} :1100 v_4 :0100 v_{14} :1110	v_{13} :1101 v_5 :0101 v_1 :0001
P 3	v_4 :0100 v_5 :0101 v_7 :0111	v_4 :0100 v_6 :0110 v_7 :0111	v_4 :0100 v_6 :0110 v_{14} :1110	v_5 :0101 v_7 :0111 v_1 :0001
P 4	v_6 :0110 v_7 :0111 v_2 :0010	v_7 :0111 v_2 :0010 v_3 :0011	v_6 :0110 v_2 :0010 v_{14} :1110	v_7 :0111 v_3 :0011 v_1 :0001
P 5	v_2 :0010 v_3 :0011 v_{11} :1011	v_2 :0010 v_{10} :1010 v_{11} :1011	v_2 :0010 v_{10} :1010 v_{14} :1110	v_3 :0011 v_{11} :1011 v_1 :0001
P 6	v_{10} :1010 v_{11} :1011 v_8 :1000	v_{11} :1011 v_8 :1000 v_9 :1001	v_{10} :1010 v_8 :1000 v_{14} :1110	v_{11} :1011 v_9 :1001 v_1 :0001

Table 2.3: The three non-zero switching state vectors in each tetrahedron.

Figure II.17 represents the physical positions of the voltage vectors in each prism and in each tetrahedron.

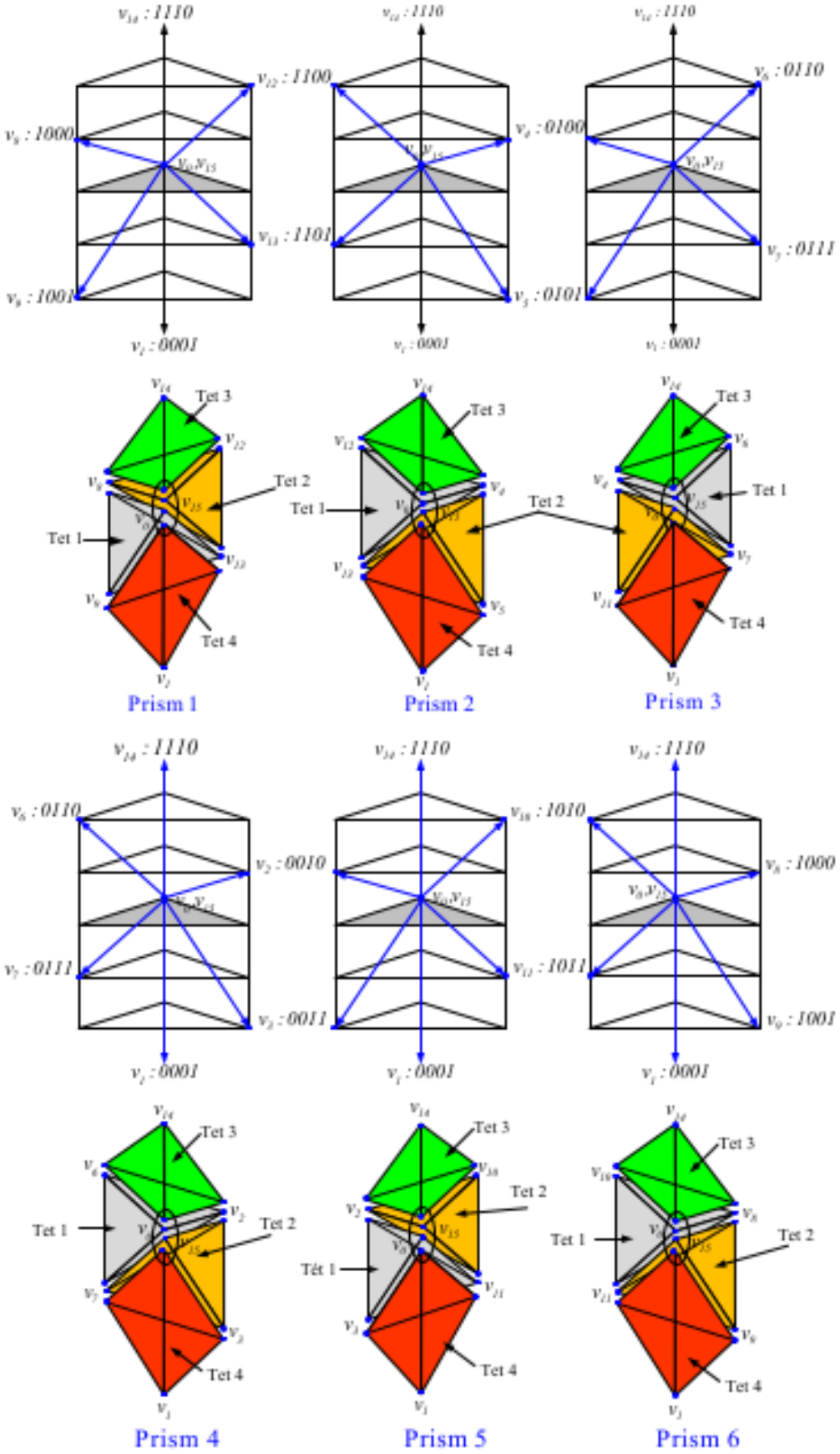


Figure II.17: represents the physical positions of the voltage vectors in each prism and in each tetrahedron [131].

We determine the equations of the planes that delimit each tetrahedron from the coordinates $(v^*_{f\alpha}, v^*_{f\beta}, v^*_{f0})$ in order to detect the tetrahedron that contains the reference vector.

For tetrahedron 1 of the firstprism, the equation of the first plane containing the vectors $v_o(0,0,0)$, v_9,v_{13} follows the equation [131]:

$$\begin{cases} a\sqrt{\frac{2}{3}}V_{dc} + b.0 + c = \frac{V_{dc}}{\sqrt{3}} \\ a\sqrt{\frac{1}{6}}V_{dc} + b\frac{\sqrt{2}}{2}V_{dc} + c = -\frac{V_{dc}}{\sqrt{3}} \end{cases} \quad \text{(II.63)}$$

This gives:

$$a = \frac{\sqrt{2}}{2}, b = -\sqrt{\frac{3}{2}}, c = 0 \quad \text{(II.64)}$$

The equation of the first plane is therefore:

$$v^*_{f0} = v^*_{f\alpha}\frac{\sqrt{2}}{2} - v^*_{f\beta}\sqrt{\frac{3}{2}} \quad \text{(II.65)}$$

The equation of the second plane containing the vectors $v_o(0,0,0)$, v_8 and v_{13} follows the equation:

$$\begin{cases} a\sqrt{\frac{2}{3}}V_{dc} + b.0 + c = -\frac{2V_{dc}}{\sqrt{3}} \\ a\sqrt{\frac{1}{6}}V_{dc} + b\frac{\sqrt{2}V_{dc}}{2} + c = -\frac{V_{dc}}{\sqrt{3}} \end{cases} \quad \text{(II.66)}$$

Which gives:

$$a = -\sqrt{2}, b = 0, c = 0 \quad \text{(II.67)}$$

The equation of this plane is:

$$v^*_{f0} = -v^*_{f\alpha}\sqrt{2} \quad \text{(II.68)}$$

Figure II.18 represent the planes of tet 1 belonging to prism 1:

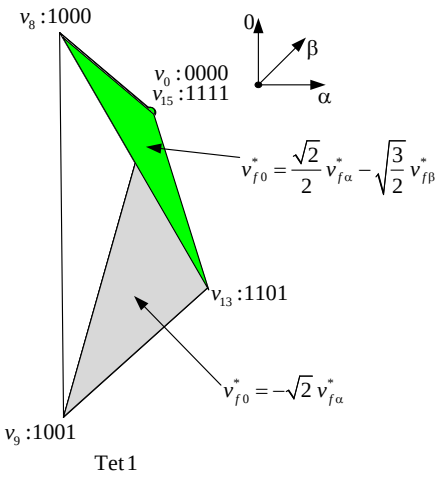


Figure II.18: Representation of the equations of the planes of tetrahedron 1 of prism I

For the end of the reference vector to be in tetrahedron 1, the following two inequalities must be verified:

$$\begin{aligned} v_{f0}^{*} &< v_{f\alpha}^{*}\frac{\sqrt{2}}{2} - v_{f\beta}^{*}\sqrt{\frac{3}{2}} \\ v_{f0}^{*} &> -v_{f\alpha}^{*}\sqrt{2} \end{aligned} \tag{II.69}$$

In this way, the passage of the voltage vector in the other tetrahedra will be calculated and located.

Table 2.4 presents the equations of the planes needed to delimit each tetrahedron [131].

	Tet 1	Tet 2	Tet 3	Tet 4
P_1	$v_{f0}^{*} < \frac{\sqrt{2}}{2}v_{f\alpha}^{*} - \sqrt{\frac{3}{2}}v_{f\beta}^{*}$ $v_{f0}^{*} > -\sqrt{2}v_{f\alpha}^{*}$	$v_{f0}^{*} < \frac{\sqrt{2}}{2}v_{f\alpha}^{*} + \sqrt{\frac{3}{2}}v_{f\beta}^{*}$ $v_{f0}^{*} > \frac{\sqrt{2}}{2}v_{f\alpha}^{*} - \sqrt{\frac{3}{2}}v_{f\beta}^{*}$	$v_{f0}^{*} > \frac{\sqrt{2}}{2}v_{f\alpha}^{*} + \sqrt{\frac{3}{2}}v_{f\beta}^{*}$	$v_{f0}^{*} < -\sqrt{2}v_{f\alpha}^{*}$
P_2	$v_{f0}^{*} < \frac{\sqrt{2}}{2}v_{f\alpha}^{*} + \sqrt{\frac{3}{2}}v_{f\beta}^{*}$ $v_{f0}^{*} > -\sqrt{2}v_{f\alpha}^{*}$	$v_{f0}^{*} < -\sqrt{2}v_{\alpha}^{*}$ $v_{f0}^{*} > \frac{\sqrt{2}}{2}v_{f\alpha}^{*} - \sqrt{\frac{3}{2}}v_{f\beta}^{*}$	$v_{f0}^{*} > \frac{\sqrt{2}}{2}v_{f\alpha}^{*} + \sqrt{\frac{3}{2}}v_{f\beta}^{*}$	$v_{f0}^{*} < \frac{\sqrt{2}}{2}v_{f\alpha}^{*} - \sqrt{\frac{3}{2}}v_{f\beta}^{*}$
P_3	$v_{f0}^{*} < \frac{\sqrt{2}}{2}v_{f\alpha}^{*} + \sqrt{\frac{3}{2}}v_{f\beta}^{*}$ $v_{f0}^{*} > \frac{\sqrt{2}}{2}v_{f\alpha}^{*} - \sqrt{\frac{3}{2}}v_{f\beta}^{*}$	$v_{f0}^{*} < -\sqrt{2}v_{f\alpha}^{*}$ $v_{f0}^{*} > \frac{\sqrt{2}}{2}v_{f\alpha}^{*} + \sqrt{\frac{3}{2}}v_{f\beta}^{*}$	$v_{f0}^{*} > -\sqrt{2}v_{f\alpha}^{*}$	$v_{f0}^{*} < \frac{\sqrt{2}}{2}v_{f\alpha}^{*} - \sqrt{\frac{3}{2}}v_{f\beta}^{*}$
P_4	$v_{f0}^{*} < -\sqrt{2}v_{f\alpha}^{*}$ $v_{f0}^{*} > \frac{\sqrt{2}}{2}v_{f\alpha}^{*} - \sqrt{\frac{3}{2}}v_{f\beta}^{*}$	$v_{f0}^{*} < \frac{\sqrt{2}}{2}v_{f\alpha}^{*} - \sqrt{\frac{3}{2}}v_{f\beta}^{*}$ $v_{f0}^{*} > \frac{\sqrt{2}}{2}v_{f\alpha}^{*} + \sqrt{\frac{3}{2}}v_{f\beta}^{*}$	$v_{f0}^{*} > -\sqrt{2}v_{f\alpha}^{*}$	$v_{f0}^{*} < \frac{\sqrt{2}}{2}v_{f\alpha}^{*} + \sqrt{\frac{3}{2}}v_{f\beta}^{*}$
P_5	$v_{f0}^{*} < -\sqrt{2}v_{f\alpha}^{*}$ $v_{f0}^{*} > \frac{\sqrt{2}}{2}v_{f\alpha}^{*} + \sqrt{\frac{3}{2}}v_{f\beta}^{*}$	$v_{f0}^{*} < \frac{\sqrt{2}}{2}v_{f\alpha}^{*} - \sqrt{\frac{3}{2}}v_{f\beta}^{*}$ $v_{f0}^{*} > -\sqrt{2}v_{f\alpha}^{*}$	$v_{f0}^{*} > \frac{\sqrt{2}}{2}v_{f\alpha}^{*} - \sqrt{\frac{3}{2}}v_{f\beta}^{*}$	$v_{f0}^{*} < \frac{\sqrt{2}}{2}v_{f\alpha}^{*} + \sqrt{\frac{3}{2}}v_{f\beta}^{*}$
P_6	$v_{f0}^{*} < \frac{\sqrt{2}}{2}v_{f\alpha}^{*} - \sqrt{\frac{3}{2}}v_{f\beta}^{*}$ $v_{f0}^{*} > \frac{\sqrt{2}}{2}v_{f\alpha}^{*} + \sqrt{\frac{3}{2}}v_{f\beta}^{*}$	$v_{f0}^{*} < \frac{\sqrt{2}}{2}v_{f\alpha}^{*} + \sqrt{\frac{3}{2}}v_{f\beta}^{*}$ $v_{f0}^{*} > -\sqrt{2}v_{f\alpha}^{*}$	$v_{f0}^{*} > \frac{\sqrt{2}}{2}v_{f\alpha}^{*} - \sqrt{\frac{3}{2}}v_{f\beta}^{*}$	$v_{f0}^{*} < -\sqrt{2}v_{f\alpha}^{*}$

Table 2.4: Equations of the planes delimiting each tetrahedron

II.4.5.1.3. Projection of the reference voltage vector

The switching times of the switches depend on the spatial state of the voltage vector. For this, the principle of 3D SVM is used, which consists of projecting the desired reference voltage vector onto

the three axes of the αβ0 plane. These projections define the switching times. Figure II.19 shows the projection of the reference voltage vector onto these three adjacent vectors.

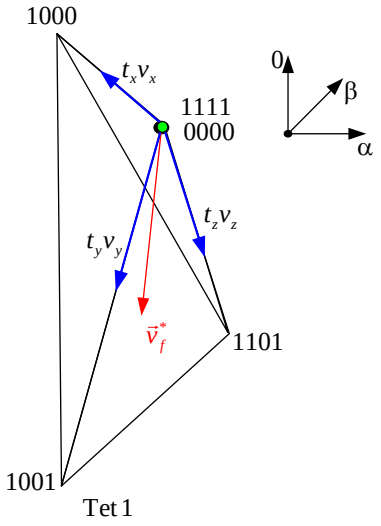


Figure II.19: Projection of the reference vector onto the adjacent vectors.

First, we define an impulse that must meet the following conditions.

- Symmetry.
- The same state at the middle and two ends.
- Defined within a time interval T_s called the sampling time, such that the signal period contains an integer number of samples of duration T_h each.

We denote by t_x, t_y, t_z, and t0 the application times of the inverter state vectors (v_x, v_y, v_z, v_1, v_{16}) which belong to the tetrahedron *i* of the prism *j*, so that $\bar{v}^*$ is equal to the average value of these vectors during a sampling period:

$$\bar{v}^* = \bar{v}_x + \bar{v}_y + \bar{v}_z + \bar{v}_o \qquad \text{(II.70)}$$

With $x, y, z \in \{1,...,14\}$ *et* $o \in [0,15]$

The average of the reference vector is expressed by:

$$\bar{v}^* = \frac{1}{T_h}\int_t^{t+T_h} \vec{v}^* dt \qquad \text{(II.71)}$$

Since the sampling period T_h is well small, the average value of v^* can be considered constant.

Since v_x, v_y, v_z, and v_o are fixed vectors, it yield:

$$\bar{V}_i = \frac{1}{T_h}\int_t^{t+t_i} V_i dt = \frac{1}{T_h} V_i t_i \qquad \text{(II.72)}$$

With *i=x, y, z, 0.*

Therefore, in each tetrahedron, the corresponding durations of the switching vectors are given as:

$$T_h v^* = t_x v_x + t_y v_y + t_z v_z + t_o v_o \qquad \text{(II.73)}$$

By comparing the real and imaginary parts of both members, we obtain:

$$\begin{cases} T_h v_\alpha^* = t_x v_x^\alpha + t_y v_y^\alpha + t_z v_z^\alpha \\ T_h v_\beta^* = t_x v_x^\beta + t_y v_y^\beta + t_z v_z^\beta \\ T_h v_0^* = t_x v_x^0 + t_y v_y^0 + t_z v_z^0 \end{cases} \quad \text{(II.74)}$$

In matrix form, Equation (II.74) is written as:

$$T_h \begin{bmatrix} v_\alpha^* \\ v_\beta^* \\ v_0^* \end{bmatrix} = \begin{bmatrix} v_x^\alpha & v_y^\alpha & v_z^\alpha \\ v_x^\beta & v_y^\beta & v_z^\beta \\ v_x^0 & v_y^0 & v_z^0 \end{bmatrix} \begin{bmatrix} t_x \\ t_y \\ t_z \end{bmatrix} \quad \text{(II.75)}$$

We can simplify equation (II.75) as follows:

$$T_h \begin{bmatrix} v_\alpha^* \\ v_\beta^* \\ v_0^* \end{bmatrix} = V_{dc} [A] \begin{bmatrix} t_x \\ t_y \\ t_z \end{bmatrix} \quad \text{(II.76)}$$

With [A] being a projection matrix of the reference voltage vector onto the non-zero switching state vectors specific to each tetrahedron.

This gives:

$$\begin{bmatrix} t_x \\ t_y \\ t_z \end{bmatrix} = \frac{T_h}{V_{dc}} [A]^{-1} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \\ v_0^* \end{bmatrix} \quad \text{(II.77)}$$

We apply the zero vectors for the remainder of the switching period, each for half of this time. Thus:

$$t_0 = T_h - t_x - t_y - t_z \quad \text{(II.78)}$$

Table (2.5) provides the projection matrix $[A]^{-1}$ for the set of tetrahedra:

	Tet 1	Tet 2	Tet 3	Tet 4
P_1	$\begin{matrix} \frac{\sqrt{2}}{\sqrt{3}} & 0 & \frac{1}{\sqrt{3}} \\ \frac{1}{\sqrt{6}} & -\frac{\sqrt{2}}{2} & -\frac{1}{\sqrt{3}} \\ 0 & \sqrt{2} & 0 \end{matrix}$	$\begin{matrix} \frac{\sqrt{3}}{\sqrt{2}} & -\frac{\sqrt{2}}{2} & 0 \\ -\frac{1}{\sqrt{6}} & \frac{\sqrt{2}}{2} & \frac{1}{\sqrt{3}} \\ \frac{1}{\sqrt{6}} & \frac{\sqrt{2}}{2} & -\frac{1}{\sqrt{3}} \end{matrix}$	$\begin{matrix} \frac{\sqrt{3}}{\sqrt{2}} & -\frac{\sqrt{2}}{2} & 0 \\ 0 & \sqrt{2} & 0 \\ -\frac{1}{\sqrt{6}} & -\frac{\sqrt{2}}{2} & \frac{1}{\sqrt{3}} \end{matrix}$	$\begin{matrix} \frac{\sqrt{3}}{\sqrt{2}} & -\frac{\sqrt{2}}{2} & 0 \\ 0 & \sqrt{2} & 0 \\ -\frac{\sqrt{2}}{\sqrt{3}} & 0 & -\frac{1}{\sqrt{3}} \end{matrix}$
P_2	$\begin{matrix} \frac{\sqrt{2}}{\sqrt{3}} & 0 & \frac{1}{\sqrt{3}} \\ \frac{1}{\sqrt{6}} & \frac{\sqrt{2}}{2} & -\frac{1}{\sqrt{3}} \\ -\frac{\sqrt{3}}{\sqrt{2}} & \frac{\sqrt{2}}{2} & 0 \end{matrix}$	$\begin{matrix} \frac{\sqrt{3}}{\sqrt{2}} & \frac{\sqrt{2}}{2} & 0 \\ -\frac{1}{\sqrt{6}} & \frac{\sqrt{2}}{2} & \frac{1}{\sqrt{3}} \\ -\frac{\sqrt{2}}{\sqrt{3}} & 0 & -\frac{1}{\sqrt{3}} \end{matrix}$	$\begin{matrix} \frac{\sqrt{3}}{\sqrt{2}} & \frac{\sqrt{2}}{2} & 0 \\ -\frac{\sqrt{3}}{\sqrt{2}} & \frac{\sqrt{2}}{2} & 0 \\ -\frac{1}{\sqrt{6}} & -\frac{\sqrt{2}}{2} & \frac{1}{\sqrt{3}} \end{matrix}$	$\begin{matrix} \frac{\sqrt{3}}{\sqrt{2}} & \frac{\sqrt{2}}{2} & 0 \\ -\frac{\sqrt{3}}{\sqrt{2}} & \frac{\sqrt{2}}{2} & 0 \\ \frac{1}{\sqrt{6}} & -\frac{\sqrt{2}}{2} & -\frac{1}{\sqrt{3}} \end{matrix}$
P_3	$\begin{matrix} -\frac{1}{\sqrt{6}} & \frac{\sqrt{2}}{2} & \frac{1}{\sqrt{3}} \\ \frac{1}{\sqrt{6}} & \frac{\sqrt{2}}{2} & -\frac{1}{\sqrt{3}} \\ -\frac{\sqrt{3}}{\sqrt{2}} & -\frac{\sqrt{2}}{2} & 0 \end{matrix}$	$\begin{matrix} 0 & \sqrt{2} & 0 \\ -\frac{1}{\sqrt{6}} & -\frac{\sqrt{2}}{2} & \frac{1}{\sqrt{3}} \\ -\frac{\sqrt{2}}{\sqrt{3}} & 0 & -\frac{1}{\sqrt{3}} \end{matrix}$	$\begin{matrix} 0 & \sqrt{2} & 0 \\ -\frac{\sqrt{3}}{\sqrt{2}} & -\frac{\sqrt{2}}{2} & 0 \\ \frac{\sqrt{2}}{\sqrt{3}} & 0 & \frac{1}{\sqrt{3}} \end{matrix}$	$\begin{matrix} 0 & \sqrt{2} & 0 \\ -\frac{\sqrt{3}}{\sqrt{2}} & -\frac{\sqrt{2}}{2} & 0 \\ \frac{1}{\sqrt{6}} & -\frac{\sqrt{2}}{2} & -\frac{1}{\sqrt{3}} \end{matrix}$
P_4	$\begin{matrix} -\frac{1}{\sqrt{6}} & \frac{\sqrt{2}}{\sqrt{2}} & \frac{1}{\sqrt{3}} \\ -\frac{\sqrt{2}}{\sqrt{3}} & 0 & -\frac{1}{\sqrt{3}} \\ 0 & -\sqrt{2} & 0 \end{matrix}$	$\begin{matrix} -\frac{\sqrt{3}}{\sqrt{2}} & \frac{\sqrt{2}}{2} & 0 \\ -\frac{1}{\sqrt{6}} & -\frac{\sqrt{2}}{2} & \frac{1}{\sqrt{3}} \\ \frac{1}{\sqrt{6}} & -\frac{\sqrt{2}}{2} & -\frac{1}{\sqrt{3}} \end{matrix}$	$\begin{matrix} -\frac{\sqrt{3}}{\sqrt{2}} & \frac{\sqrt{2}}{2} & 0 \\ 0 & -\sqrt{2} & 0 \\ \frac{\sqrt{2}}{\sqrt{3}} & 0 & \frac{1}{\sqrt{3}} \end{matrix}$	$\begin{matrix} -\frac{\sqrt{3}}{\sqrt{2}} & \frac{\sqrt{2}}{2} & 0 \\ 0 & -\sqrt{2} & 0 \\ \frac{1}{\sqrt{6}} & \frac{\sqrt{2}}{2} & -\frac{1}{\sqrt{3}} \end{matrix}$
P_5	$\begin{matrix} -\frac{1}{\sqrt{6}} & -\frac{\sqrt{2}}{2} & \frac{1}{\sqrt{3}} \\ -\frac{\sqrt{2}}{\sqrt{3}} & 0 & -\frac{1}{\sqrt{3}} \\ \frac{\sqrt{3}}{\sqrt{2}} & -\frac{\sqrt{2}}{2} & 0 \end{matrix}$	$\begin{matrix} -\frac{\sqrt{3}}{\sqrt{2}} & -\frac{\sqrt{2}}{2} & 0 \\ \frac{\sqrt{2}}{\sqrt{3}} & 0 & \frac{1}{\sqrt{3}} \\ \frac{1}{\sqrt{6}} & -\frac{\sqrt{2}}{2} & -\frac{1}{\sqrt{3}} \end{matrix}$	$\begin{matrix} -\frac{\sqrt{3}}{\sqrt{2}} & -\frac{\sqrt{2}}{2} & 0 \\ \frac{\sqrt{3}}{\sqrt{2}} & -\frac{\sqrt{2}}{2} & 0 \\ -\frac{1}{\sqrt{6}} & \frac{\sqrt{2}}{2} & \frac{1}{\sqrt{3}} \end{matrix}$	$\begin{matrix} -\frac{\sqrt{3}}{\sqrt{2}} & -\frac{\sqrt{2}}{2} & 0 \\ \frac{\sqrt{3}}{\sqrt{2}} & -\frac{\sqrt{2}}{2} & 0 \\ \frac{1}{\sqrt{6}} & \frac{\sqrt{2}}{2} & -\frac{1}{\sqrt{3}} \end{matrix}$

P_6	$\begin{matrix} -\frac{1}{\sqrt{6}} & -\frac{\sqrt{2}}{2} & \frac{1}{\sqrt{3}} \\ \frac{1}{\sqrt{6}} & -\frac{\sqrt{2}}{2} & -\frac{1}{\sqrt{3}} \\ \frac{\sqrt{3}}{\sqrt{2}} & \frac{\sqrt{2}}{2} & 0 \end{matrix}$	$\begin{matrix} 0 & -\sqrt{2} & 0 \\ \frac{\sqrt{2}}{\sqrt{3}} & 0 & \frac{1}{\sqrt{3}} \\ \frac{1}{\sqrt{6}} & \frac{\sqrt{2}}{2} & -\frac{1}{\sqrt{3}} \end{matrix}$	$\begin{matrix} 0 & -\sqrt{2} & 0 \\ \frac{\sqrt{3}}{\sqrt{2}} & \frac{\sqrt{2}}{2} & 0 \\ -\frac{1}{\sqrt{6}} & \frac{\sqrt{2}}{2} & \frac{1}{\sqrt{3}} \end{matrix}$	$\begin{matrix} 0 & -\sqrt{2} & 0 \\ \frac{\sqrt{3}}{\sqrt{2}} & \frac{\sqrt{2}}{2} & 0 \\ -\frac{\sqrt{2}}{\sqrt{3}} & 0 & -\frac{1}{\sqrt{3}} \end{matrix}$

Table 2.5: Projection matrix [A] for each tetrahedron to determine the duty cycles

II.4.5.1.4. Control pulses Generation

Figure II.20 indicates the switching functions Fj associated with the upper switches of the inverter over a sampling period for the voltage vectors to be applied in the four tetrahedra of the first prism. It is noted that each switch changes its state only twice per sampling period [131].

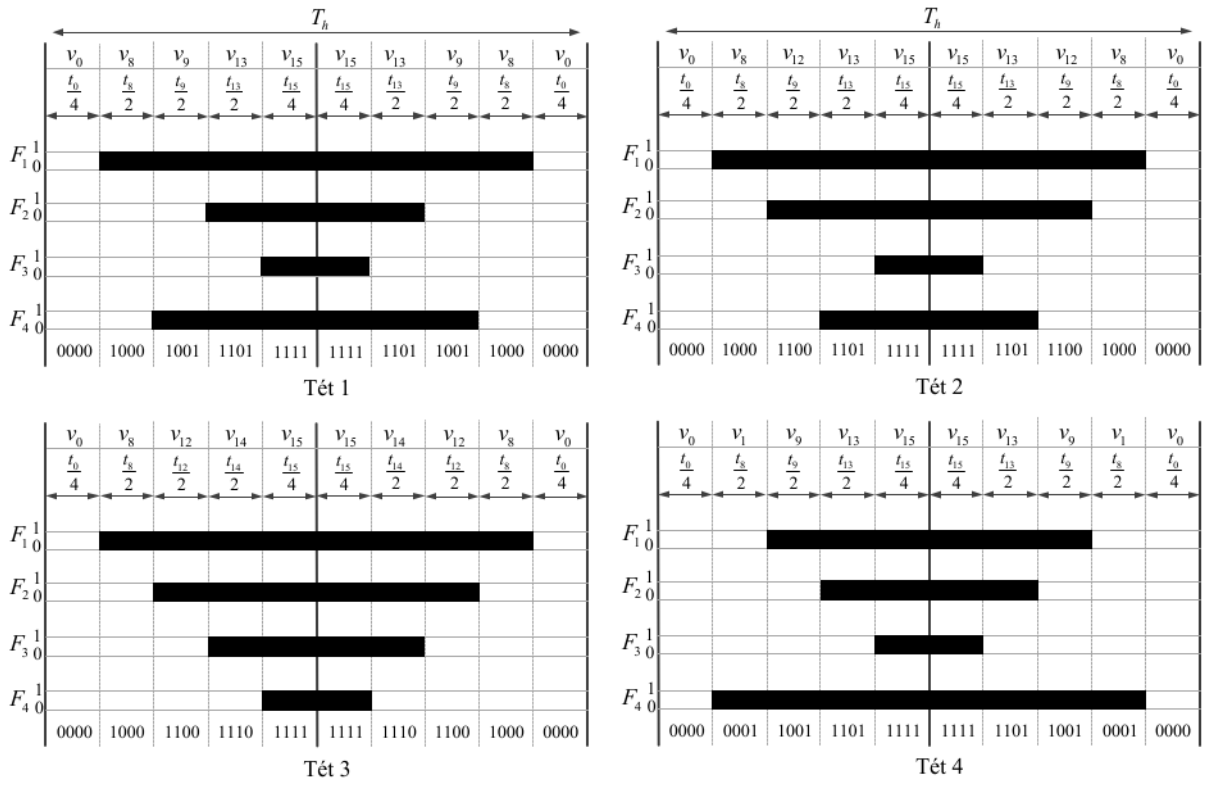


Figure II.20: Shapes of the switching functions F_j for the four tetrahedra of the first prism in three-dimensional vector modulation control (3DSVM).

II.4.6. Simulation results and discussion

II.4.6.1. System performance assessment under sudden solar irradiance and nonlinear load changes

The objective of this test is to evaluate the overall performance of the PV grid connected 4LI in terms of power balance, reactive power compensation, harmonic eliminations, and tracking references with respect to sudden changes in solar irradiance and single phase nonlinear loads, the following scenario is considered:

1. From 0 < *t* <0.2 s, Stable operation at 1000 W/s irradiance with 4 Ω and 10 mH single phase nonlinear loads;
2. From 0.2 < *t* <0.3 s, Irradiance decrease from 1000 W/s to 600 W/s with 4 Ω and 10 mH single phase nonlinear loads;
3. From 0.3 < *t* <0.4 s, Irradiance increase from 600 W/s to 400 W/s with 4 Ω and 10 mH single phase nonlinear loads;
4. From 0.4< *t* <0.5 s, Irradiance increase from 400 W/s to 800 W/s with 4 Ω and 10 mH single phase nonlinear loads;
5. From 0.6 < *t* <0.75 s, Load change from 4 Ω and 10 mH to 2 Ω and 5 mH with 1000 W/s Irradiance.

The simulation results of this control method are shown in Figures. II.21 (a) to (h), which respectively show: (a) the active powers of the system, (b) the reactive powers of the system, (c) the output currents of the 4LI, (d) the 4LI natural current with load natural current, (e) the three-phase grid currents, (f) the first-phase grid voltage along with its current, (g) first-phase 4LI output current along with its reference, and (h) the DC bus voltage with its reference. The simulation illustrates the system's ability to maintain stability and power quality under dynamic different considered operating conditions:

Figure II.21-a depicts the active power distribution among the PV grid-connected 4LI system components (P_{grid}, P_{load}, $P_{inverter}$, and P_{PV}). It can be seen from this figure that before the variation in solar irradiance ($0 \leq t \leq 0.2$ s), the system active power flow stabilizes with the load active power demand (P_{load}) at approximately 30 kW, while P_{PV} stabilizes at around 9 kW. The 4LI inject the active power from the PV generator to the grid ($P_{inverters}$ at ~12 kW), and because this active power is less than the active power required to satisfy the load demand, the remaining active power (around 22 kW) is absorbed from the three-phase grid.

During the second operation phase when the solar irradiance decreases ($0.2 \leq t \leq 0.3$ s) and ($0.3 \leq t \leq 0.4$ s), the PV power output adjusts accordingly and decreases to approximately 7 kW and 5kW, respectively. As shown in figure (II.21-a), the grid power increases to around 26 kW in period ($0.2 \leq t \leq 0.3$ s) and to around 28.5 kW in period ($0.3 \leq t \leq 0.4$ s) to maintain nonlinear load active power supply and guarantee system active power flow stability (the load continues to draw constant power).

When the solar irradiance mode increases during the phase ($0.4 \leq t \leq 0.5$ s) and further increases during the phase ($0.5 \leq t \leq 0.6$ s), the PV power output adjusts accordingly, increasing to around 10 kW during phase ($0.4 \leq t \leq 0.5$ s) and to approximately 12 kW during the operating phase ($0.5 \leq t \leq 0.6$ s). The grid power decreases proportionally during both these operation phases to maintain the nonlinear active power supply and guarantee system active power flow stability.

The most dramatic change occurs after t=0.6s with the nonlinear load change, where P_{load} increases substantially to approximately 58 kW, and P_{grid} increases to about 58 kW, indicating the system's ability to handle higher load demands while maintaining system active power flow stability. During this operation phase, the $P_{inverter}$ remains around 0 kW, slightly lower than P_{PV}, suggesting that the 4LI cannot inject the active power produced by the PV generator, likely due to the increased nonlinear load reactive power demand. In this case, the 4LI allocate part of its capacity to compensate for the nonlinear load reactive power demand while guaranteeing system active and reactive power flow stability.

Figure (II.21-b) shows the system reactive power distributions among the PV grid-connected 4LI's system components (Q_{grid}, Q_{load}, and $Q_{inverter}$). From this figure, we can clearly see that the 4LI compensate for all the reactive power demanded by the nonlinear load and maintains fairly constant reactive power throughout irradiance changes, with Q_{grid} near zero, suggesting good power factor control. When the nonlinear load is changed at t = 0.6 s during the fourth operating phase, significant jump in Q_{load} and $Q_{inverter}$ are accor, demonstrating the increased reactive power demand of the new

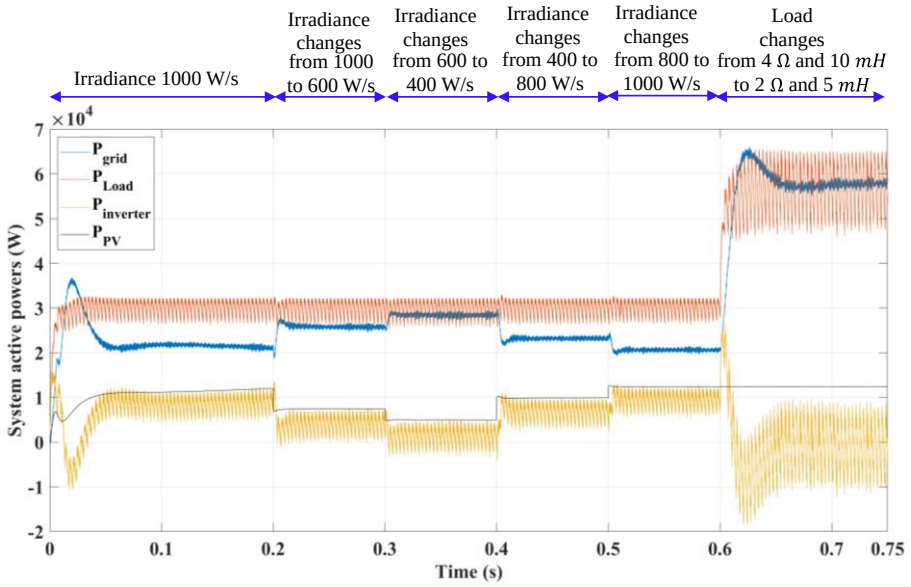
load and the 4LI are compensate for all the reactive power demanded by the new nonlinear load and maintains Q_{grid} near zero, suggesting good power factor control. Despite the fluctuating solar input, the system continues to provide reactive power support, particularly to compensate for the nonlinear loads. The ability of the PVG 4LI to maintain reactive power injection illustrates its role in power factor correction at the PCC.

The study state and dynamic performance of the 4LI under sudden variations in irradiance and single phase nonlinear load conditions is illustrated through their outputs, including the three-phase and neutral line currents in Figures II.21 (c, d,e and f). During the initial period (0–0.2 s) under stable irradiance of 1000 W/m² and a nonlinear single-phase load (4 Ω, 10 mH), the 4LI outputs track perfectly the nonlinear single-phase load harmonics, as shown in Figures II.21 (d and e). This indicates effective harmonic mitigation and precise reference tracking, highlighting the capability of the control strategy to compensate for the nonlinearities introduced by the load. As irradiance decreases sequentially to 600 W/m² during the second period (0.2–0.3 s) and then to 400 W/m² during the third period (0.3–0.4 s), the 4LI output currents exhibit a corresponding reduction in amplitude, while maintaining precise reference tracking operation. This demonstrates the system's ability to adapt to varying PVG output power. When irradiance recovers to 800 W/m² (0.4–0.5 s), the output currents respond appropriately with an increase in amplitude, confirming the controller's effective tracking of the available PV power. A significant dynamic occurs between 0.6–0.75 s when the single phase nonlinearload changes from 4 Ω/10 mH to 2 Ω/5 mH under restored irradiance (1000 W/m²). Here, the 4LI output currents increase sharply in amplitude due to the heavier nonlinear single phase load and the overall current profiles remain relatively smooth, indicating that the controller continues to maintain acceptable harmonic performance and stability under abrupt loading conditions. Additionally, the 4LI neutral current maintains a near-perfect match, confirming the four-leg configuration's effectiveness in managing zero-sequence and neutral currents in the presence of single phase nonlinear loading, as shown Figure II.21 e.

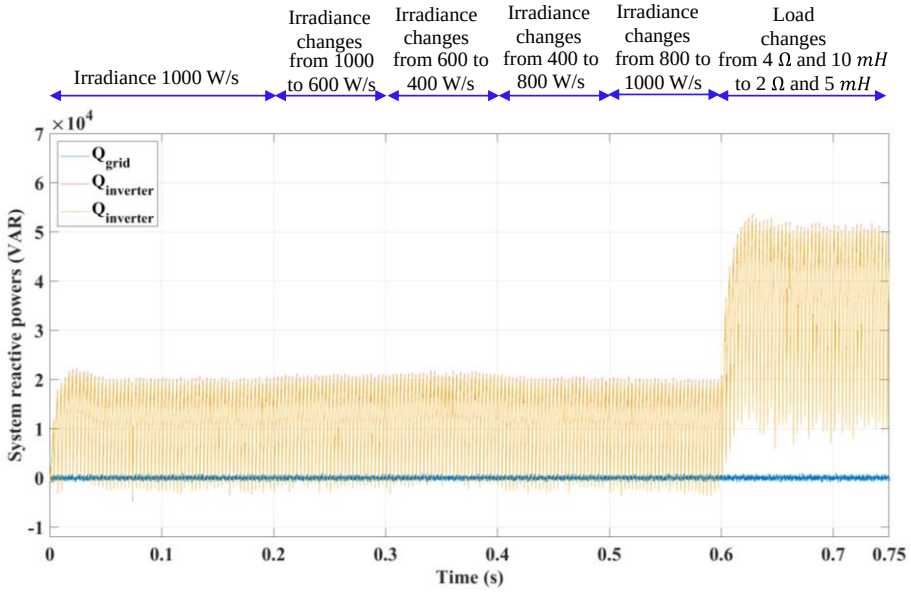
The behavior of the grid currents i_{gabc} under these dynamic operating conditions is shown in Figures II.21 (f), revealing the robustness of the system and control strategy in maintaining power quality during disturbances. In the steady state from 0 to 0.2 s, the grid currents are balanced and sinusoidal despite the presence of single-phase nonlinear loads, confirming effective harmonic compensation by the 4LI. As irradiance is reduced stepwise from 1000 W/m² to 600 W/m² (0.2–0.3 s) and then further to 400 W/m² (0.3–0.4 s), a corresponding decrease in the amplitude of the grid currents is observed. However, the waveforms remain highly sinusoidal and well-synchronized, demonstrating the controller's ability to manage power flow effectively while suppressing harmonics. When irradiance is ramped back to 800 W/m² between 0.4–0.5 s, the grid currents increase in amplitude accordingly, with negligible distortion. The grid current amplitude adapts smoothly to the changing PVG power without introducing transients, indicating a seamless power balancing response by the system. The most notable disturbance occurs between 0.6–0.75 s, when the load shifts to a more demanding 2 Ω / 5 mH nonlinear profile while the irradiance returns to 1000 W/m². This sudden increase in nonlinear loads results in a significant rise in grid current amplitude, which is handled effectively by the 4LI. The waveforms remain balanced and sinusoidal, with minimal harmonic content, highlighting the system's proficiency in mitigating single phase nonlinear loading effects through harmonic suppression and reactive power compensation.

Figure II.21 (g) presents the first phase grid voltage (v_{ga}/10) and its current (i_{ga}) waveforms. It can be seen from this figure that the grid current is always in phase with its voltage under different solar irradiance and single phase nonlinear loading, maintaining proper phase relationship despite these conditions, indicating effective power factor control.

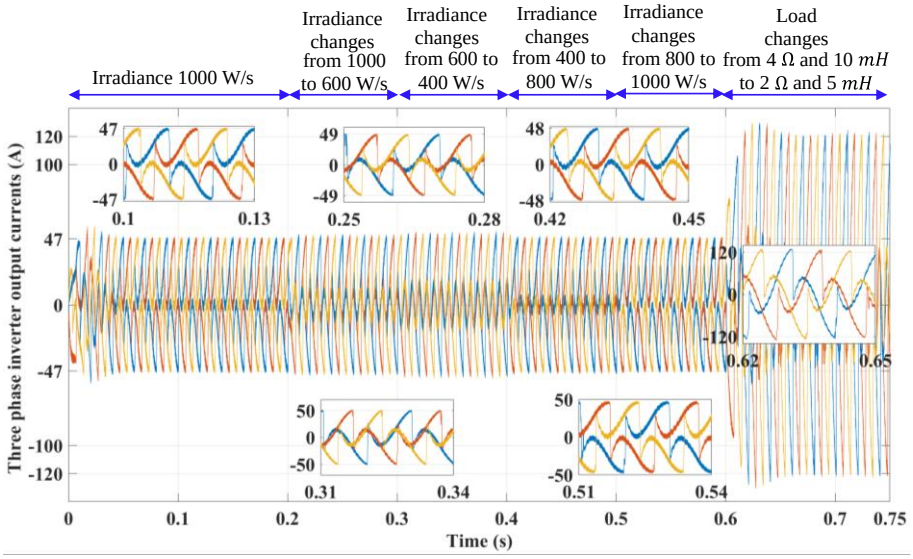
As shown in Figures II.21 (g), the 4LI input DC bus voltage closely follow its respective reference, even during rapid irradiance and load shifts. This demonstrates robust control strategy, ensuring system reliability and stable operation.


Irradiance 1000 W/s
Irradiance changes from 1000 to 600 W/s
Irradiance changes from 600 to 400 W/s
Irradiance changes from 400 to 800 W/s
Irradiance changes from 800 to 1000 W/s
Load changes from 4 Ω and 10 mH to 2 Ω and 5 mH
×10^4
P_grid
P_Load
P_inverter
P_PV
System active powers (W)
Time (s)

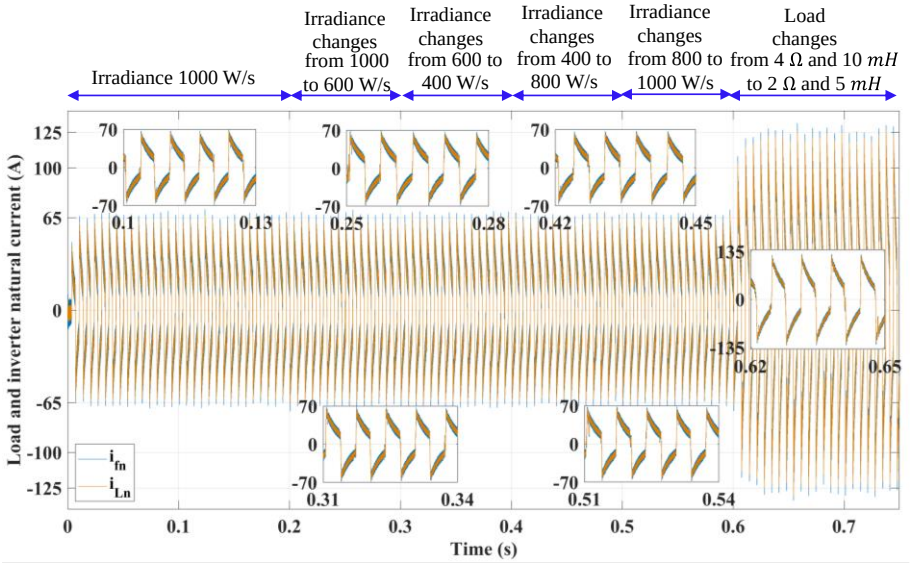
(a)


Irradiance 1000 W/s
Irradiance changes from 1000 to 600 W/s
Irradiance changes from 600 to 400 W/s
Irradiance changes from 400 to 800 W/s
Irradiance changes from 800 to 1000 W/s
Load changes from 4 Ω and 10 mH to 2 Ω and 5 mH
×10^4
Q_grid
Q_inverter
Q_inverter
System reactive powers (VAR)
Time (s)

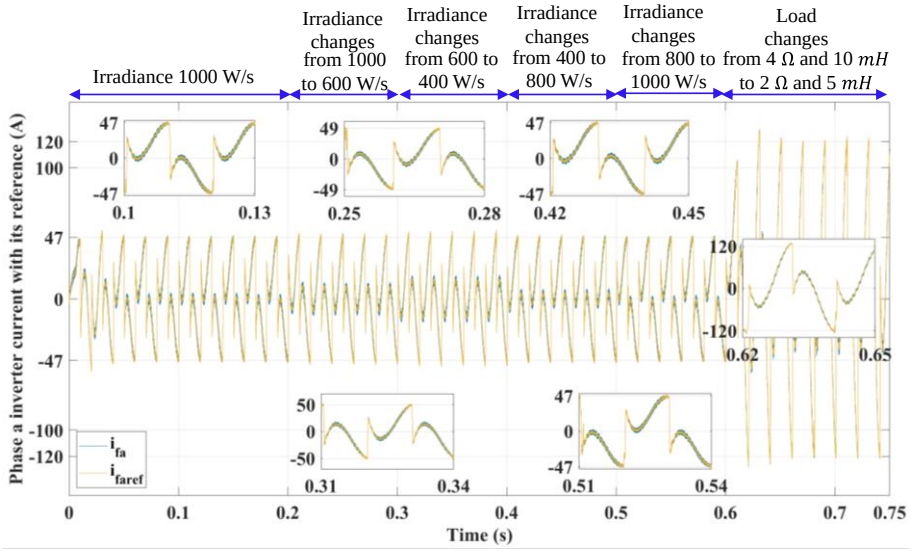
(b)


Irradiance 1000 W/s
Irradiance changes from 1000 to 600 W/s
Irradiance changes from 600 to 400 W/s
Irradiance changes from 400 to 800 W/s
Irradiance changes from 800 to 1000 W/s
Load changes from 4 Ω and 10 mH to 2 Ω and 5 mH
Three phase inverter output currents (A)
Time (s)

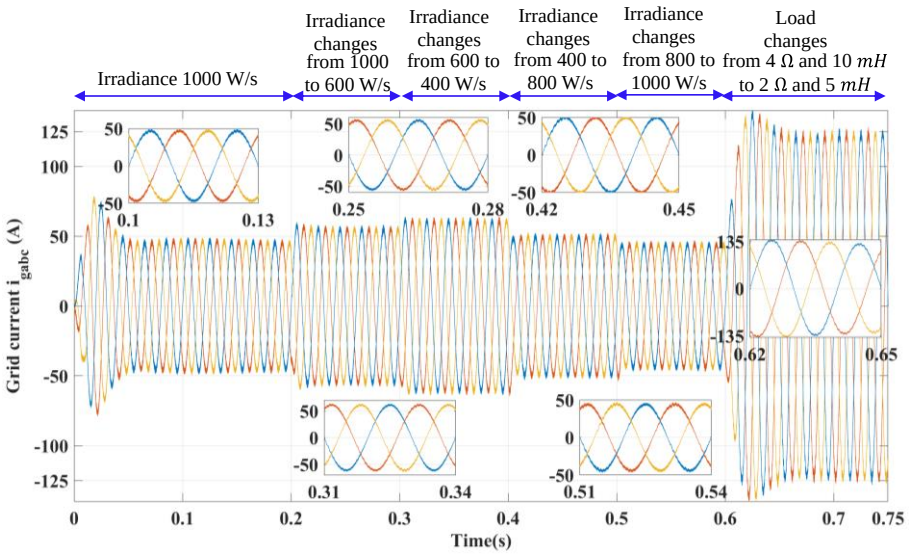
(c)


Irradiance 1000 W/s
Irradiance changes from 1000 to 600 W/s
Irradiance changes from 600 to 400 W/s
Irradiance changes from 400 to 800 W/s
Irradiance changes from 800 to 1000 W/s
Load changes from 4 Ω and 10 mH to 2 Ω and 5 mH
Load and inverter natural current (A)
i_fn
i_Ln
Time (s)

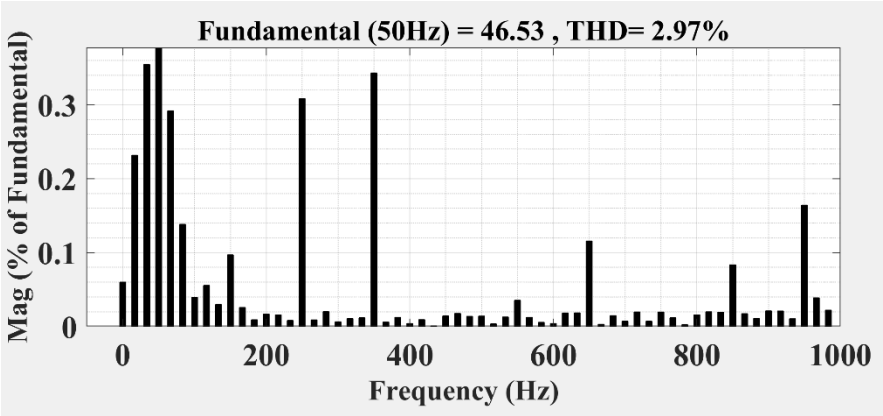
(d)


Irradiance 1000 W/s
Irradiance changes from 1000 to 600 W/s
Irradiance changes from 600 to 400 W/s
Irradiance changes from 400 to 800 W/s
Irradiance changes from 800 to 1000 W/s
Load changes from 4 Ω and 10 mH to 2 Ω and 5 mH
Phase a inverter current with its reference (A)
i_fa
i_faref
Time (s)

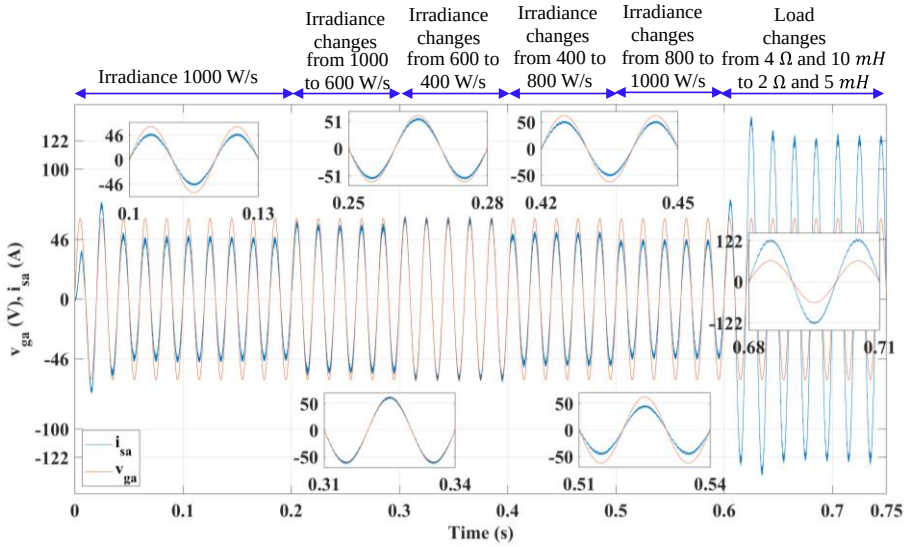
(e)


Irradiance 1000 W/s
Irradiance changes from 1000 to 600 W/s
Irradiance changes from 600 to 400 W/s
Irradiance changes from 400 to 800 W/s
Irradiance changes from 800 to 1000 W/s
Load changes from 4 Ω and 10 mH to 2 Ω and 5 mH
Grid current i_{gabc} (A)
Time(s)

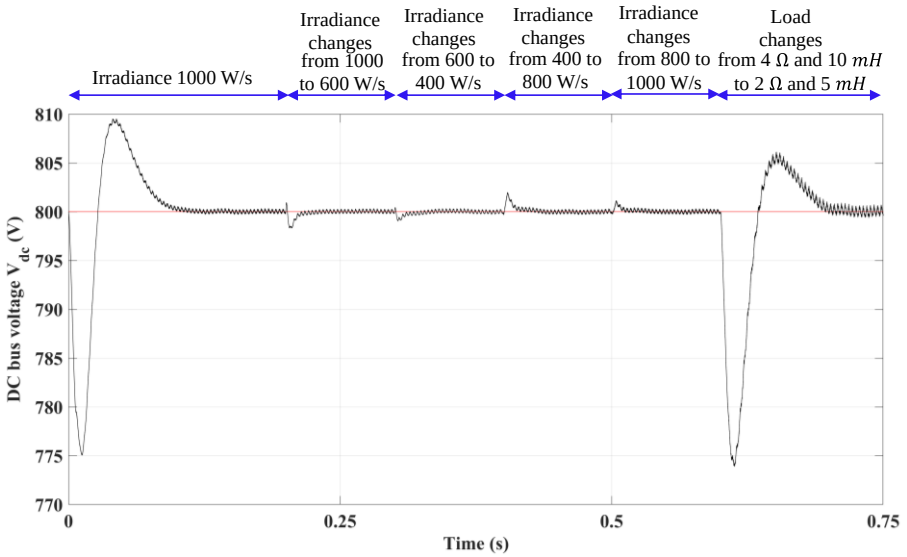
(f)


Fundamental (50Hz) = 46.53 , THD= 2.97%
Mag (% of Fundamental)
Frequency (Hz)

(e)



(f)



(j)

Figure II.21. Performance of the overall system under sudden changes in solar irradiance and single phase nonlinear loads.

II.4.5. Control of the 4LI-based PVG grid connected for reactive power compensation mode under linear load

In this case, to support the reactive power demand of linear loads connected to the grid, a PVG system equipped with a 4LI is used to serve as a dedicated reactive power compensator, as shown in Figure II.22. Linear loads such as induction motors, transformers, and fluorescent lamps, typically draw not only active power but also significant reactive power from the grid. In a conventional system, this reactive power burden is entirely supported by the utility grid, which can lead to voltage drops, increased transmission losses, and reduced system efficiency. In our application, the PVG does not supply active power to the loads but focuses solely on injecting reactive power as needed. The grid continues to supply all active power requirements, while the PVG dynamically compensates the reactive portion, improving the power factor and enhancing voltage profiles at the PCC. This

approach not only reduces the burden on the utility but also leverages renewable energy infrastructure to improve power quality without feeding active power into the grid. As shown in this figure, the only difference between this mode and the previous one is the 4LI's output current reference detections, while they both modes employ the same essential components discussed previously, including the synchronization method, output current and DC voltage regulation loops, and the PWM signal generations method.

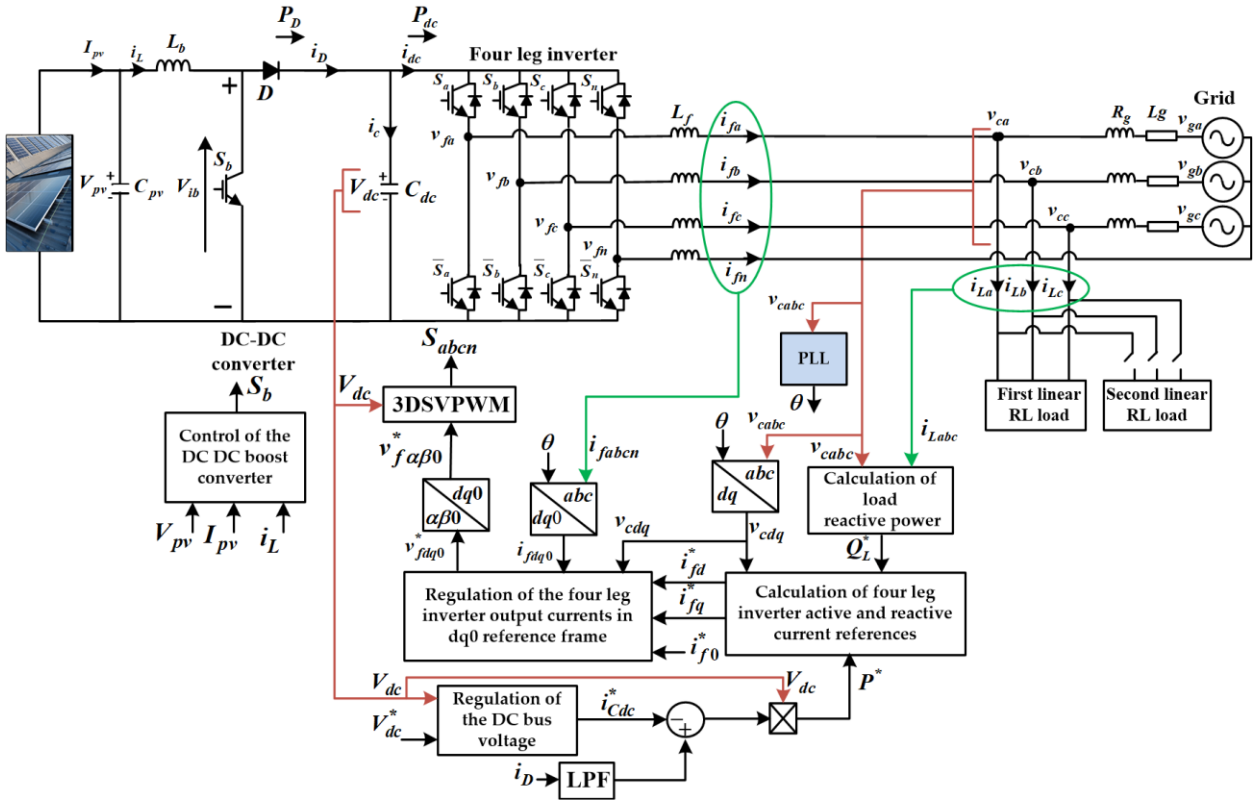


Figure II.22: Overall control diagram of the PV grid-connected 4LI system for reactive power compensation under three phase linear load.

II.5.1. Detection of the 4LI's output current references in mode reactive power compensation

In this mode, the loads are balanced and linear, producing negligible harmonic distortion. As a result, the control objective focuses exclusively on reactive power compensation. The generation of the 4LI's current references begins with measuring the load voltage (at PCC) and determining the desired level of reactive power to be compensated, typically based on a reactive power setpoint or through a power factor control loop. The reactive component of the current is then generated, commonly using the dq0 reference frame, where the d0-axes reference currents are set to zero and the q-axis current is regulated to achieve the desired compensation. Afterward, the regulation and decoupling 4LI output current control loop's outputs are transformed back into the αβ0 frame and used as the output voltage references of the 4LI that can transformed into PWM singles using the 3DSVM. Since harmonic extraction is not required in this mode, the control strategy is simpler and computationally less intensive compared to first mode.

In this mode, the p–q–o theory is also employed to generate the 4LI's current references. The 4LI can injects the active power calculated by equation (II.79), to ensure the stability of the DC bus voltage, while simultaneously compensating the total reactive power of the load q_L^*, as determined by equation (II.80).

$$p^* = V_{dc} I_{dc}^* = v_{cd} i_{Ld} + v_{cq} i_{Lq} \quad \text{(II.79)}$$

$$q_L^* = v_{cd} i_{Lq} - v_{cq} i_{Ld} \quad \text{(II.80)}$$

where i_{Ld} and i_{Lq} denote the direct and quadrature components of the load current in the dq0 frame, respectively.

Based on Equations (II.79) and (II.80), the 4LI output current references can be calculated as follows:

$$\begin{bmatrix} i_{fd}^* \\ i_{fq}^* \\ i_{fo}^* \end{bmatrix} = \frac{1}{v_{cd}^2 + v_{cq}^2} \begin{bmatrix} v_{cd} & -v_{cq} & 0 \\ v_{cq} & v_{cd} & 0 \\ 0 & 0 & v_{cd}^2 + v_{cq}^2 \end{bmatrix} \begin{bmatrix} p^* \\ q_L^* \\ i_{Lo}^* \end{bmatrix} \quad \text{(II.81)}$$

II.5.2. Simulation Results and Discussion

The objective of this test is to evaluate the overall performance of the PV grid connected 4LI in terms of power balance, reactive power compensation, and tracking references with respect to sudden changes in solar irradiance and linear loads, the following scenario is considered:

- From $0 < t < 0.25$ s, Stable operation at 1000 W/s irradiance with 4 Ω and 10 mH linear loads;
- From $0.25 < t < 0.5$ s, Irradiance decrease from 1000 W/s to 600 W/s with 4 Ω and 10 mH linear loads;
- From $0.5 < t < 0.75$ s, Irradiance increase from 600 W/s to 400 W/s with 4 Ω and 10 mH linear loads;
- From $0.75 < t < 1$ s, Irradiance increase from 400 W/s to 800 W/s with 4 Ω and 10 mH linear loads;
- From $1 < t < 1.5$ s, Load change from 4 Ω and 10 mH to 2 Ω and 5 mH with 1000 W/s Irradiance.

The parameters of system and controllers are given in Table A.1 and A2 (Appendix A).

Figure. II.23 presents the active power exchange among the PVG, 4LI, and the grid. As expected, the grid supplies the bulk of the active load demand, while the PVG contributes only a small portion. This contribution is not intended to feed active power to the load but to stabilize the DC bus voltage as shown in Figure. II.31. The stability of this exchange, even under irradiance and linear load changes, validates the effectiveness of the DC-bus voltage control loop.

Figure. II.24 illustrates that the reactive power supplied by the PVG via the 4LI almost exactly matches the reactive demand of the load across all operating conditions, which demonstrate that the 4LI dynamically compensates the reactive power drawn by the load. As a result, the reactive power supplied by the grid remains close to zero, confirming that the power factor at the PCC is effectively corrected to near unity.

The three-phase output currents of the 4LI are depicted in Figure. II.25. These currents exhibit sinusoidal waveforms with amplitudes varying according to irradiance and load conditions. The accurate amplitude scaling and waveform tracking reflect the precision of the inner output current control loop in generating and following current references as shown in Figure. II.26 (phase-a output current with its reference). This figure comparing the actual phase-a output current of the 4LI with its reference. The close overlap between the two current confirms the high fidelity of the inner output

current control loop. Acceptable steady-state error and dynamic response are observed, demonstrating that the inner output current control loop effectively handles irradiance and load variations.

The frequency spectra of the inverter output currents are shown in Figure II.27 for two operating intervals:

Low output current amplitude region (0.5–0.75 s): in this region, Figure. II.27a, although the amplitude of fundamental current decreases due to reduced irradiance, harmonic distortion remains within acceptable limits (<5%), confirming good waveform quality under reduced irradiance.

High output current amplitude region (1.25–1.5 s): in this region, Figure. II.27b, the spectrum exhibits low-order harmonics due to the increases of load demand, confirming good waveform quality under increases of load demand.

These indicate that the 3DSVPWM technique with the cascade control loops strategy maintain effective harmonic suppression across operating conditions.

Figure. II.28 shows the three-phase grid currents after compensation. It can be seen that the the grid currents are nearly sinusoidal and significantly reduced in reactive content. This confirms that the 4LI's reactive power injection relieves the utility grid of its reactive burden, improving overall efficiency.

The harmonic spectra of these grid currents in both low and high output current amplitude regions are shown in Figures. II.29a and II.29b. The results of these figures indicate that harmonic distortion in the grid currents is minimal in both amplitude regions and within the acceptable limit (<5%), demonstrating the combined effect of 4LI compensation and the linear load profile. This ensures compliance with power quality standards such as IEEE 519.

The phase-a grid voltage and current waveforms are compared in Figure II.30. As shown in this figure, both the grid current and voltage have nearly in-phase relationship, which confirms that the system can successfully compensate the reactive power, which validates the power factor correction achieved by the PVG-4LI system.

Finally, Figure. II.31 illustrates the regulation of the DC-link voltage. As it can be seen from this figure, despite the variations in irradiance and load, the DC bus voltage is maintained close to its reference value. The acceptable oscillations observed during transitions confirm the responsiveness of the outer DC-bus voltage control loop, which quickly restores stability. Maintaining a stable DC bus voltage is critical to ensuring reliable system operation and continuous reactive power support.

The simulation results comprehensively demonstrate the capability of the PVG grid connected 4LI system to operate as a reactive power compensator under linear load and irradiance conditions. Key findings include:

- The 4LI successfully supplies the full reactive power demand of the linear load, maintaining unity power factor at the grid or PCC.
- The DC-bus voltage remains well-regulated despite irradiance fluctuations and sudden linear load changes.
- The output current control exhibits good reference tracking with acceptable steady-state error.

- The harmonic distortion of both 4LI and grid currents remains withing the acceptable standard (<5%), satisfying power quality requirements.

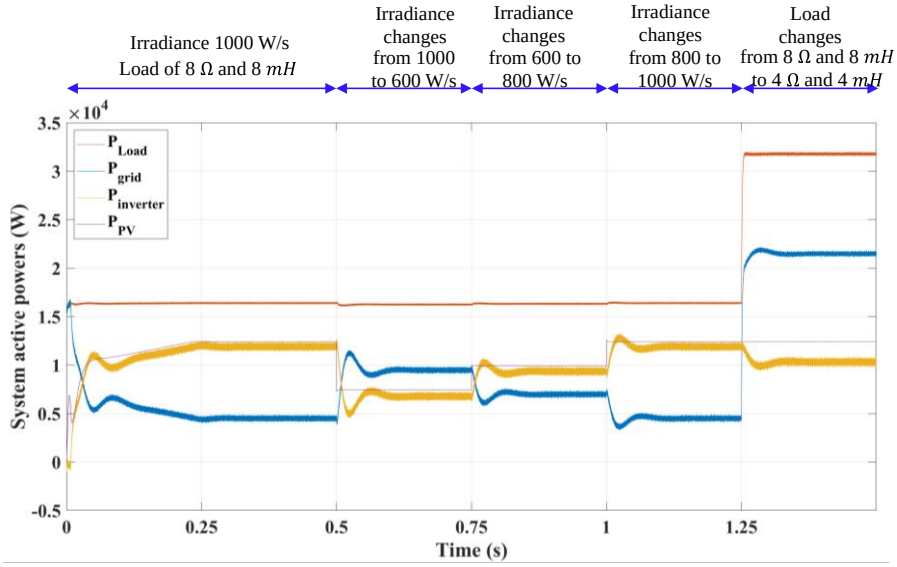


Figure II.23. PV grid connected four leg inverter system active powers.

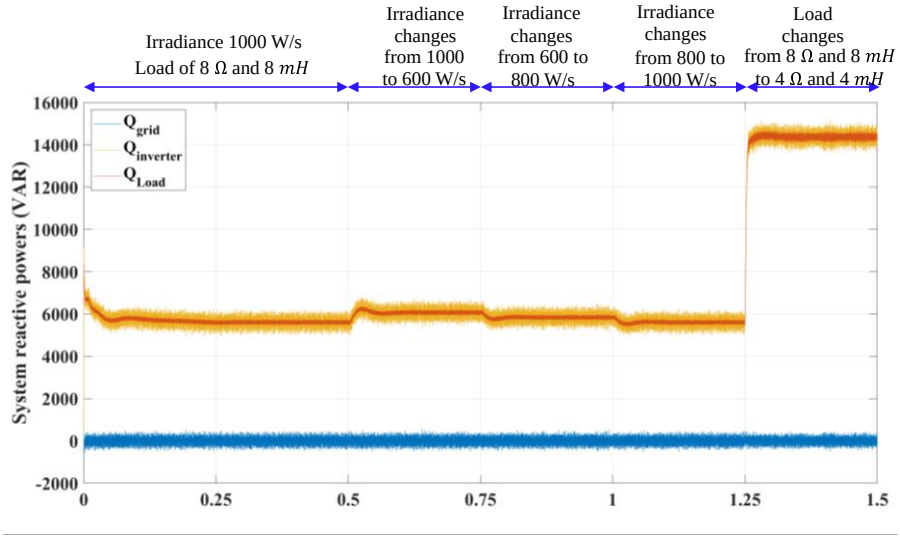


Figure II.24. PV grid connected four leg inverter system powers.

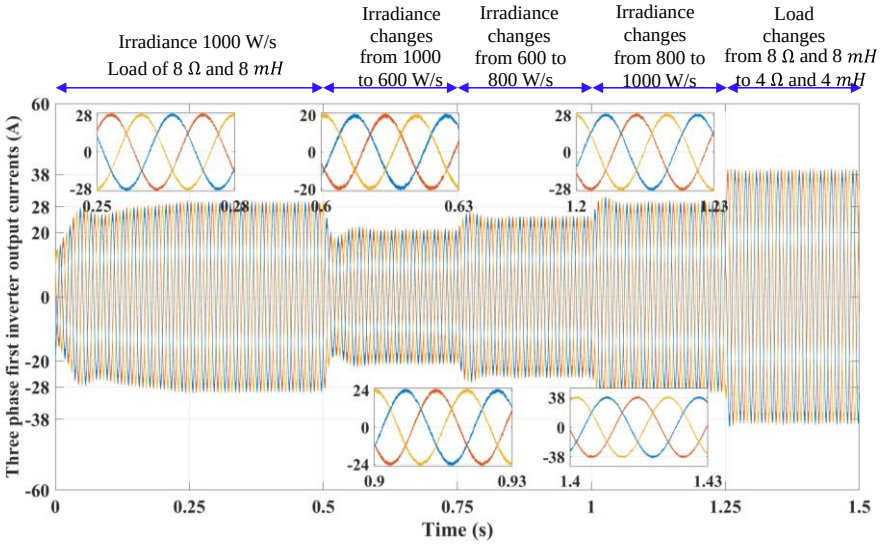


Figure II.25. Four leg inverter output three phase currents.

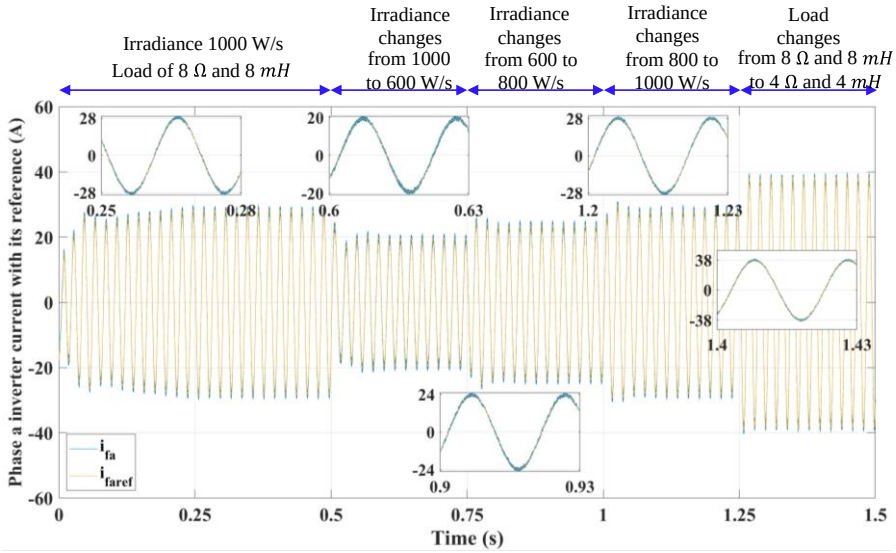
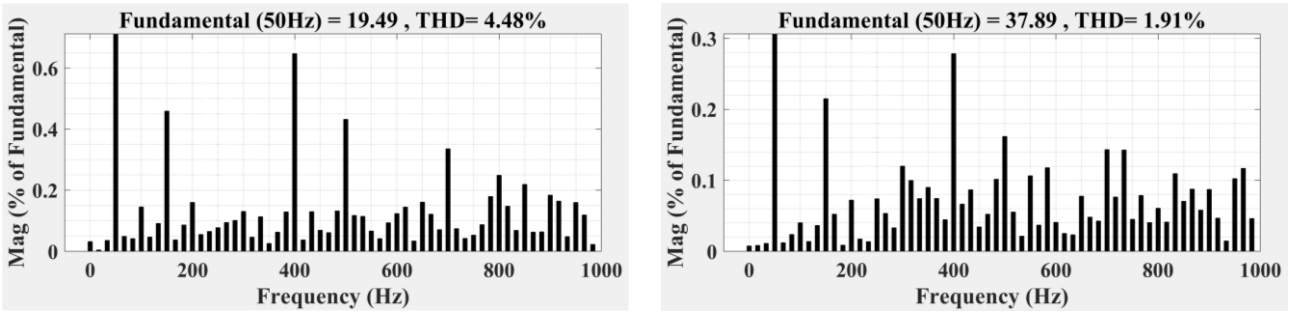


Figure II.26. Phase *a* of Four leg inverter output current with its reference.



(a) **(b)**

Figure II.27. Spectrum harmonic of first phase inverter's output current. (a) In zone of lower amplitude [0.5 0.75 s], (b) In zone of high amplitude [1.25 1.5 s].

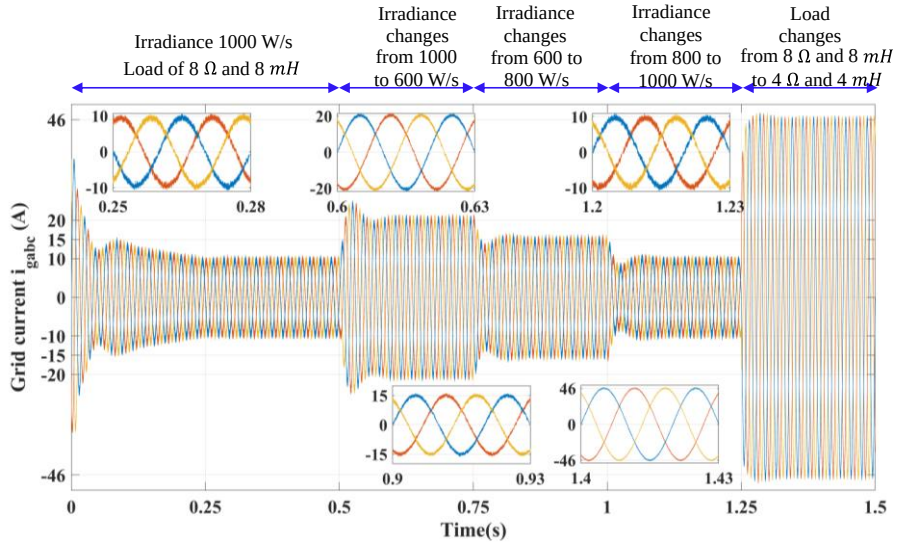
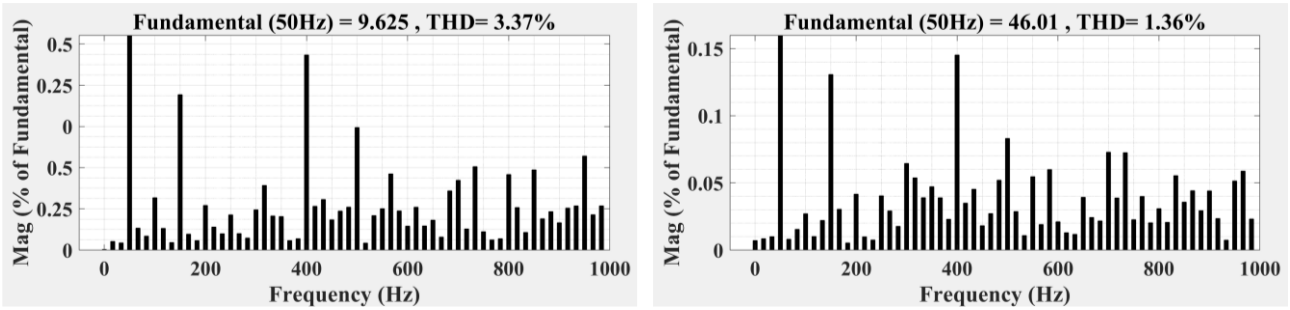


Figure II.28. Three phase grid currents.



(a) **(b)**

Figure II.29. Spectrum harmonic of first phase grid current. (a) In zone of lower amplitude [0.5 0.75 s], (b) In zone of high amplitude [1.25 1.5 s].

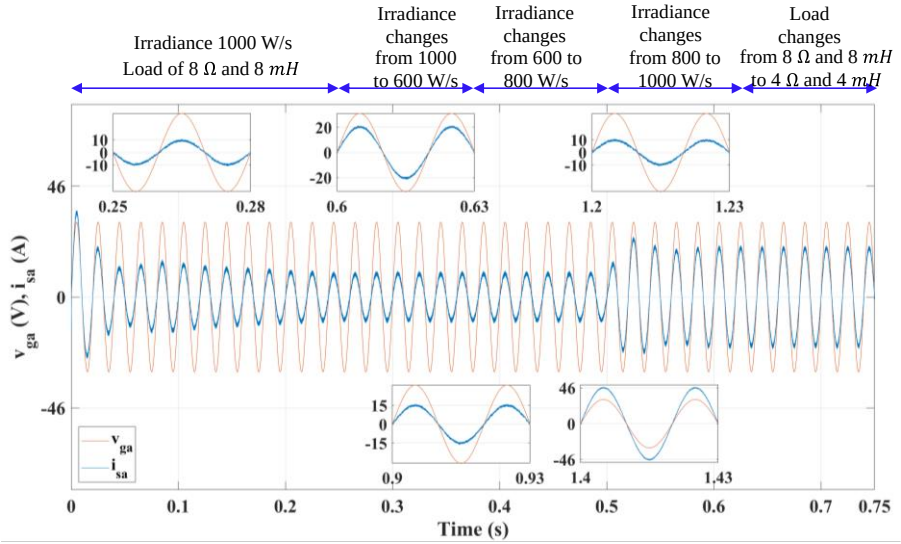


Figure II.30. First phase grid current with its corresponding voltage.

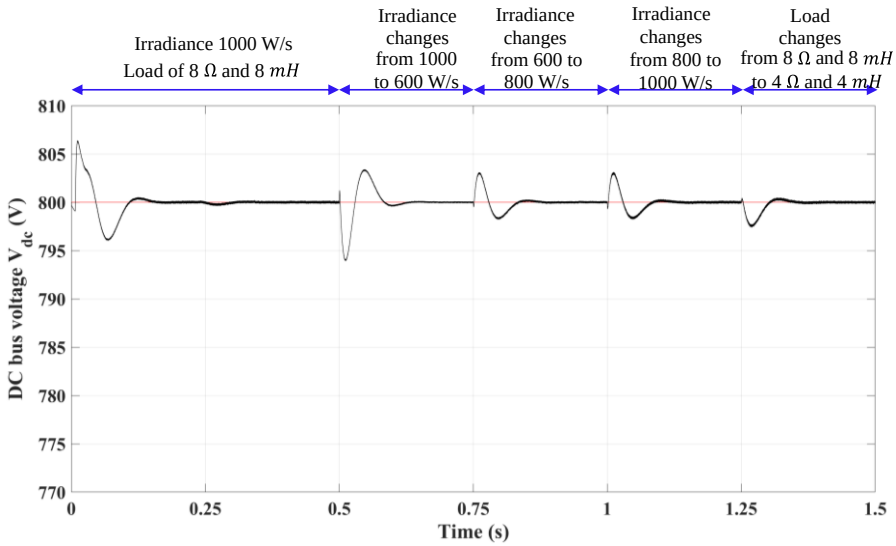


Figure II.31. DC bus voltage.

II.5. Conclusion

In this chapter, we explored the integration of a 4LI topology within a grid-connected photovoltaic (PV) conversion system. This configuration brings together the strengths of the conventional three-leg inverter with the added benefits of four-leg inverter.

We began by introducing and describing the main components of the overall PV grid-connected 4LI architecture, which operates as a four-leg active power filter. This system is capable of compensating current harmonics produced by single-phase nonlinearloads connected to a four-wire power grid. Additionally, we presented the mathematical models of the system in three different reference frames: the abc frame, the αβ0 frame, and the dq0frame.

The widely used instantaneous power theory (pq0 method) for identifying harmonic currents in four-leg active filtering applications was discussed. For tracking the reference currents, we adopted the 3D-SVM technique, which is commonly applied in such control strategies and forms the basis for the implementation of the parallel active filter control in our work.

Furthermore, we addressed the regulation of both the DC-link voltage and the 4LI currents in the synchronous frame using PI controllers. The design and tuning of these controllers were carried out through pole placement methods.

On the system level, the overall control strategy for the PV-4LI demonstrated excellent performance. It effectively facilitated MPPT for the PV generator, ensured stable power injection into the grid, maintained DC bus voltage regulation, and provided reactive power compensation alongside harmonic current suppression for nonlinear loads.

Despite the promising performance demonstrated by the single 4LI-based PV grid-connected system, several limitations emerge when scaling this topology to high-power applications. The main

constraints include the increased stress on individual switching devices, elevated current ratings required for each inverter leg, heightened switching losses and thermal management challenges, and the limited current handling capability of a single inverter structure. Moreover, in high-power scenarios, the failure of a single 4LI can compromise the entire system's operation, reducing overall reliability and availability. These limitations necessitate either oversized power semiconductor devices or voltage/current derating, both of which reduce cost-effectiveness and system efficiency. To overcome these challenges, the use of parallel-connected four-leg inverters presents a compelling solution. By distributing the total power demand across multiple 4LI units, each inverter operates at a reduced power level, thereby decreasing component stress, improving thermal distribution, and enhancing system redundancy and fault tolerance. Furthermore, parallel operation enables modular system design, facilitating easier maintenance and scalability. The next chapter will thoroughly investigate the modeling, control strategies, and performance evaluation of parallel four-leg inverter configurations for high-power PV grid-connected systems, with particular emphasis on current sharing techniques, synchronization methods, and enhanced reliability under various operating conditions.

Chapter 3

Modeling and linear control of PVG grid connected parallel four leg inverters system

III.1. Introduction

In applications requiring significant energy capacity, including distributed energy generation infrastructure, single 4LI encounter restrictions related to power switch current limitations. These constraints impede the achievement of critical performance metrics including reliability, power capacity, and modular functionality. Parallel configuration of 4LIs represents a viable solution that enables enhanced power capacity while addressing these inherent limitations. While multilevel 4LI architectures are optimized for voltage amplification, parallel inverter systems are specifically designed to increase current capacity, thereby circumventing the current restrictions of power switching components. The implementation of parallel 4LI topologies offers significant advantages over single four-leg configurations, including increased system capacity, reduced thermal stress on switching elements, mitigation of current rating constraints, and enhanced system stability, reliability, and modularity. Furthermore, parallel arrangement facilitates increased apparent switching frequency at output terminals, reduced harmonic distortion, minimized electromagnetic interference, and improved system efficiency and redundancy.

A significant challenge in parallel 4LI systems is the formation of zero-sequence circulating current (ZSCC) pathways resulting from disparities in zero-sequence voltages (ZSVs) between parallel units [161–170]. These discrepancies typically originate from mismatches in filter inductance parameters, unbalanced output current distribution, or non-uniform switching frequencies. ZSCC introduces substantial distortions in inverter output currents, particularly affecting third-harmonic components and their multiples, which leads to abnormal acoustic emissions and mechanical vibrations in filter inductances. Additional adverse effects include increased output voltage distortion, elevated power losses, compromised system efficiency and reliability, heightened electromagnetic interference, and increased current stress on power switching devices [162–168].

This research introduces a novel control method to address ZSCC issues in parallel 4LI systems. The proposed control strategy involves modification of 3DSVPWM techniques. This approach aims to eliminate ZSCC through ZSV differential reduction by adjusting zero-vector duty ratios in the 3DSVPWM algorithm during each switching cycle. The zero-vector duty ratios are parameterized using an adjustment variable obtained from ZSCC regulation through a dedicated PI controller. This modified 3DSVPWM methodology offers numerous advantages, including: adjustable zero-vector duty ratios for effective ZSCC suppression; maintained output current quality during unbalanced current sharing or filter parameter variations; suppression of ZSV differentials; high impedance to ZSCC; implementation simplicity; compatibility with multiple parallel four-leg PWM converter configurations; preservation of control objectives and output quality; and maximization of DC voltage utilization. Moreover, this approach potentially enhances system efficiency, reliability, and operational longevity through optimized switching device utilization, reduced power losses associated with ZSCC, and minimized stress on power switching components.

III.2. State of the art on ZSCC elimination techniques in parallel 4LIs

It is necessary that the current capacity of the DC-AC conversion stage must be increased in order to have the required power in certain applications such as mining, photovoltaic and wind production systems, etc. [79], [131], [166-170]. One of the most effective ways to achieve this objective is the parallel connection of 4LIs.

Unlike multilevel 4LI topologies, which allow for increased output voltages, the parallel connection of 4LIs enables higher output currents. Furthermore, it offers the same advantages as multilevel four leg structures in terms of reduced component ratings, improved waveform quality, and modularity, which ensures continuity of service and allows for rapid adaptation to specification modifications [163–170]. However, the most significant concern in parallel 4LI's configurations is the current circulation between the different parallel 4LIs, often referred to in the literature as Zero-Sequence Circulating Current (ZSCC). There are several factors causing ZSCC generation, such as unequal current sharing between parallel 4LIs, differences in output filter impedance values, switching mechanisms, or switch dead-time. These asymmetries lead to potential differences between the parallel legs (branches), and since parallel 4LIs share the same

AC and DC sides, this current easily finds a path to circulate between the different parallel 4LIs.

The ZSCC causes distortion and asymmetry in output currents, as well as a decrease in the overall system performance. Various control strategies have been proposed to address this problem. Although various dynamics associated with ZSCC in parallel traditional three leg inverters have been investigated, research specifically focused on circulation current suppression in parallel- arrangement of 4LIs remains limited. These parallel converter configurations, which share common DC and AC bus topologies, are employed primarily for their capacity to regulate zero-sequence currents and thereby minimize voltage fluctuations at the PCC. The average model of such a topology, along with the corresponding equivalent models for ZSCC, has been formulated and analyzed in [22], [171].

In [171], a modified sinusoidal PWM (SPWM) strategy operating in the dq0 reference frame was introduced to mitigate ZSCC in a parallel arrangement of two 4LIs connected to the grid, particularly under conditions of unbalanced filter inductances. This technique achieves ZSCC reduction by exclusively regulating the neutral current of the fourth leg of the secondary 4LI. However, despite its merits, this method incurs high switching losses and exhibits suboptimal DC voltage utilization. Additionally, it lacks direct ZSCC regulation, which compromises both suppression effectiveness and output current quality under scenarios involving filter parameter imbalances and unequal current sharing.

To address ZSCC and its associated low-frequency harmonic components (LFHCs), a sinusoidal PWM technique incorporating a third-harmonic injection feedforward control in the abc reference frame was proposed in [172]. This method successfully reduces current distortion and ZSCC-LFHCs under mismatched filter conditions. Nonetheless, it suffers from inherent limitations such as reduced DC bus voltage utilization and elevated switching losses. Moreover, the method presents difficulties in separately regulating the ZSC and ZSV in parallel 4LI systems that are an essential requirement in four-wire configurations due to the inseparability of these components in the abc reference frame [173].

An alternative approach, involving a modified three-level 3D-SVPWM, was introduced in [174] for parallel-connected three-level T-type 4LIs operating in the dq0 frame. This technique effectively suppresses ZSCC and output current harmonics while allowing for independent regulation of ZSC and ZSV in each 4LI. However, this strategy is not compatible with the parallel 4LI’s topology considered in this thesis.

In [175], an SPWM control strategy based on identical ZSV injection was developed for parallel two-level three-leg converters connected to the grid. A further advancement was presented in [176], where a modified SPWM approach utilizing a PI controller was employed in a parallel system of two 4LIs within a SAPSS. This method adjusts one SPWM modulation voltage using a regulated ZSV derived from ZSCC control. Although applicable to both parallel three-leg and 4LIs, these SPWM-based strategies result in significant peak-to-peak ZSCC values and high output current harmonics. Moreover, the reliance on SPWM within the abc reference frame inherently restricts direct control of individual ZSVs across parallel 4LIs. This discrepancy in

ZSV magnitudes leads to elevated ZSCC levels, ultimately compromising the performance, efficiency, and reliability of parallel 4LI systems.

In this regard, the present study introduces an enhanced ZSCC suppression strategy based on a modified 3D-SVPWM used for parallel-connected 4LIs-based PV grid connected system [177]. The core principle of the proposed technique involves mitigating ZSCC by minimizing the disparity between ZSVs. This is achieved through dynamic adjustment of the zero-vector duty ratios within each switching cycle, as defined by the modified 3D-SVPWM scheme. Specifically, the zero-vector duty ratios are modulated using a control variable generated via a proportional-integral (PI) controller, which actively regulates the ZSCC toward zero.

The proposed method offers several advantages, which it enables flexible tuning of zero-vector duty ratios for effective ZSCC mitigation, thereby preserving output current quality even under conditions of unbalanced current distribution or mismatched output filter parameters. Additionally, the approach facilitates straightforward and direct regulation of both ZSCs and ZSVs, suppresses ZSV discrepancies, and provides high impedance to the LFHCs associated with ZSCC. The method is also characterized by its implementation simplicity, compatibility with multi-parallel 4LI configurations, and its non-intrusive nature with respect to the primary control objectives and output performance of the system, while maintaining high DC voltage utilization.

Moreover, the proposed control strategy is anticipated to improve the overall efficiency, reliability, and service life of parallel 4LI systems. This is accomplished by optimizing the operation of power switches, minimizing losses attributed to both ZSCC and switching activity, and reducing thermal and electrical stress on the switching devices.

III.3. Topology and modeling of the parallel 4LIs-based PVG grid connected system

Parallel 4LIs play a crucial role in PV grid-connected systems by providing flexible and reliable power conversion, especially in systems with unbalanced or nonlinear loads. Each inverter operates with an additional fourth leg, which allows for independent control of the neutral current, ensuring stable and balanced power delivery to the grid even under unbalanced conditions. When connected in parallel, these 4LIs enhance system scalability, increase power capacity, and improve fault tolerance. Their configuration also supports better voltage regulation, efficient load sharing, and higher overall system reliability, making them highly beneficial for modern PV applications where stability and flexibility are key. A configuration of two parallel-connected 4LI's systems, is illustrated in Figure. III.1. Both 4LIs share a common DC bus and AC connection, and interface with a three-phase PCC through an LC output filter. The LC filter serves to suppress high-frequency switching components, thereby ensuring smooth output currents and voltages in the parallel system. For the sake of modeling simplicity, the duty ratio of the upper switch corresponding to phase leg k (k=a,b,c,n) in 4LI x (x=1,2) is denoted by d_{kx} [171].

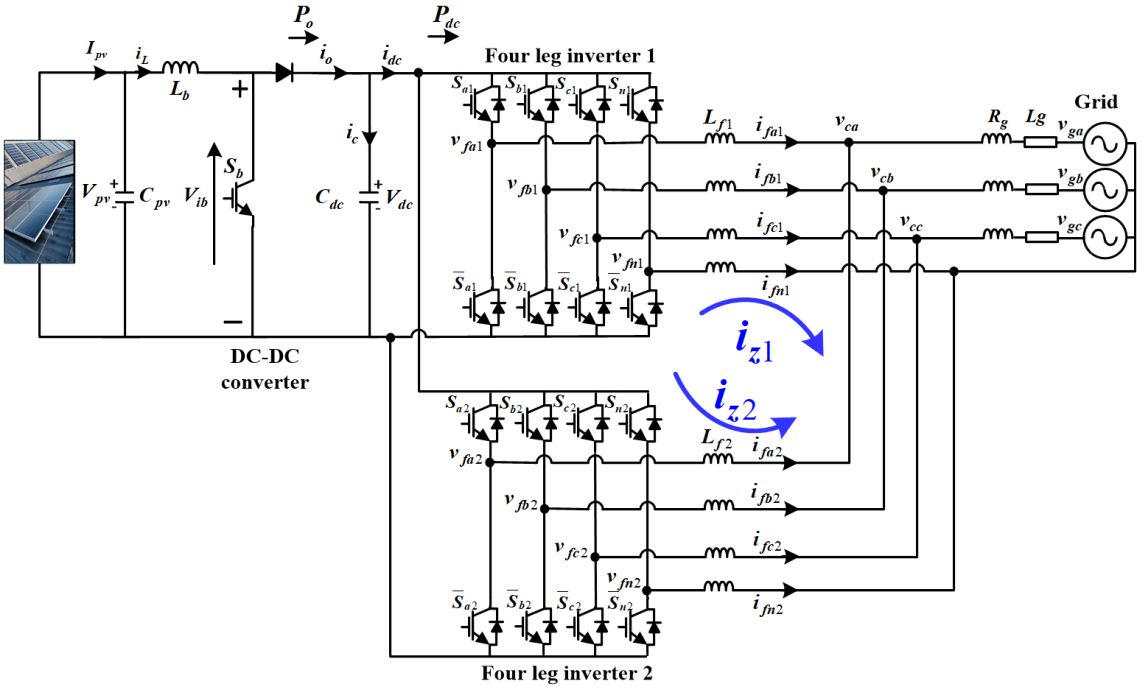


Figure. III.1. Topologies of the PV grid connected parallel 4LI's system.

III.3.1. Parallel system output current dynamics

According to the topologies of the parallel 4LI in Figure. III.1, the three phase output voltages of each 4LI, expressed in the abc reference frame, can be defined as a function of the DC-bus voltage and the corresponding average duty ratios as follows [171]:

$$\begin{bmatrix} v_{fax} \\ v_{fbx} \\ v_{fcx} \\ v_{fnx} \end{bmatrix} = V_{dc} \begin{bmatrix} d_{ax} \\ d_{bx} \\ d_{cx} \\ d_{nx} \end{bmatrix} \quad \text{(III.1)}$$

The equivalent circuit model of the parallel connected 4LIs in Figure. III.1 is depicted in Figure. III.2

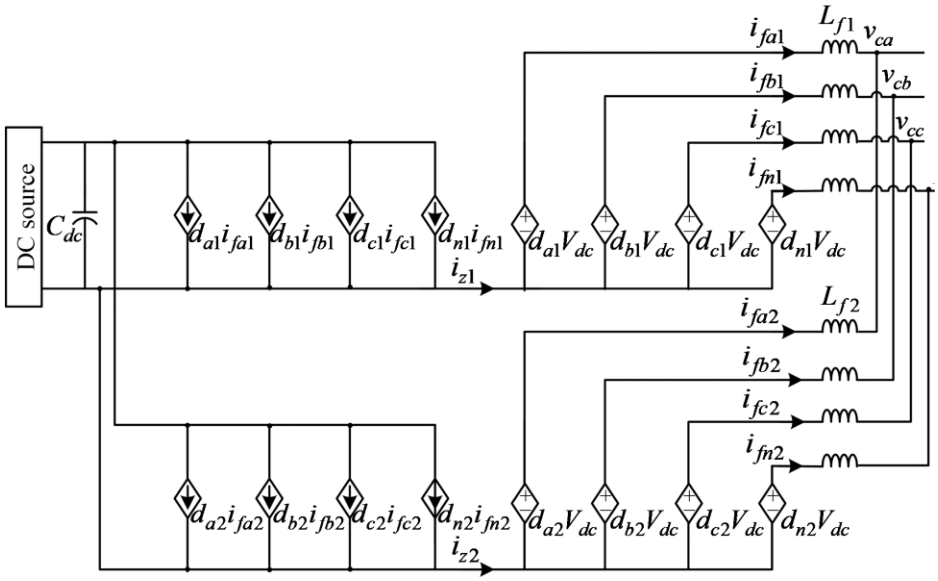


Figure. III.2. Equivalent circuit of two parallel 4LIs in abc frame.

According to the Figure. III.2, the output current dynamics of the parallel system in the abc frame are given as a function of the duty ratio be the following equations:

$$\begin{cases} L_{f1}\frac{di_{fa1}}{dt} = d_{a1}V_{dc} - v_{ca} + L_{f1}\frac{di_{fn1}}{dt} \\ L_{f1}\frac{di_{fb1}}{dt} = d_{b1}V_{dc} - v_{cb} + L_{f1}\frac{di_{fn1}}{dt} \\ L_{f1}\frac{di_{fc1}}{dt} = d_{c1}V_{dc} - v_{cc} + L_{f1}\frac{di_{fn1}}{dt} \end{cases} \quad \text{(III.2)}$$

$$\begin{cases} L_{f2}\frac{di_{fa2}}{dt} = d_{a2}V_{dc} - v_{ca} + L_{f2}\frac{di_{fn2}}{dt} \\ L_{f2}\frac{di_{fb2}}{dt} = d_{b2}V_{dc} - v_{cb} + L_{f2}\frac{di_{fn2}}{dt} \\ L_{f2}\frac{di_{fc2}}{dt} = d_{c2}V_{dc} - v_{cc} + L_{f2}\frac{di_{fn2}}{dt} \end{cases} \quad \text{(III.3)}$$

The DC input current of each 4LI is given by:

$$i_{dcx} = d_{ax}i_{fax} + d_{bx}i_{fbx} + d_{cx}i_{fcx} + d_{nx}i_{fnx} \quad \text{(III.4)}$$

where $V_{fx}=[v_{fax}v_{fbx}v_{fcx}v_{fnx}]^T$ and $I_{fx}=[i_{fax}i_{fbx}i_{fcx}i_{fnx}]^T$ represent the output voltage and current vectors of 4LI *x*, respectively.

Equations (III.2) and (III.3) illustrate that the dynamic behavior of the output current in the two parallel-connected 4LI system, when expressed in the abc reference frame, is characterized by considerable complexity, which poses significant challenges for both system analysis and control design. To address this, a simplified, low-order average models of the parallel system output currents are derived in the dq0 frame by applying Park's transformation to Equations (III.2) and (III.3), resulting in the dynamic currents of both 4LIs in the dq0 frame as presented in Equations (III.5) and (III.6).

$$\begin{cases} \frac{di_{fd1}}{dt} = \frac{d_{d1}V_{dc}}{L_{f1}} - \frac{v_{cd}}{L_{f1}} + \omega i_{fq1} \\ \frac{di_{fq1}}{dt} = \frac{d_{q1}V_{dc}}{L_{f1}} - \frac{v_{cq}}{L_{f1}} - \omega i_{fd1} \\ \frac{di_{f01}}{dt} = \frac{d_{01}V_{dc}}{4L_{f1}} \end{cases} \quad \text{(III.5)}$$

$$\begin{cases} \frac{di_{fd2}}{dt} = \frac{d_{d2}V_{dc}}{L_{f2}} - \frac{v_{cd}}{L_{f2}} + \omega i_{fq2} \\ \frac{di_{fq2}}{dt} = \frac{d_{q2}V_{dc}}{L_{f2}} - \frac{v_{cq}}{L_{f2}} - \omega i_{fd2} \\ \frac{di_{f02}}{dt} = \frac{d_{02}V_{dc}}{4L_{f2}} \end{cases} \quad \text{(III.6)}$$

The output voltages of each 4LI in the dq0 reference frame are expressed by:

$$\begin{bmatrix} v_{fdx} \\ v_{fqx} \\ v_{f0x} \end{bmatrix} = V_{dc} \begin{bmatrix} d_{dx} \\ d_{qx} \\ d_{0x} \end{bmatrix} \quad \text{(III.7)}$$

As previously discussed, in parallel 4LI's systems, ZSCC not only arise from factors such as mismatched filter parameters or unequal output current sharing, but typically induce ZSCs, which also manifest specifically in the fourth leg of each inverter, where they must be effectively suppressed. Based on the average equivalent circuit model of the two parallel 4LIs, represented in the dq0 reference frame and illustrated in Figure. III.3, the dq-axes are interconnected through two voltage-controlled currentsources and four current-controlled voltagesources. In contrast, the 0-axis remains decoupled from the dq-axes, implying that the zero-sequence component is confined solely to the 0-axis and remains independent of the d- axis and q-axis dynamics. As a result, the ZSC canbe controlled separately by controlling the neutral current associated with the fourth leg of each inverter. This characteristic directly supports the development of the proposed circulating current suppression method and simplifies its implementation.

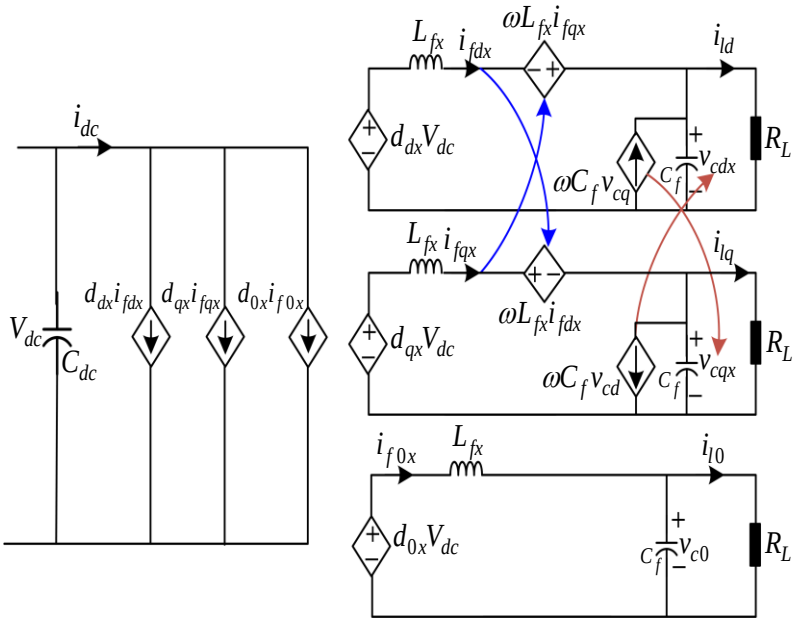


Figure. III.3. Average equivalent circuit model of the two parallel 4LIs in the dq0 frame.

III.3.2. Parallel system DC bus voltage dynamic

Based on the parallel system configuration illustrated in Figure. III.1, the dynamic behavior of the DC bus voltage can be described as a function of the current variation within the DC bus, as expressed by the following equation:

$$\frac{dV_{dc}}{dt} = \frac{1}{C_{dc}} i_c = \frac{1}{C_{dc}} (i_D - i_{dc}) \tag{III.8}$$

where i_C is the current in the parallel system input DC capacitor, i_D is the output current of the DC-DC boost converter, and i_{dc} the parallel system input current.

III.3.3. ZSCC characteristics and modeling

When multiple 4LIs are parallel connected via shared DC and AC buses as shown in Figure III.1, discrepancies in ZSVs between the parallel 4LIs arise, particularly under mismatched filter inductance or unbalanced output currents, which result in the circulation of ZSCCs through their respective phase legs. These ZSCCs are inherently complex to model, analyze, and regulate. To address these challenges, the phase-leg averaging technique proposed in [171] is employed. Using this method, the average phase-leg models for the two parallel 4LIs are developed and depicted in Figure. III.2. On the basis of this model, the expressions for the ZSCCs circulating between the parallel 4LI modules can be derived. As shown in the figure, the ZSCCs flowing between the two 4LIs exhibit identical magnitudes but are 180 degrees out of phase, as mathematically described in Equations (III.9) and (III.10).

$$\begin{cases} i_{z1} = i_{fa1} + i_{fb1} + i_{fc1} + i_{fn1} \\ i_{z2} = i_{fa2} + i_{fb2} + i_{fc2} + i_{fn2} \end{cases} \tag{III.9}$$

$$i_z = i_{z1} = -i_{z2} \tag{III.10}$$

According to Figure. III.2, we have:

$$\begin{cases} d_{a1}V_{dc} - L_{f1}\frac{di_{fa1}}{dt} = d_{b1}V_{dc} - L_{f1}\frac{di_{fb1}}{dt} \\ \qquad\qquad\qquad = d_{c1}V_{dc} - L_{f1}\frac{di_{fc1}}{dt} \\ \qquad\qquad\qquad = d_{n1}V_{dc} - L_{f1}\frac{di_{fn1}}{dt} \end{cases} \quad \text{(III.11)}$$

$$\begin{cases} d_{a2}V_{dc} - L_{f2}\frac{di_{fa2}}{dt} = d_{b2}V_{dc} - L_{f2}\frac{di_{fb2}}{dt} \\ \qquad\qquad\qquad = d_{c2}V_{dc} - L_{f2}\frac{di_{fc2}}{dt} \\ \qquad\qquad\qquad = d_{n2}V_{dc} - L_{f2}\frac{di_{fn2}}{dt} \end{cases} \quad \text{(III.12)}$$

By summing the two equalities (III.11) and (III.12), we obtained:

$$\sum_{k=a,b,c,n} d_{k1}V_{dc} - L_{f1}\sum_{k=a,b,c,n}\frac{di_{fk1}}{dt} = \sum_{k=a,b,c,n} d_{k2}V_{dc} - L_{f2}\sum_{k=a,b,c,n}\frac{di_{fk2}}{dt} \quad \text{(III.13)}$$

The zero-sequence..duty..ratio (ZSDR) for a 4LI is.defined as the.sum.of.the.duty.ratios of all its.phase legs. For the case of two parallel-connected 4LIs, this relationship is formulated and expressed in Equation (III.14) as follows:

$$\begin{cases} d_{z1} = \sum_{k=a,b,c,n} d_{k1} = d_{a1} + d_{b1} + d_{c1} + d_{n1} \\ d_{z2} = \sum_{k=a,b,c,n} d_{k2} = d_{a2} + d_{b2} + d_{c2} + d_{n2} \end{cases} \quad \text{(III.14)}$$

By substituting Equations (III.9) and (III.14) into Equation (III.13), we obtained:

$$d_{z1}V_{dc} - L_{f1}\frac{di_{z1}}{dt} = d_{z2}V_{dc} - L_{f2}\frac{di_{z2}}{dt} \quad \text{(III.15)}$$

where $d_{z1}V_{dc} = v_{zsv1}$ and $d_{z2}V_{dc} = v_{zsv2}$ are the ZSVs of 4LIs 1 and 2, respectively, which are given by:

$$\begin{cases} v_{zsv1} = (d_{a1} + d_{b1} + d_{c1} + d_{n1})V_{dc} \\ v_{zsv2} = (d_{a2} + d_{b2} + d_{c2} + d_{n2})V_{dc} \end{cases} \quad \text{(III.16)}$$

From Equation (III.10) and Equation (III.14), the ZSCC model can be expressed by:

$$(L_{f1} + L_{f2})\frac{di_z}{dt} = (d_{z2} - d_{z1})V_{dc} \quad \text{(III.17)}$$

Using Equation (III.16) and Equation (III.17), the ZSCC can be expressed by:

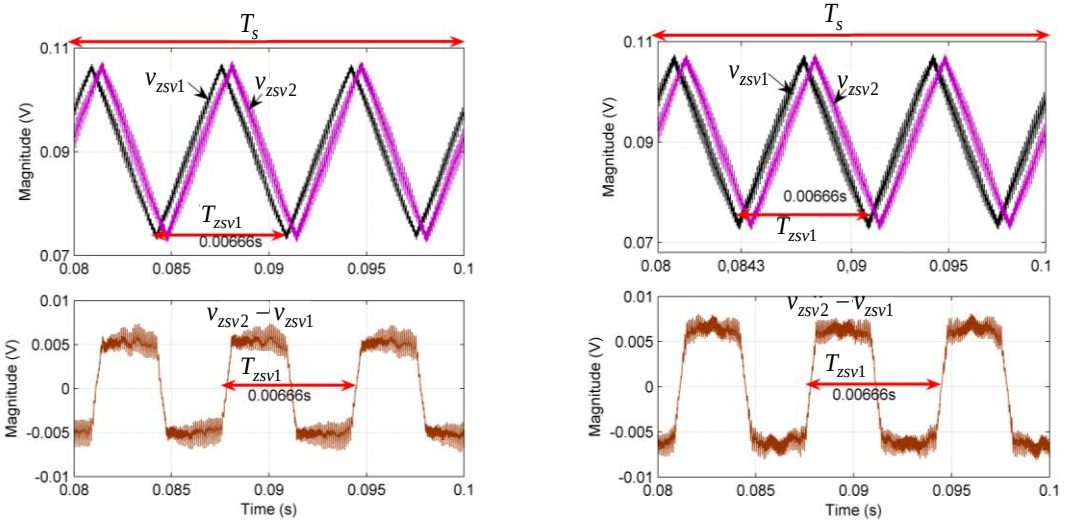
$$(L_{f1} + L_{f2})\frac{di_z}{dt} = v_{zsv2} - v_{zsv1} \quad \text{(III.18)}$$

The ZSCC in Equation (III.18) can be expressed in Laplace domain as follows:

$$I_z(s) = \frac{\Delta v_{zsv}(s)}{(L_{f1}+L_{f2})} \quad \text{(III.19)}$$

Equation (III.19) illustrates that the primary factor responsible for the generation of ZSCC is the difference in ZSV between the two parallel 4LIs, denoted as Δv_{zsv}. This discrepancy may arise from various factors, including mismatched parallel system output filter inductances, uneven

distribution of output currents, or inconsistencies among switching devices. When the ZSDRs, d_{z1} and d_{z2}, corresponding to the ZSVs of the parallel 4LIs (v_{zsv1} and v_{zsv2}), are identical, the occurrence of ZSCC is theoretically eliminated. Figures III.4a and III.4b present the ZSV waveforms of the two parallel 4LIs and their difference, Δv_{zsv}, under conditions of both inductance imbalance and unequal current sharing, with a modulation index of 1 and a load voltage frequency of 50 Hz. The ZSVs exhibit a triangular waveform characterized by a frequency three times that of the grid voltage (150 Hz) and consistent amplitude, though a phase shift is observed in both scenarios. The corresponding Δv_{zsv} waveform forms a square wave with the same tripled frequency. As established in references [178, 179], the ZSCC induced by Δv_{zsv} ideally follows a triangular waveform with a frequency three times that of the load voltage frequency. Consequently, ZSCC can be effectively mitigated by precisely controlling Δv_{zsv} to maintain a zero value.



(a) (b)

Figure III.4. ZSVs and their corresponding differences for parallel 4LIs operating with a modulation index of m=1.0 and a grid voltage frequency of f=50 Hz; (a) scenario with mismatched filter inductances, and (b) scenario with unequal output current sharing.

By applying Fourier series analysis, as described in [180], to the data presented in Figures III.4a and III.4b, the ZSV of each 4LI (v_{zsvx}) in the parallel system can be mathematically approximated as follows:

$$v_{zsvx}(t) = d_{zx}V_{dc} \approx \frac{8V_z}{\pi^2}\sum_{h=1,3,5,..}^{\infty}\frac{(-1)^{(h-1)/2}}{h^2}sin(h\omega_3 t) \quad \text{(III.20)}$$

where $V_z = V_{z1} = V_{z2}$ is the amplitude of the ZSV of each 4LI and $\omega_3 = 3\omega$ is the frequency of the ZSVs.

Considering this value, when v_{zsv2} experiences a phase shift of λ relative to v_{zsv1}, the expressions for the two zero-sequence voltages can be represented as:

$$\begin{cases} v_{zsv1}(t) \approx \frac{8V_z}{\pi^2}\sum_{h=1,3,5,..}^{\infty}\frac{(-1)^{\frac{(h-1)}{2}}}{h^2}sin(h\omega_3 t) \\ v_{zsv2}(t) \approx \frac{8V_z}{\pi^2}\sum_{h=1,3,5,..}^{\infty}\frac{(-1)^{(h-1)/2}}{h^2}sin(h\omega_3 t-\lambda) \end{cases} \quad \text{(III.21)}$$

According to Equation (III.21), the difference between the two ZSVs can be written as:

$$\Delta v_{zsv} \approx \frac{\boldsymbol{8V_z}}{\boldsymbol{\pi^2}}\sum_{h=1,3,..}^{\infty}\frac{-1^{\frac{(h-1)}{2}}}{h^2}(sin(h\omega_3 t-\lambda)-sin(h\omega_3 t)) \quad \text{(III.22)}$$

Equation (III.21) can be expressed in the following alternative form:

$$\Delta v_{zsv} \approx -\frac{\boldsymbol{16V_z}}{\boldsymbol{\pi^2}}sin\left(\frac{\lambda}{2}\right)\sum_{h=1,3,..}^{\infty}\frac{(-1)^{\frac{(h-1)}{2}}}{h^2}cos\left(h\omega_3 t-\frac{\lambda}{2}\right) \quad \text{(III.23)}$$

According to Equation (III.19), the ZSCC can be calculated by dividing Δv_{zsv} in Equation (III.23) by the corresponding impedance at each harmonic component frequency, as shown below:

$$i_z(t) \approx \frac{-16\boldsymbol{V_z}sin\left(\frac{\lambda}{2}\right)}{(L_{f1}+L_{f2})\boldsymbol{\pi^2}\omega_3}\sum_{h=1,3,..}^{\infty}\frac{(-1)^{\frac{(h-1)}{2}}}{h^2}cos\left(h\omega_3 t-\frac{\lambda}{2}\right) \quad \text{(III.24)}$$

As demonstrated in Equation (III.24), the ZACC consists of multiple additional harmonics, with the fundamental frequency being 150 Hz. These harmonics can be expressed as follows:

$$i_z(t) \approx i_z^{1st}(t) + i_z^{3rd}(t) + i_z^{5rd}(t) + i_z^{7rd}(t) \quad \text{(III.25)}$$

where:

$i_z^{1st}(t) = B\cos(\omega_3 t-\lambda)$, $i_z^{3rd}(t) = B\cos(3\omega_3 t-\lambda)$, $i_z^{5rd}(t) = B\cos(5\omega_3 t-\lambda)$,……and $B = \frac{-2A\sin\left(\frac{\lambda}{2}\right)}{(L_{f1}+L_{f2})\omega_3}$

As outlined in the introduction of this chapter, two methods for eliminating circulating current are proposed: the adjustment of modulation voltages in the carrier-based sinusoidal pulse-width modulation (SPWM) scheme, and the modification of duty ratio of zero-vectors within the 3DSVPWM approach. The detailed principles and implementation of both ZSCC control and elimination strategies are presented in the following subsections.

III.4 ZSCC control and elimination in parallel 4LIs-based PV grid connected system

III.4.1. Adjusted SPWM modulation voltages approach

In this subsection, a simpler approach using modified SPWM with ZSCC PI regulator was used for parallel 4LIs-based PV grid connected system to eliminate ZSCC generated under unbalanced output filter inductances and output current sharing conditions, which adjusted SPWM reference modulation voltages through voltage term derived from ZSCC PI regulator [176].

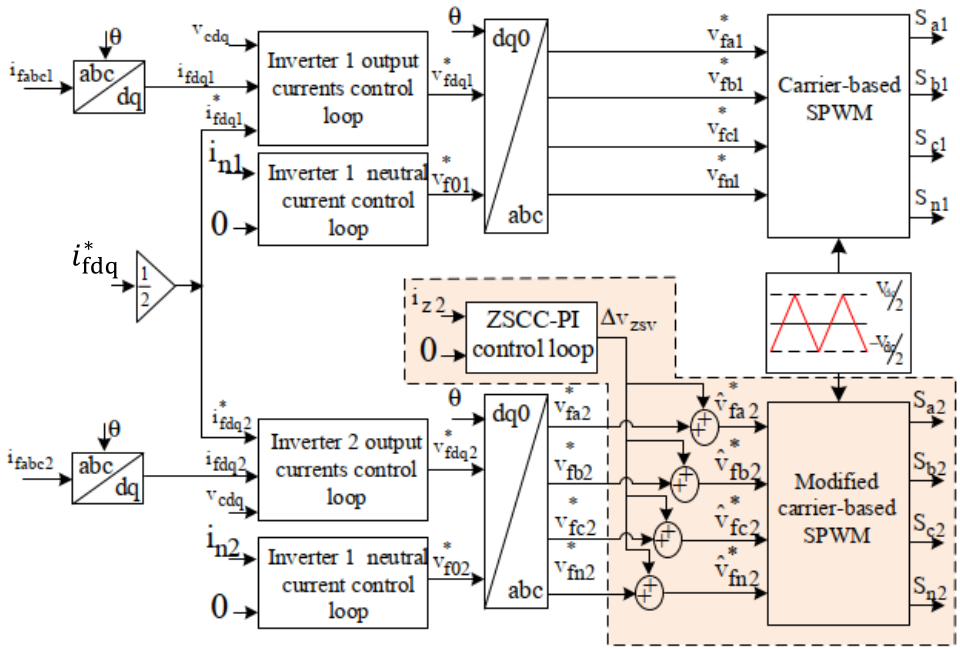


Figure. III.5. Control of the parallel 4LIs using the adjusted PWM reference modulation voltages-based SPWM

$$v_{z2} = (v_{a2}^* + v_{b2}^* + v_{c2}^* + v_{n2}^*)/4 \quad \text{(III.26)}$$

In our work, we adjust the PWM reference modulation voltages of the second 4LI, as shown in Figure. III.5. Accordingly, the new zero-sequence modulation voltages v'_{z2} of the second 4LI after compensating the voltage term v to adjusted the reference modulation voltages can be calculated using the new modulation voltages ($v_{a2}^{*\prime}, v_{b2}^{*\prime}, v_{c2}^{*\prime}, v_{n2}^{*\prime}$) as follows:

$$\begin{aligned} v'_{z2} &= (v_{a2}^{*\prime} + v_{b2}^{*\prime} + v_{c2}^{*\prime} + v_{n2}^{*\prime})/4 \\ &= \big((v_{a2}^* + v) + (v_{b2}^* + v) + (v_{c2}^* + v) + (v_{n2}^* + v)\big)/4 \end{aligned} \quad \text{(III.27)}$$

Substituting (III.26) into (III.27), the new zero-sequence modulation voltages v'_{z2} of the adjusted reference modulation voltages approach is compensated by the ZSCC control loop using the compensating voltage term v as follows:

$$v'_{z2} = v_{z2} + v \quad \text{(III.28)}$$

From Equation (III.28), the difference between the ZSVs of the two parallel 4Lis Δv_z after compensating the modulation voltages of the adjusted SPWM approach is expressed by:

$$\Delta v_{zs} = v'_{zs2} - v_{zs1} = \frac{(v_{a2}^* - v_{a1}^* + v) + (v_{b2}^* - v_{b1}^* + v) + (v_{c2}^* - v_{c1}^* + v) + (v_{n2}^* - v_{n1}^* + v)}{4} \quad \text{(III.28)}$$

By substituting Equation (III.28) into Equation (III.19), we obtain the modified Laplace model of the ZSCC as:

$$I_z(s) = \frac{\Delta v_z + v}{(L_1 + L_2)s} \quad \text{(III.29)}$$

Equation (III.29) demonstrates that the ZSCC magnitude is primarily determined by the compensating voltage term v. To achieve effective ZSCC elimination, this compensating voltage term must be precisely determined to counteract modulation voltage differences between parallel 4LIs caused by mismatches in output inductances or the sharing of output currents. However, determining the appropriate compensating voltage requires dynamic adaptation to various operating conditions. Therefore, this work suggests a ZSCC feedback control method to generate the compensating voltage term v that automatically adapts to system parameter variations and operating conditions.

III.4.1.1. ZSCC regulation-based adjusted SPWM modulation voltages approach

Upon compensating for the reference modulation voltages of the second 4LI, the updated ZSCC model described in Equation (III.19) exhibits first-order system behavior, which facilitates the design of closed-loop control strategies. Various linear controllers for ZSCC regulation, including PI controllers [176], [180], PI with feedforward loops [181], PI-deadbeat controllers [182], and PI-quasi-resonant controllers (PIQRC) [183, 184], have been developed recently. In our work, PI controller is employed to block the propagation of ZSCC, as shown in Figure III.6. The purpose of PI-based ZSCC is to mitigate the difference between the ZSVs by acting upon the compensating voltage term v that automatically adapts to variations in system parameters and operating conditions as follows:

$$v = (i_z^* - i_z)\left(\left(k_{piz} + \frac{k_{iz}}{s}\right)\right) \tag{III.30}$$

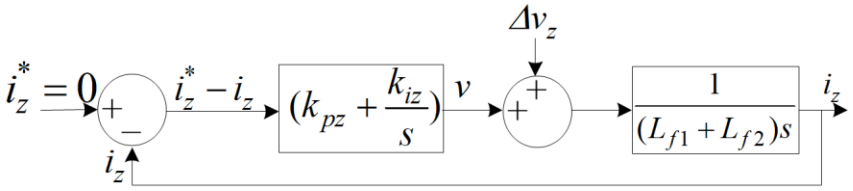


Figure. III.6. Block diagram of the PI-based ZSCC regulation

where k_{pz} and k_{iz} are the proportional and integral the gains of the PI for the ZSCC within the adjusted modulation voltages-based SPWM approach, which are expressed by [176]:

$$\begin{cases} k_{pz} = (L_{f1} + L_{f2})\xi_z\omega_{cz} \\ k_{iz} = (L_{f1} + L_{f2})\omega_{cz}^2 \end{cases} \tag{III.31}$$

ω_{cz} and $\xi_z$are, respectively, the cut off frequency and the damping factor of the PI regulator for the ZSCC within the within the adjusted modulation voltages-based SPWM approach.

III.4.2. Adjusted 3DSVPWM's zero-vector duty ratios approach

As mentioned in the state-of-the-art review of this chapter, several contributions have been proposed in the literature to address the problem of ZSCC between parallel inverters [163–170]. However, there are only a few articles that deal with the same issue in parallel 4LIs [171–177]. In this section, we propose a new method for eliminating ZSCC specifically dedicated to the eliminating the difference between the ZSVs of the two parallel 4LIs Δv_z by introducing a

variable allowing the adjustment of the duty ratio of zero-vectors (ZVs) within the 3DSVPWM technique that can influence the difference in ZSDRs $\Delta d_z = d_{z2} - d_{z1}$.

As highlighted in the first chapter of this thesis, the conventional 3DSVPWM technique is extensively employed for the PWM single generations of three-phase 4LIs, owing to its notable advantages such as maintaining a constant switching frequency, minimizing AC-side current harmonics, and reducing DC-bus voltage fluctuations. Moreover, this method is capable of generating symmetrical output voltages from 4LIs even under unbalanced load conditions [131], [160]. The 3DSVPWM strategy utilizes a total of sixteen state vectors (v_1, v_2…., v_{16}), comprising fourteen active vectors (AVs) and two ZVs, which are spatially distributed within a three-dimensional space vector diagram based on the αβ0 reference frame, as illustrated in Figure. III.7a. In this method, the state vectors are further projected onto five discrete voltage levels in a two-dimensional space, while the complete 3-D diagram is segmented into six prisms. Each of these prisms is subdivided into four tetrahedrons, each formed by a combination of three AVs and two ZVs, as depicted in Figures. III.7b and III.7c, where the first tetrahedron of the first prism is presented as an illustrative example.

Within each tetrahedron, the duty ratios corresponding to the three active vectors of 4LI *x* are denoted as d_{1x}, d_{2x}, and d_{3x}, while the combined duty ratio of the zero vectors is represented by d_{0x}. Based on these definitions, the reference voltage vector within the first tetrahedron of the first prism can be synthesized during each switching period T_s as expressed in Equation (III.25):

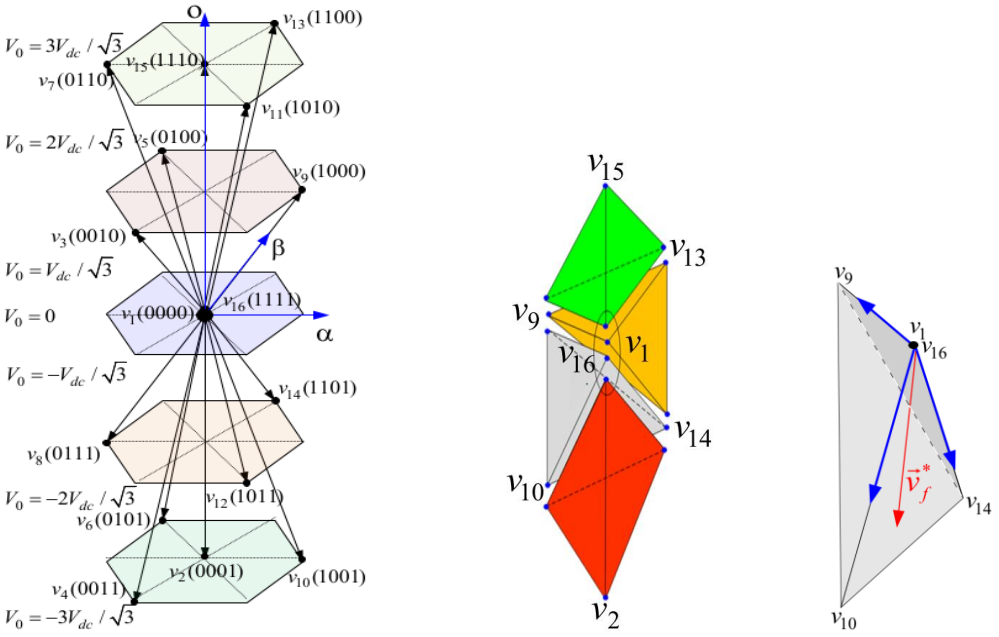


Figure. III.7. Four-leg inverter voltage vector's distributions; a) 3-D space vector diagram (αβ0), b) tetrahedrons within prism 1, and c) tetrahedron1within prism1 and their voltage vectors.

$$v_{fx}^* = \frac{d_{1x}v_9 + d_{2x}v_{10} + d_{3x}v_{14} + d_{0x}(v_0 + v_{16})}{T_s} \quad \text{(III.32)}$$

The sum of duty ratios of all vectors in each tetrahedron is given by:

$$d_{1x} + d_{2x} + d_{3x} + d_{0x} = 1 \quad \text{(III.33)}$$

According to Equation (33), we obtain the duty ratio of zero vectors d_{0x} as follows:

$$d_{0x} = 1 - d_{1x} - d_{2x} - d_{3x} \quad \text{(III.34)}$$

As illustrated in Figure III.7c, where the reference voltage vector for each 3DSVPWM-based parallel system, as defined in Equation (III.32), is assumed to lie within the first tetrahedron of the first prism, the corresponding state vectors and their associated duty ratios are organized according to a nine-segment switching sequence, as depicted in Figure III.8. In this sequence, the zero vectors are symmetrically placed at the beginning, middle, and end of each switching period with equal duty ratios d_0. While the active vectors are arranged in a manner that minimizes switching transitions within the switching period, thereby reducing switching losses.

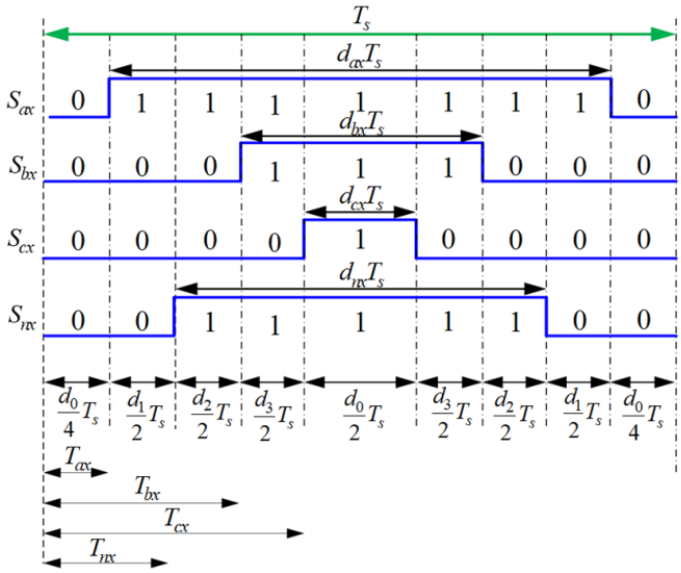


Figure. III.8. Distribution of the active and zero vectors along with their corresponding duty ratios within each switching interval in the traditional 3DSVPWM method.

According to Equation (III.14) and as illustrated in Figure. III.8, the ZSDR d_{zx} of each four leg converter within the parallel system is related to the duty ratios of the active and zero vectors in each switching period by:

$$\begin{aligned} d_{zx} &= d_{ax} + d_{bx} + d_{cx} + d_{nx} \\ &= d_{1x} + 2d_{2x} + 3d_{3x} + 2d_{0x} \end{aligned} \quad \text{(III.35)}$$

Substituting Equation (III.34) into Equation (III.35), we have:

$$d_{zx} = -d_{1x} + 2d_{3x} \quad \text{(III.36)}$$

The switching transition times T_{ax}, T_{bx}, T_{cx}, and T_{nx} corresponding to the state vectors in each 4LI within the parallel system can be defined as follows:

$$\begin{cases} T_{ax} = \frac{d_{0x}}{4} T_s \\ T_{bx} = T_{ax} + \frac{d_{1x}}{2} T_s + \frac{d_{2x}}{2} T_s \\ T_{cx} = T_{bx} + \frac{d_{3x}}{2} T_s \\ T_{nx} = T_{ax} + \frac{d_{1x}}{2} T_s \end{cases} \quad \text{(III.37)}$$

Since the traditional 3DSVPWM technique does not account for the modulation of ZSVs, ZSCCs are inevitably generated between parallel 4LIs. To address this issue, the proposed adjusted 3DSVPWM zero-vector duty ratios method approach in this subsection effectively eliminates the influence of ZSVs and suppresses the resulting ZSCC.

Drawing upon the preceding of ZSCC analysis and with the aim of eliminating the differential ZSVs between parallel 4LIs (Δv_{zsv}), this work proposes an innovative modification to the 3DSVPWM approach. The proposed approach introduces a dynamic adjustment parameter y_x that modifies ZSDRs based on ZSCC regulation outcomes within each switching interval, specifically targeting the duty ratios of zero vectors.

The distribution architecture of the active and zero vectors along with their corresponding duty ratios within each switching interval of the adjusted 3DSVPWM approach is illustrated in Figure. III.9, using the first tetrahedron of the first prism as a representative example. As demonstrated, the adjustment variable y_x modulates the ZSDRs of zero vectors during each switching cycle to neutralize the ZSDR differential Δd_z between d_{z1} and d_{z2}. This modulation transforms the duty ratios d_{0x} of the two zero vectors v_1 and v_{16} to modified values $d_{0x}/2 - 2y_x$ and $(d_{0x}/2 + 2y_x)$, establishing a controlled relationship between them. These strategic modifications to zero vector duty ratios maintain system control objectives and preserve output quality parameters including current characteristics, voltage profiles, and DC-bus voltage utilization efficiency. The differential parameter Δd_z can be effectively regulated through controlled manipulation of zero vectors. From a theoretical perspective, ZSCC elimination can be achieved by establishing Δd_z at zero, which constitutes the fundamental objective of the proposed adjusted 3DSVPWM approach.

Analysis of Figure III.9 confirms that the developed adjusted 3DSVPWM approach demonstrates satisfactory performance when operating within specified conditional parameters.

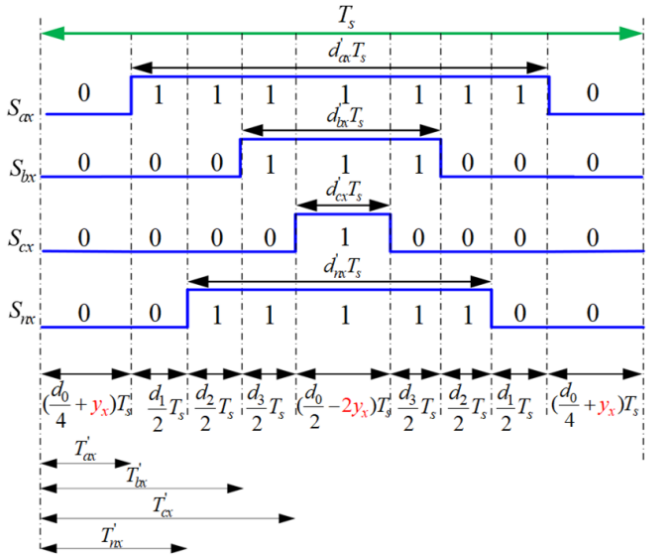


Figure. III.9. Distribution of the active and zero vectors along with their corresponding duty ratios in the proposed adjusted 3DSVPWM.

As illustrated in Figure. III.9, following the adjustment of the variable y_x, the updated ZSDRs d'_{zx} for the proposed adjusted 3D-SVPWM approach can be determined using the recalculated duty ratios ($d'_{ax}, d'_{bx}, d'_{cx}$, and d'_{nx}) according to the following expression:

$$\begin{aligned} d'_{zx} &= d'_{ax} + d'_{bx} + d'_{cx} + d'_{nx} \\ &= d_{1x} + 2d_{2x} + 3d_{3x} + 2d_{0x} - 8y_x \end{aligned} \quad \text{(III.38)}$$

By substituting Equation (III.34) into Equation (III.38), the ZSDR d'_{z2} in the proposed adjusted 3D-SVPWM approach is regulated based on the output variable y_2 of the ZSCC control loop, as expressed below:

$$d'_{zx} = (-d_{1x} + d_{3x} + 2 - 8y_x) \quad \text{(III.39)}$$

In the case of a two parallel-connected 4LI's system, the circulating currents generated by the two parallel 4LIs exhibit equal amplitudes but opposite directions. Consequently, by regulating the circulating current of one 4LI, the circulating current in the other 4LI is inherently controlled, ensuring that managing the circulating current in a single 4LI is sufficient to eliminate the circulating current throughout the entire system. Accordingly, ZSCC control is achieved by adjusting the 3D-SVPWM approach of the second 4LI through the y_2, while y_1 is fixed zero, with the first 4LI operating using C3DSVPWM approach.

Based on Equation (III.39), the difference in the ZSDRs among the two 4LIs, denoted as Δd_{zx} , for the proposed adjusted 3D-SVPWM approach can be formulated as follows:

$$\begin{aligned} d'_{zx} &= d'_{z2} - d'_{z1} \\ &= d_{11} - d_{12} + d_{32} - d_{31} - 8y_x \end{aligned} \quad \text{(III.40)}$$

Similarly, when the reference voltage vector lies within other tetrahedrons or prisms, Δd_{zx} can be computed using the same procedure.

According to Equations (III.19) and (III.40), the updated model of the ZSCC can be expressed by:

$$I_z(s) = \frac{d_{11}-d_{12}+d_{32}-d_{31}-8y_x}{(L_{f1}+L_{f2})} V_{dc} \quad \text{(III.41)}$$

Supposing that $\Delta_{12} = d_{11} - d_{12} + d_{32} - d_{31}$, Equation (III.41) becomes:

$$I_z(s) = \frac{\Delta_{12}-8y_x}{(L_{f1}+L_{f2})} V_{dc} \quad \text{(III.42)}$$

As illustrated in Figure III.9 and based on Equation (III.37), the revised switching transition times for the proposed adjusted 3D-SVPWM approach can be formulated as:

$$\begin{cases} T'_{a2} = \frac{d_{02}}{4} T_s + y_2 \\ T'_{b2} = T'_{a2} + \frac{d_{12}}{2} T_s + \frac{d_{22}}{2} T_s \\ T'_{c2} = T'_{b2} + \frac{d_{32}}{2} T_s \\ T'_{n2} = T'_{a2} + \frac{d_{12}}{2} T_s \end{cases} \quad \text{(III.43)}$$

III.4.2.1. ZSCC Regulation-based adjusted 3D-SVPWM approach

In this case, as shown in Figure. III.10, a PI regulator is also used to regulate the ZSCC within the proposed adjusted 3D-SVPWM approach, aiming to eliminate the difference Δd_{zx} between the two parallel-connected 4LIs Δd_{zx} by adjusting the control variable y_2 as in Equation (III.44):

$$y_2 = (k_{pz} + \frac{k_{iz}}{s})(i_z^* - i_z) \quad \text{(III.44)}$$

where k_{pz} and k_{iz} are the proportional and integral the gains of the PI regulator for the ZSCC within the proposed adjusted 3D-SVPWM approach, which are expressed by:

$$\begin{cases} k_{pz} = \frac{(L_{f1}+L_{f2})\xi_z \omega_{cz}}{V_{dc}} \\ k_{iz} = \frac{(L_{f1}+L_{f2})\omega_{cz}^2}{V_{dc}} \end{cases} \quad \text{(III.45)}$$

ω_{cz} and ξ_z arethe cutofffrequency and the damping factor of the PI regulator for the ZSCC within the proposed adjusted 3D-SVPWM approach.

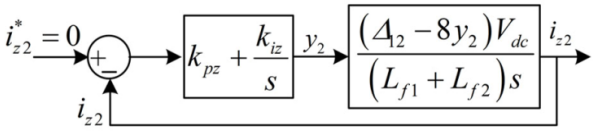


Figure. III.10. Bloc diagram of the PI regulator for the ZSCC within the proposed adjusted 3D-SVPWM approach.

III.5. Control of the parallel connected 4LIs-based reactive power compensation

III.5.1. Application of the adjusted modulation voltage references based SPWM

The overall control structure of the PV grid connected parallel 4LI's system, including the adjusted modulation voltage references based SPWM control method, is illustrated in Figure

III.11. In the following subsections, each control loop withing the overall control structure will be presented.

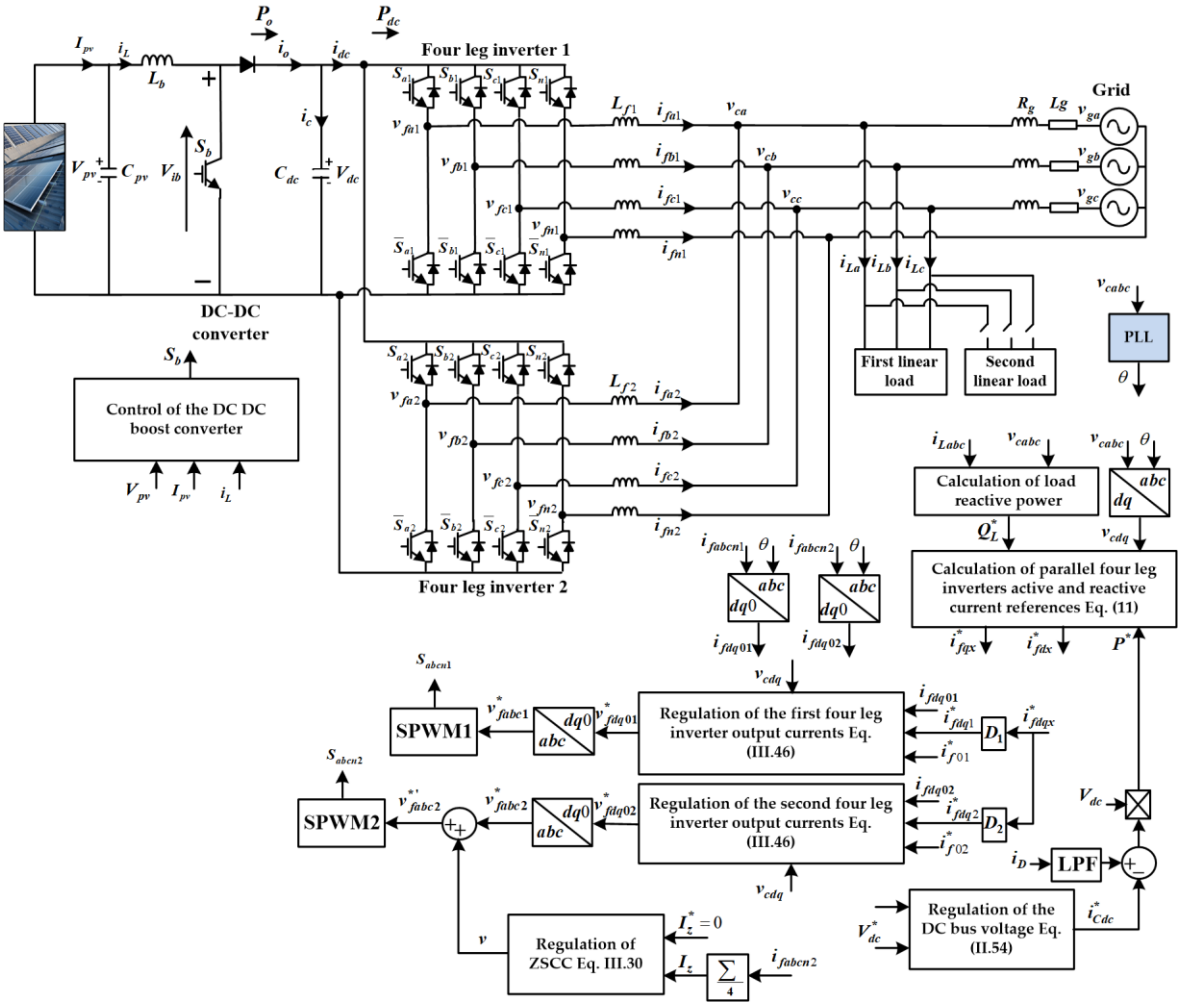


Figure. III.11. Control block diagram of the PV grid connected parallel 4LI system based reactive power compensation using the adjusted modulation voltage references-based SPWM technique.

III.5.1.1. Regulation of the parallel system output currents

The reference modulation voltages for both SPWMs in the dq0 reference frame can be determined by the regulation of the parallel 4LIs output current using PI controllers within the inner current loop of each 4LI as follows:

$$\begin{cases} v_{fdx}^{*} = \left(k_{pid} + \dfrac{k_{iid}}{s}\right)\left(i_{fdx}^{*} - i_{fdx}\right) + v_{cd} + \omega L_{fx} i_{fqx} \\ v_{fqx}^{*} = \left(k_{pid} + \dfrac{k_{iid}}{s}\right)\left(i_{fqx}^{*} - i_{fqx}\right) + v_{cq} - \omega L_{fx} i_{fdx} \\ v_{f0x}^{*} = \left(k_{pi0} + \dfrac{k_{ii0}}{s}\right)\left(i_{f0x}^{*} - \dfrac{i_{fnx}}{\sqrt{3}}\right) + v_{c0} \end{cases} \quad \text{(III.46)}$$

where k_{pidq0} and k_{iidq0} are the inner current loop PI controller parameters and can be calculated using the pole placement technique as follows:

$$\begin{cases} k_{pidqx} = 2L_{fx}\xi_i\omega_{ci} \\ k_{iidqx} = L_{fx}\omega_{ci}^2 \end{cases} \quad \text{(III.47)}$$

$$\begin{cases} k_{pi0} = \frac{8}{\sqrt{3}}L_{fx}\xi_i\omega_{ci} \\ k_{ii0} = \frac{4}{\sqrt{3}}L_{fx}\omega_{ci}^2 \end{cases} \quad \text{(III.49)}$$

where ω_{ci} and ξ_i are the cutoff angular frequency and the damping factor of the inner current loop PI regulators, respectively.

i_{fdq0x}^* denote the filter's current references, which are obtained from the outer load voltage loop as follows:

III.5.1.2. Parallel 4LI's system output current references

The parallel system output reference currents used in both inner control loops are determined based on the active and reactive powers injected/compensated by the system as follows:

$$\begin{cases} i_{fdx}^* = D_1\left(\frac{v_{cd}P^* + v_{cq}Q_L^*}{v_{cd}^2 + v_{cq}^2}\right) \\ i_{fqx}^* = D_2\left(\frac{-v_{cq}P^* + v_{cd}Q_L^*}{v_{cd}^2 + v_{cq}^2}\right) \\ i_{f0x}^* = 0 \end{cases} \quad \text{(III.50)}$$

where D_1 and D_2 represent the active and reactive powers injected/compensated percentage of each 4LI ($D_1 + D_2 = 1$).

III.5.1.3. Active power reference

In PV grid-connected inverter systems, the DC voltage must be maintained constant at a certain voltage level. For this reason, a PI is necessary to maintain the DC voltage constant under all operating conditions. From the DC bus regulation loop, the reference for the active power delivered to the grid P^* can be determined as in Equation (III.51):

$$P^* = V_{dc}\left(-\left(k_{pv} + \frac{k_{iv}}{s}\right)(V_{dc}^* - V_{dc}) + i_D\right) \quad \text{(III.51)}$$

III.5.1.4. Simulation results and discussion

III.5.1.4.1. Performance of the parallel system under difference in the output filter inductances

In this case, the output current sharing of both 4LIs is balanced, and the output inductances are unequal values, where L_{f1}= 10 mH, L_{f2}= 5 mH. The parameters of system and controllers are given in Table A.1 and A2 (Appendix A).

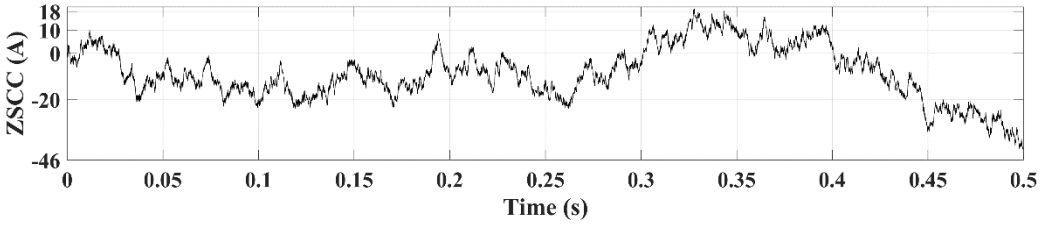
A. Without the control and elimination of ZSCC

The simulation results of the PV parallel 4LIs obtained under difference in the output filter inductances without the application of any ZSCC control and elimination are presented in figure (III.12). The figures from (a) to (d) show respectively the ZSSC, the three phase first 4LI output currents, the three phase second 4LI output currents, the first phase output current of both parallel 4LIs, and the parallel 4LI's system output currents.

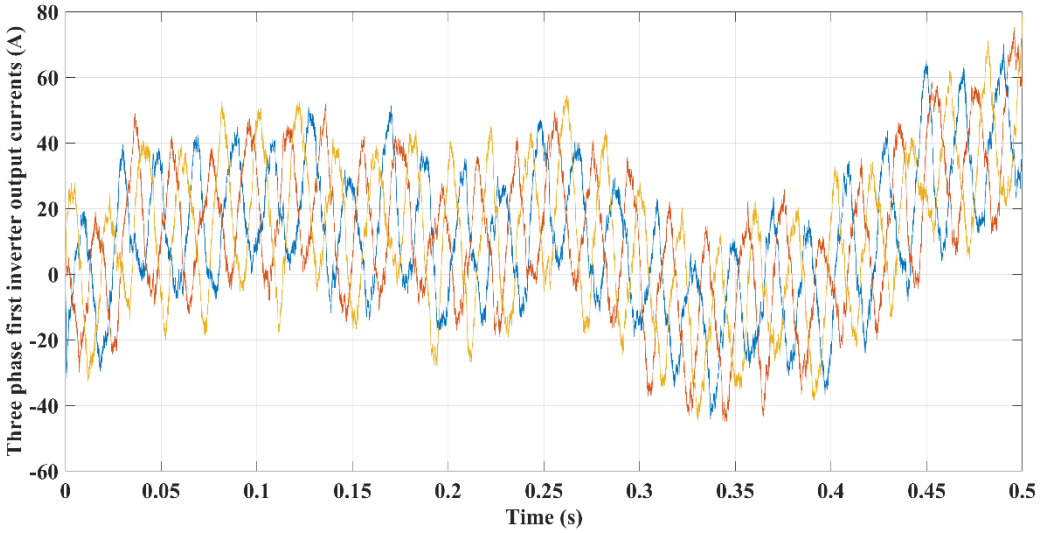
According to Figure (III.12-a), we can observe that the difference in the output filter inductance values causes irregular oscillating ZSCCs. These ZSCCs circulate between the parallel leg of the 4LIs, and as can be seen in Figures (III.12-b) and (III.12-b), they also cause asymmetry and distortion in the three phase currents of each 4LI.

In order to clearly show the effect of the ZSCC on the waveforms of the currents of each 4LI, the first phase output currents of both the parallel 4LIs are shown in Figure (III.12-d). From this figure, we can clearly observe the discrepancy and distortion present in the output currents of the same phase.

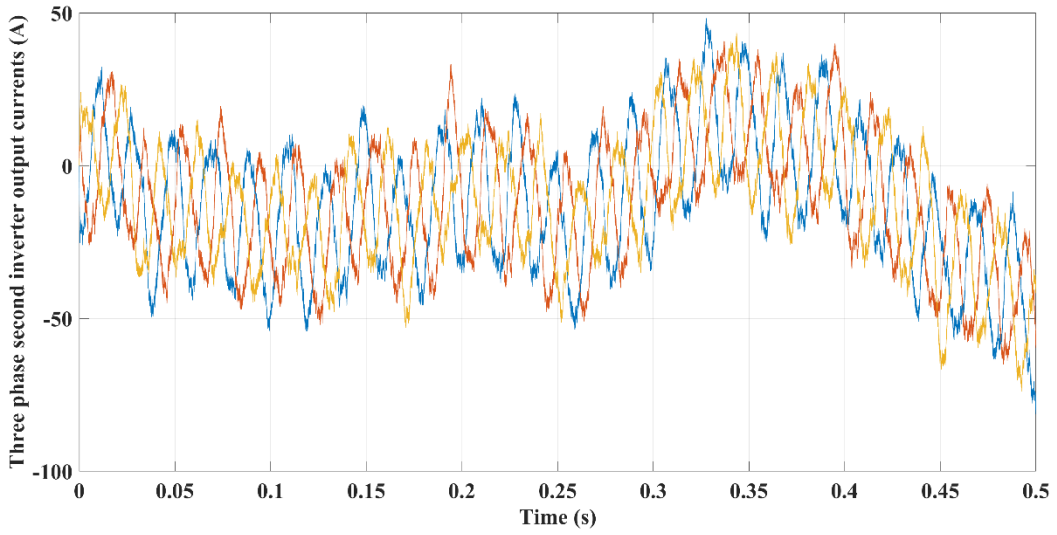
Figure (III.12-e) shows that the total currents generated by the two 4LIs (i_{fpa}, i_{fpb}, i_{fpc}) are balanced and without any distortion. This proves that the ZSCC problem only affects the internal dynamics of the 4LIs. In the following subsections, the performances of parallel 4LIs using the two circulating current elimination methods are explored.



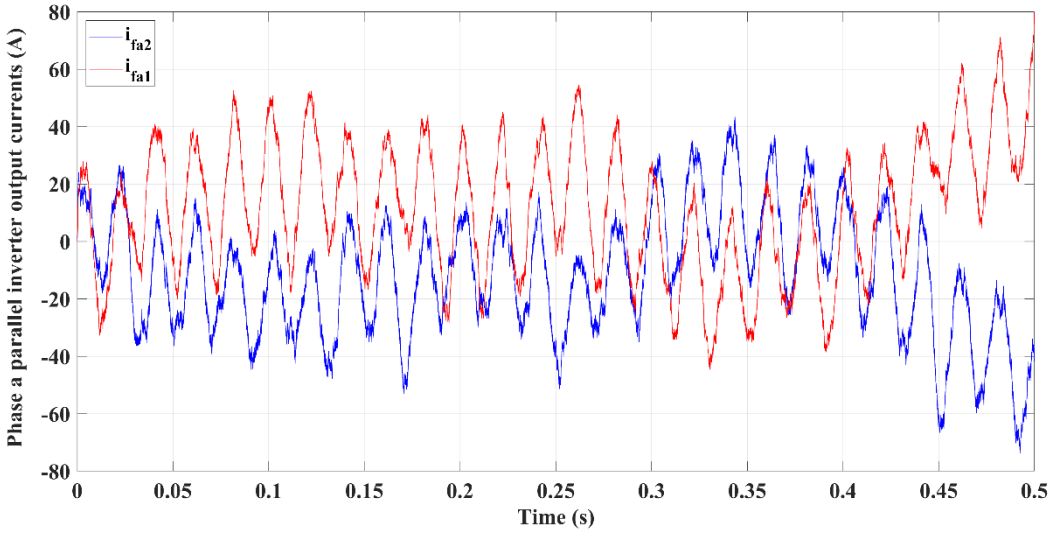
(a)



(b)



(c)



(d)

Figure III.12: Performance of the system controlled using the traditional SPWM under difference in output filter inductance values.

B. Elimination of ZSCC using adjusted modulation voltage references based SPWM

The objective of this test is to evaluate the overall performance of the PV grid connected parallel 4LIs system including the adjusted modulation voltage references based SPWM with respect to changes in solar irradiance and load variation. For this purpose, the following scenario is considered:

1. From $0 < t < 0.5$ s, Stable operation at 1000 W/s irradiance with 8 Ω and 8 mH load;
2. From $0.5 < t < 0.75$ s, Irradiance decrease from 1000 W/s to 600 W/s with 8 Ω and 8 mH load;
3. From $0.75 < t < 1$ s, Irradiance increase from 600 W/s to 800 W/s with 8 Ω and 8 mH load;

4. From 1< *t* <1.25 s, Irradiance increase from 800 W/s to 1000 W/s with 8 Ω and 8 mH load;
5. From 1.25 < *t* <1.5 s, Load change from 8 Ω and 8 mH to 4 Ω and 4 mH with 1000 W/s Irradiance.

Simulation results

The simulation results of this test are presented in Figures III.13 and III.14. Figures (a) to (e) in Figure III.13 respectively show: the active powers of the parallel system, the three-phase grid currents, the reactive powers of the parallel system, the first-phase grid voltage along with its current, and the DC bus voltage. Meanwhile, Figures (a) to (d) in Figure III.14 respectively illustrate: the ZSCC, the three-phase output currents of the first 4LI, the three-phase output currents of the second 4LI, and the first-phase output current of both parallel 4LIs.

Figure (III.13-a) depicts the active power distribution among the PV grid-connected parallel 4LI's system components (P_{grid}, P_{load}, $P_{inverter}$, and P_{PV}). It can be seen from this figure that before the variation in solar irradiance ($0 \leq t \leq 0.5$ s), the system active power flow stabilizes with the load active power demand (P_{load}) at approximately 17 kW, while P_{PV} stabilizes at around 12 kW. The two parallel 4LIs inject all the active power produced by the PV generator ($P_{inverters}$ at ~12 kW), and because this active power is less than the active power needed to satisfy the linear load demand, the remaining active power (around 5 kW) is absorbed from the three-phase grid.

During the second operation phase when the solar irradiance decreases ($0.5 \leq t \leq 0.75$ s), the PV power output adjusts accordingly and decreases to approximately 7 kW. As shown in Figure (III.13-a), the grid power increases to around 10 kW to maintain load supply and guarantee system power flow stability (the load continues to draw constant power).

When the solar irradiance increases during the third operation phase ($0.75 \leq t \leq 1$ s) and further increases during the fourth operation phase ($1 \leq t \leq 1.25$ s), the PV power output adjusts accordingly, increasing to around 9 kW during the third phase and to approximately 12 kW during the fourth operating phase. The grid power decreases proportionally during both operation phases to maintain the load supply and guarantee system active power flow stability.

The most dramatic change occurs after t=1.25s with the load change, where P_{load} increases substantially to approximately 32 kW, and P_{grid} increases to about 21 kW, indicating the system's ability to handle higher load demands while maintaining system active power flow stability. During this operation phase, the $P_{inverters}$ remains around 11 kW, slightly lower than P_{PV}, suggesting that the two parallel 4LIs cannot inject the total active power produced by the PV generator, likely due to the increased load reactive power demand. In this case, the parallel 4LIs allocate part of their capacity to compensate for the load reactive power demand while guaranteeing system active and reactive power flow stability.

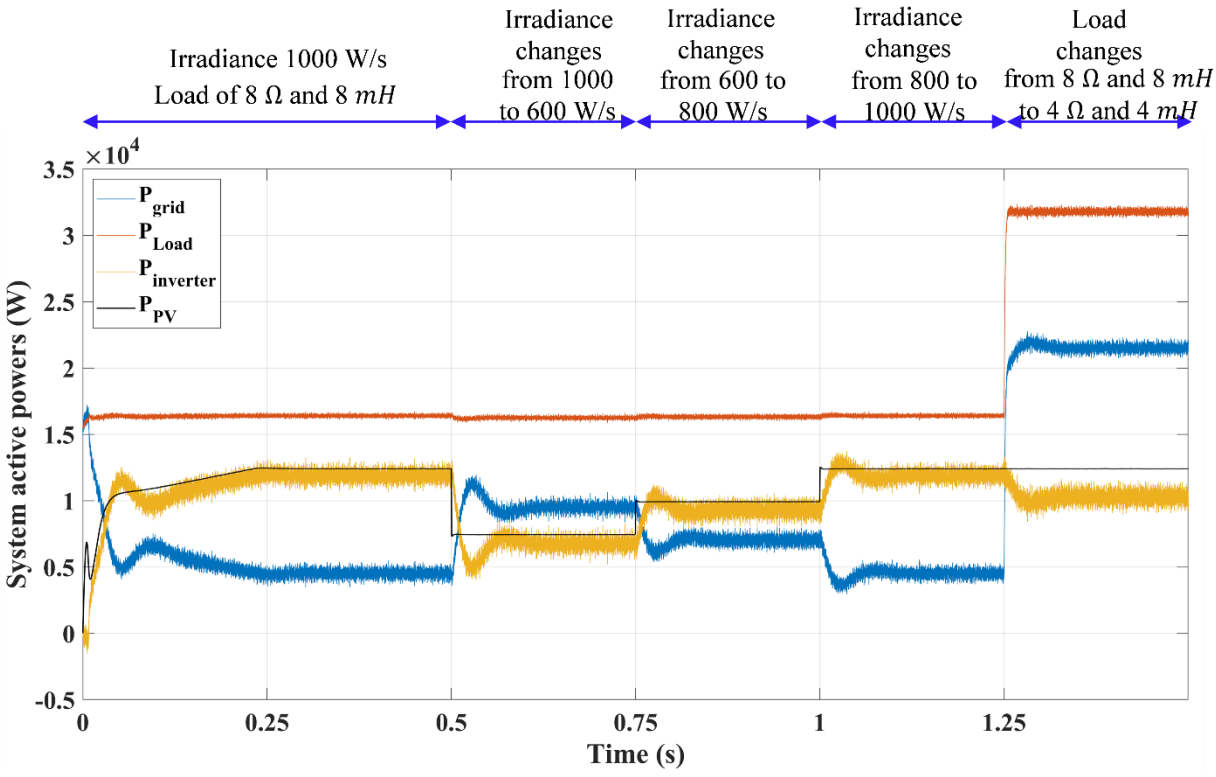
Figure (III.13-b) shows the three phase grid currents (i_{gabc}). During stable operation, the three-phase currents maintain consistent amplitude. When irradiance drops at t=0.5s, the grid current

amplitude decreases proportionally, showing the system's ability to adjust power injection. The subsequent irradiance increases at t=0.75s and t=1.0s show corresponding increases in grid current amplitude. At t=1.25s, when the load changes to 4 Ω and 4 mH, there's a significant increase in grid current amplitude, demonstrating the system's response to increased load demand.

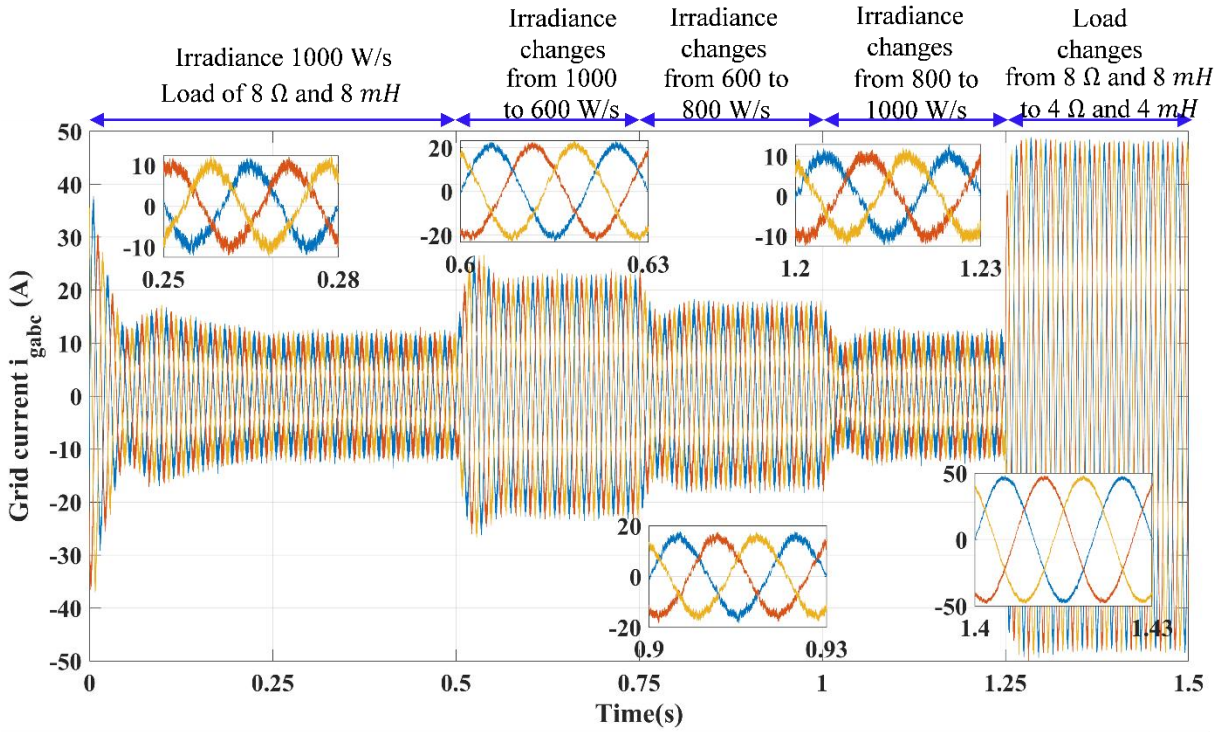
Figure (III.13-c) shows the system reactive power distribution among the PV grid-connected parallel 4LI's system components (Q_{grid}, Q_{load}, and $Q_{inverter}$). From this figure, we can clearly see that the two 4LIs compensate for all the reactive power demanded by the load and maintains fairly constant reactive power throughout irradiance changes, with Q_{grid} near zero, suggesting good power factor control. When the load is changed at t = 1.25 s during the fourth operating phase, significant jump in Q_{load} and $Q_{inverter}$ are accord, demonstrating the increased reactive power demand of the new load and the two 4LIs are compensate for all the reactive power needed by the new linear load and maintains Q_{grid} near zero, suggesting good power factor control.

Figure (III.13-d) presents the first phase grid voltage (v_{ga}/10) and its current (i_{ga}) waveforms. This figure demonstrated that the grid current is always in phase with its voltage under different solar irradiance, maintaining proper phase relationship despite irradiance changes, indicating effective power factor control. When the load changes at t=1.25s, there's a noticeable increase in grid current amplitude, but phase synchronization is maintained, suggesting good power factor control under different operating phases.

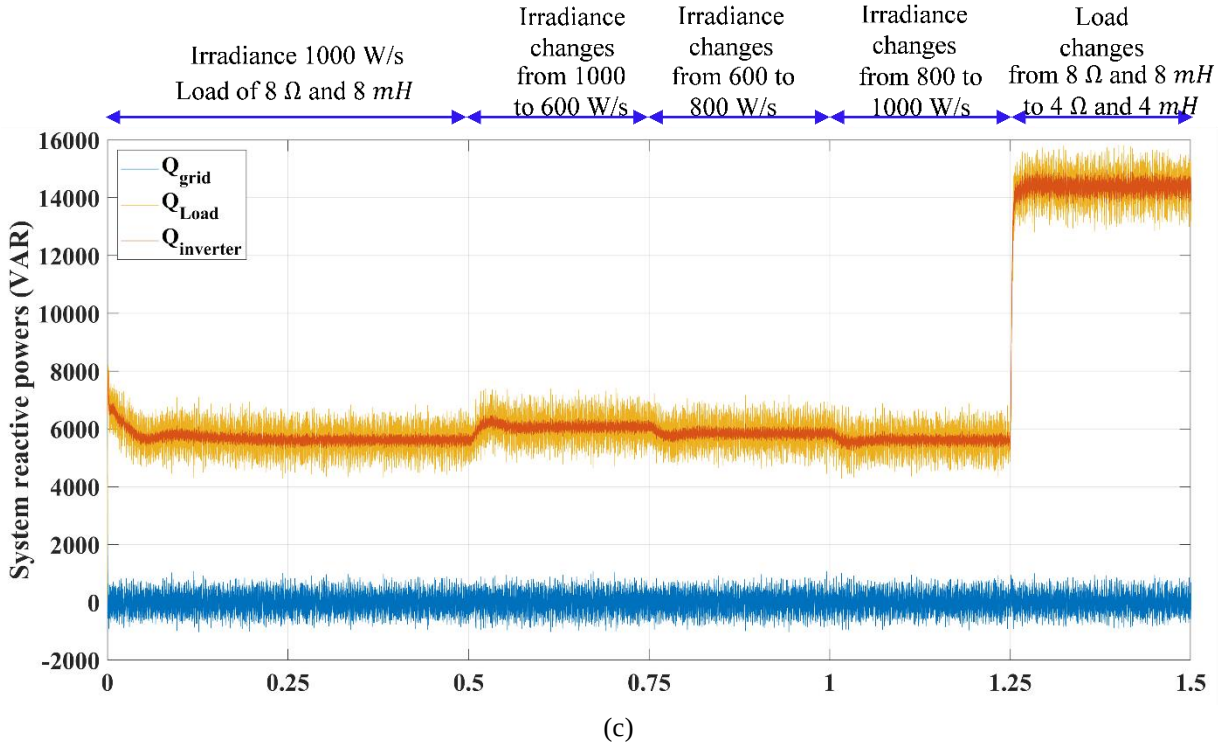
Figure (III.13-e) shows that the DC voltage is well regulated with its reference with some fluctuations during variations in solar irradiance and load.



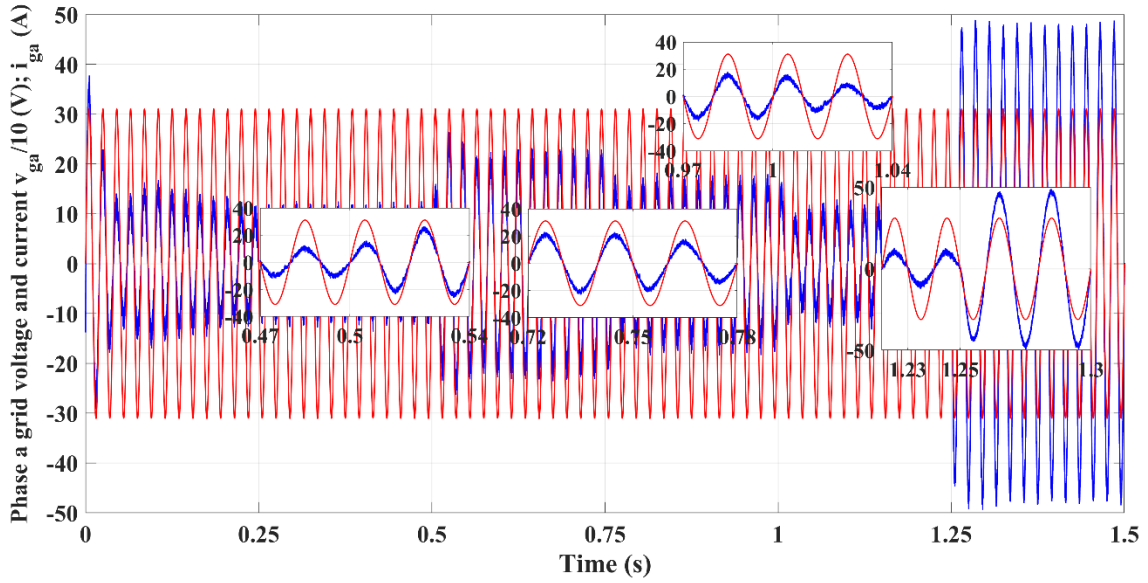
(a)


Irradiance 1000 W/s
Load of 8 Ω and 8 mH
Irradiance changes from 1000 to 600 W/s
Irradiance changes from 600 to 800 W/s
Irradiance changes from 800 to 1000 W/s
Load changes from 8 Ω and 8 mH to 4 Ω and 4 mH
Grid current i_{gabc} (A)
Time(s)

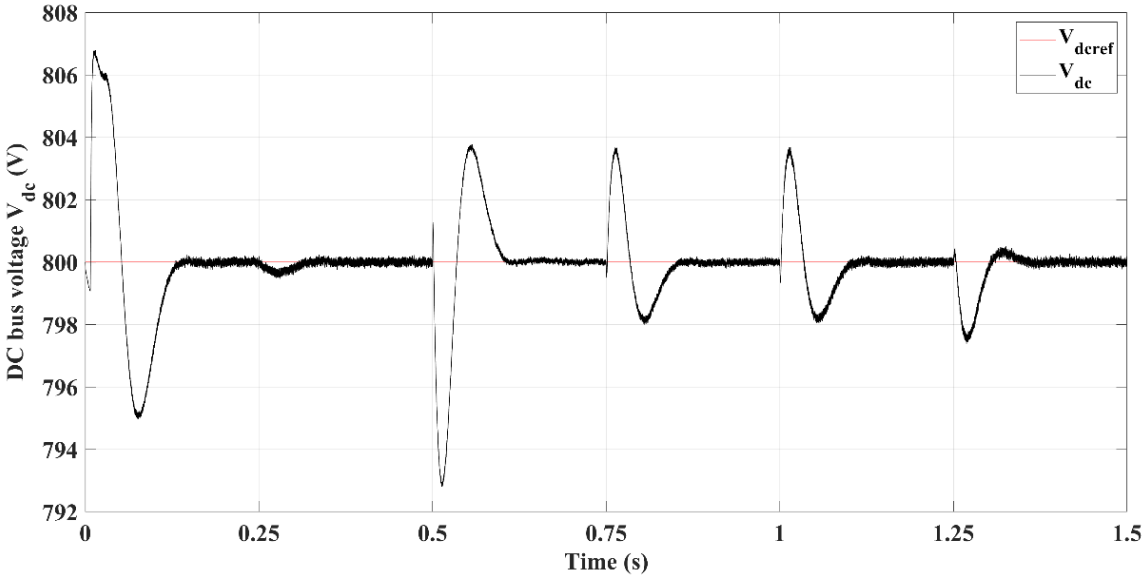
(b)


Irradiance 1000 W/s
Load of 8 Ω and 8 mH
Irradiance changes from 1000 to 600 W/s
Irradiance changes from 600 to 800 W/s
Irradiance changes from 800 to 1000 W/s
Load changes from 8 Ω and 8 mH to 4 Ω and 4 mH
Q_{grid}
Q_{Load}
$Q_{inverter}$
System reactive powers (VAR)

(c)



(d)



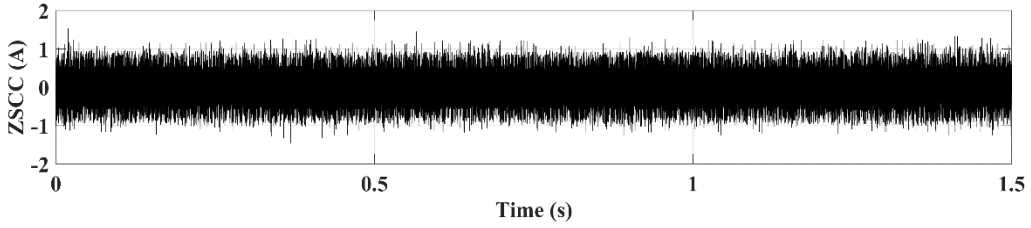
(e)

Figure III.13: Performance of the overall system controlled using the adjusted modulation voltage references based SPWM under unbalanced output filter inductances and the changes of irradiance and load.

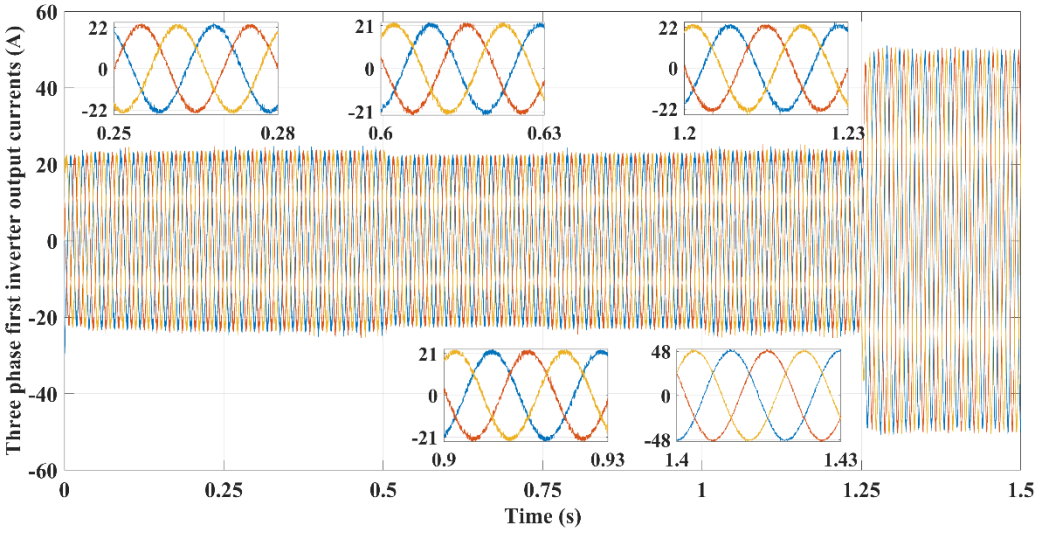
Figures (III.14-a) show that, despite the parallel two 4LIs operating with different filter inductance values as well as varying solar irradiance and load conditions, the ZSCC is well controlled around the zero with a somewhat larger peak to peak value in all operating phases due to the use of the adjusted modulation voltage references based SPWM control method.

Figures (III.14-b) to (III.14-d) illustrate the output currents of each 4LI within the parallel system and the first phase output current of both 4LIs. These results demonstrated that despite the parallel 4LIs having different output filter inductances and operating under variable solar

irradiance and load conditions, the three-phase output currents of each 4LI are well balanced, and the output currents in all parallel phases are identical, with no distortion or asymmetry observed during load variations. This further validates the proper operation of both parallel 4LIs withing the overall system and the effectiveness of the used adjusted modulation voltage references based SPWM control method.



(a)



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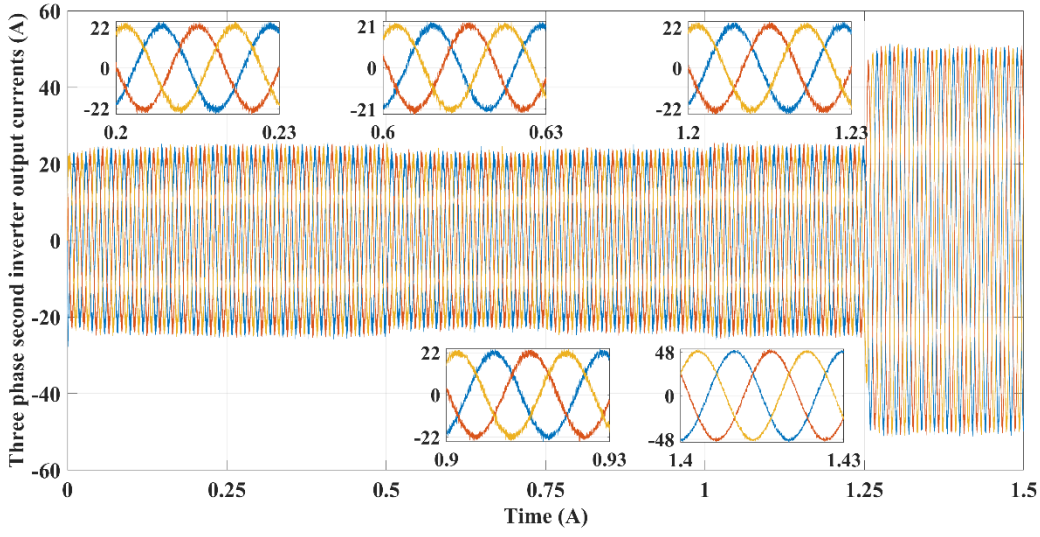

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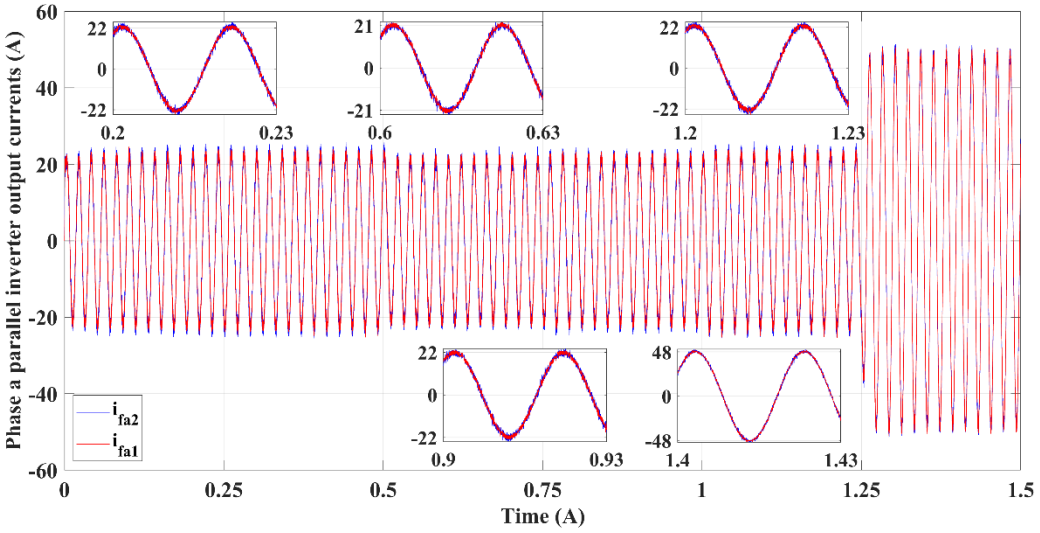
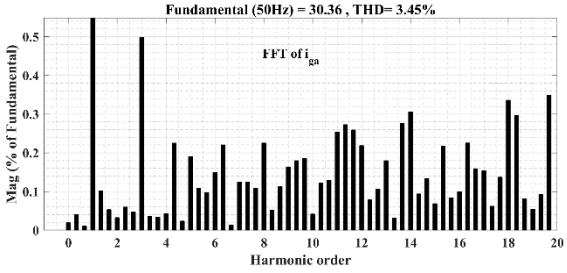


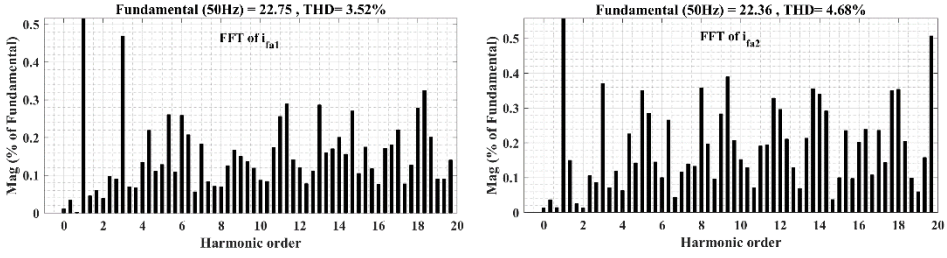
(d)

Figure III.14: Performance of the adjusted modulation voltage references based SPWM under unbalanced output filter inductances and the changes of irradiance and load.

The THD of both the grid currents and parallel 4LIs output currents are given in Figure III.15. It can be seen that the THD of both the grid currents and parallel 4LIs output currents are within the 5%, which confirmed by the IEEE 519-2 standard.



(a)



(b) (c)

Figure III.15: Harmonic spectrums. (a) first phase grid current, (b) first phase of first 4LI output current, (c) first phase of second 4LI output current

Overall, the results of this test demonstrate that the adjusted modulation voltage references based SPWM can effectively manages the PV grid-connected parallel 4LI system under unequal output inductances as well as under varying irradiance and load conditions. The controller

maintains stability during transitions, properly tracks power changes with changing irradiance, ensures appropriate power sharing between PV, grid, and load, and ensures ZSCC elimination and parallel 4LI's output current quality improvement. However, despite these performances, the parallel 4LIs controlled using the adjusted modulation voltage references based SPWM can provide large ZSCC peak to peak value, loading to high output current ripples and THDs. Thereby, to further improve the performance of the parallel 4LIs in terms of ZSCC elimination and output current ripples reduction, the adjusted 3DSVPWM is implemented in the control of the parallel 4LIs in the following subsection instead of adjusted modulation voltage references based SPWM.

C. Application of the proposed adjusted 3DSVPWM

The overall control structure of the PV grid connected parallel 4LI's system, including the proposed adjusted 3DSVPWM's zero-vector duty ratios approach, is illustrated in Figure (III.16). The simulation results of this control method are shown in Figures. III.17 and III.18. Figures (a) to (e) in Figure III.17 respectively show: the active powers of the parallel system, the grid currents, the reactive powers of the parallel system, the first-phase grid voltage along with its current, and the DC bus voltage. Additionally, Figures (a) to (d) in Figure III.18 respectively illustrate: the ZSCC, the three-phase output currents of the first 4LI, the three-phase output currents of the second 4LI, and the first-phase output current of both parallel 4LIs.

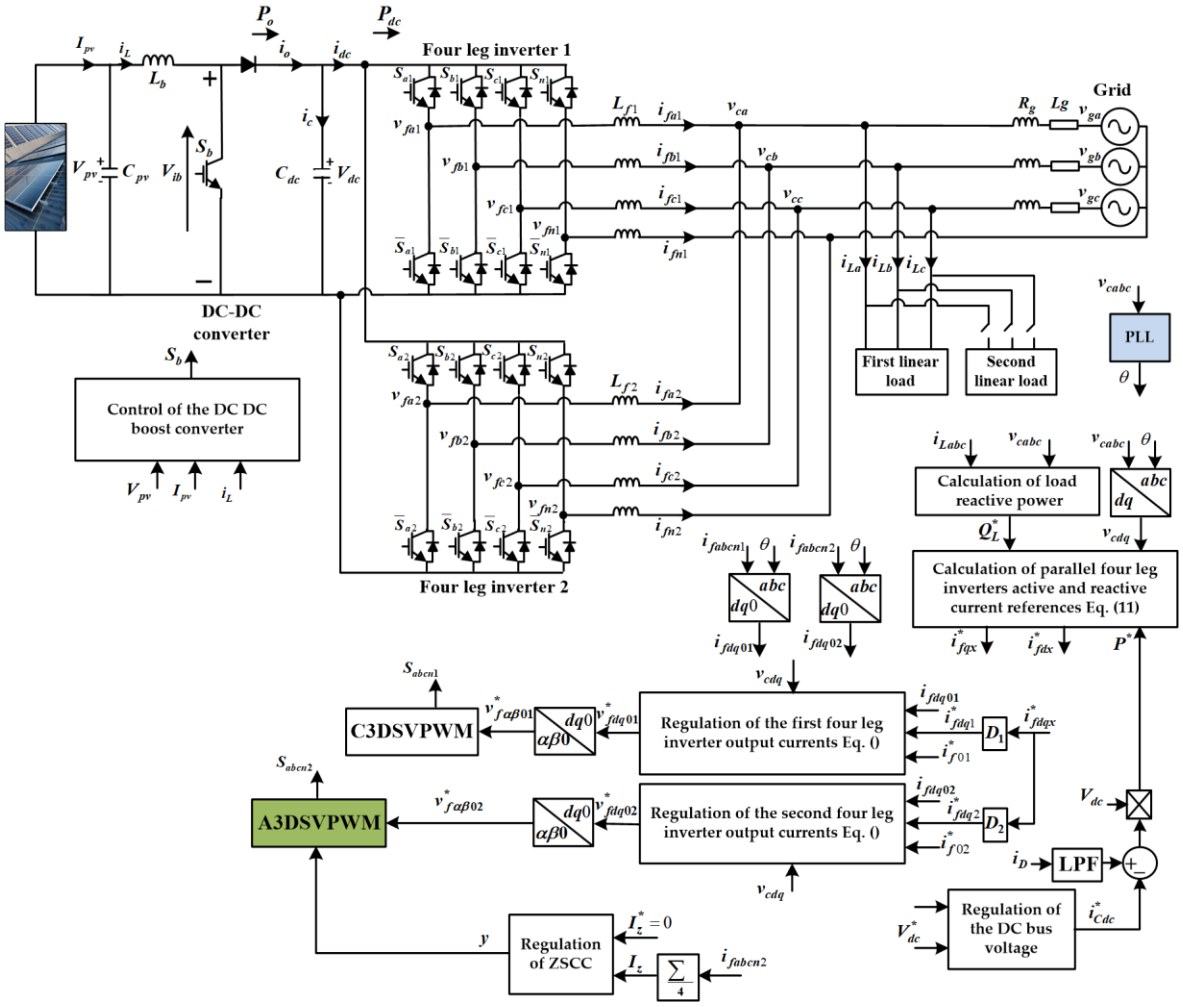


Figure. III.16. Control block diagram of the PV parallel 4LI grid connected system based reactive power compensation using the proposed adjusted 3DSVPWM.

The model of the ZSCC, derived after adjusting the ZSDR in the 3DSVPWM formulation (as shown in Equation III.42, results in a first-order system. This simplification facilitates the design of a closed-loop ZSCC control strategy. In this approach, a PI controller is employed to attenuate ZSCC harmonics that may influence the harmonic content of the parallel 4LI's output currents, as illustrated in Figure III.17. Unlike the PI regulation applied directly to the ZSCC-based adjusted modulation voltage references, the objective here is regulate circulating current-based adjusted 3DSVPWM to suppress the difference in ZSDRs among the two parallel 4LIs (Δd_{zx}) using the adjusting variable y_2 through the PI controller. This is achieved by regulating the adjusting variable y_2 derived through the ZSCC-based adjusted 3DSVPWM using the PI controller as follows:

$$y_2 = (k_{pz} + \frac{k_{iz}}{s})(i_z^* - i_z) \quad \text{(III.52)}$$

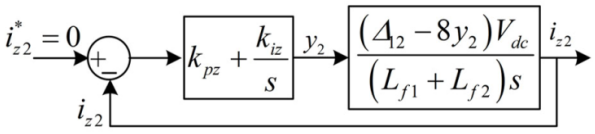


Figure. III.17: Bloc diagram of the PI loop of ZSCC-based adjusted 3DSVPWM

Simulation results

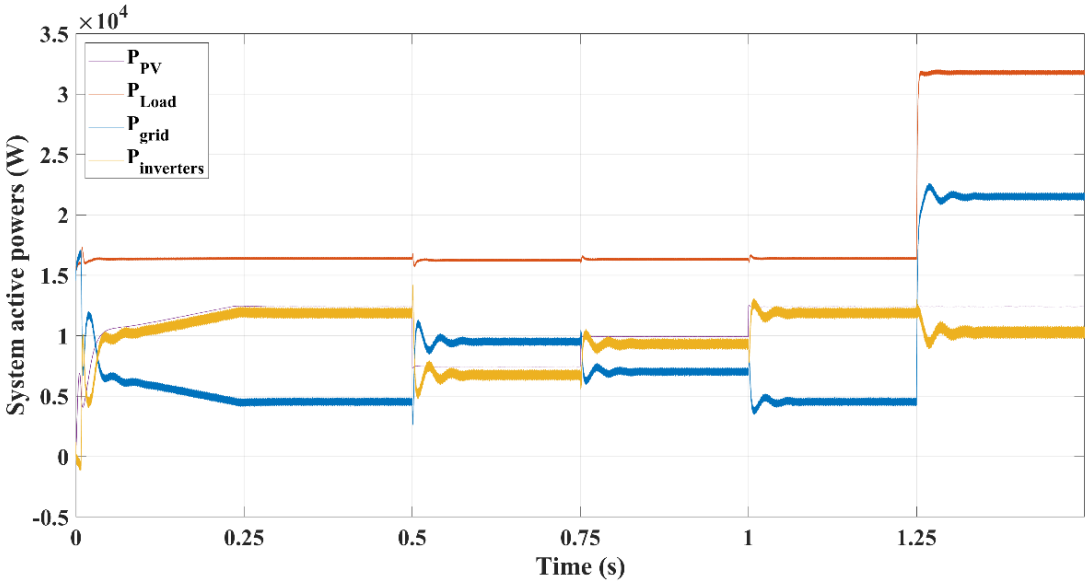
Figures III.18(a) to (e) present the simulation results of the proposed adjusted 3D-SVPWM method applied to the parallel 4LIs system under the same unbalanced filter and irradiance variation conditions used in Test B.

Figure III.18(a) shows the ZSCC between the two parallel inverters. The waveform reveals that the proposed adjusted 3D-SVPWM achieves almost complete elimination of the ZSCC. The amplitude of the circulating current is drastically reduced compared to that observed in Test B, where small residual oscillations remained. Under the proposed method, the ZSCC converges rapidly to zero with negligible steady-state error, confirming the PI-based regulation efficiency and the successful dynamic adjustment of zero-vector duty ratios.

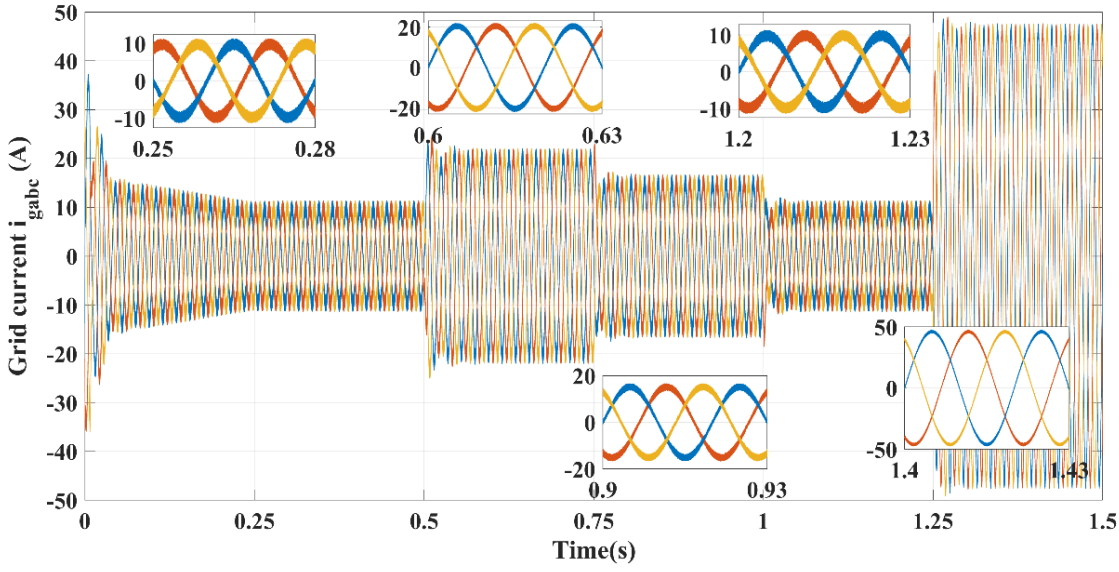
Figures III.18(b) and 18(c) illustrate the three-phase output currents of the first and second inverters, respectively. The currents of both 4LIs are nearly identical in amplitude and perfectly in phase, demonstrating excellent current sharing and synchronous behavior between parallel modules. Unlike the adjusted SPWM approach in Test B, where slight current unbalances and harmonic distortions persisted due to limited ZSV compensation, the adjusted 3D-SVPWM yields smoother sinusoidal waveforms with minimal distortion and harmonic content.

Figure III.18(d) displays the first-phase output currents of both inverters (i_{fa1} and i_{fa2}). The overlap of the two waveforms confirms that the proposed method achieves near-perfect synchronization and complete elimination of current mismatch. In contrast, the previous SPWM-based control still showed small amplitude discrepancies and phase lag between the two inverter currents, particularly during transients in irradiance and load changes.

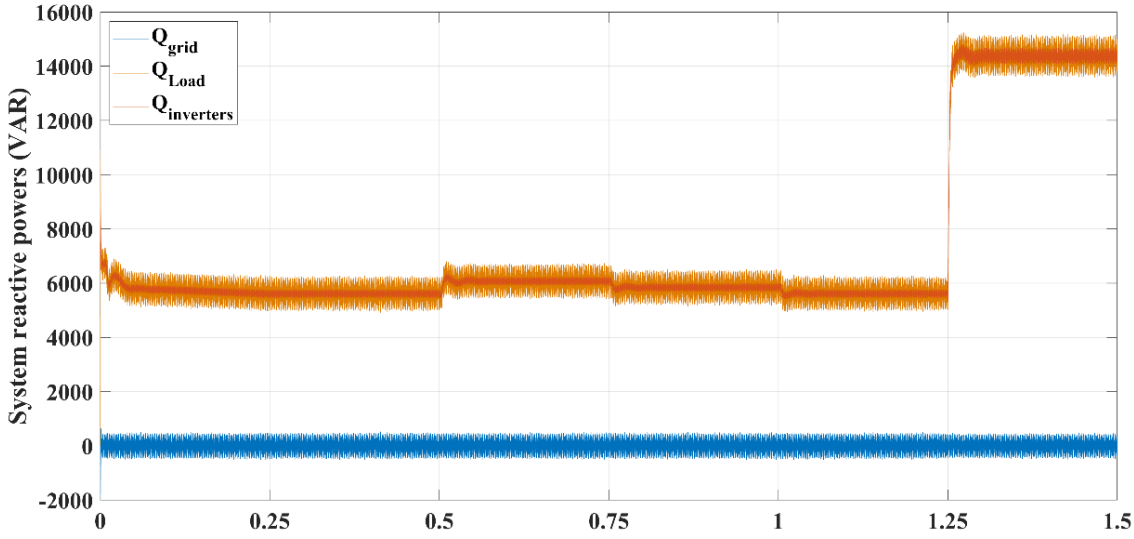
Figure III.18(e) presents the total output current of the parallel inverter system delivered to the grid. The waveform remains purely sinusoidal and balanced throughout the test, confirming that the proposed control not only suppresses internal circulating currents but also preserves high-quality grid current injection even under varying solar irradiance and load conditions.


×10^4
P_PV
P_Load
P_grid
P_inverters
System active powers (W)
Time (s)

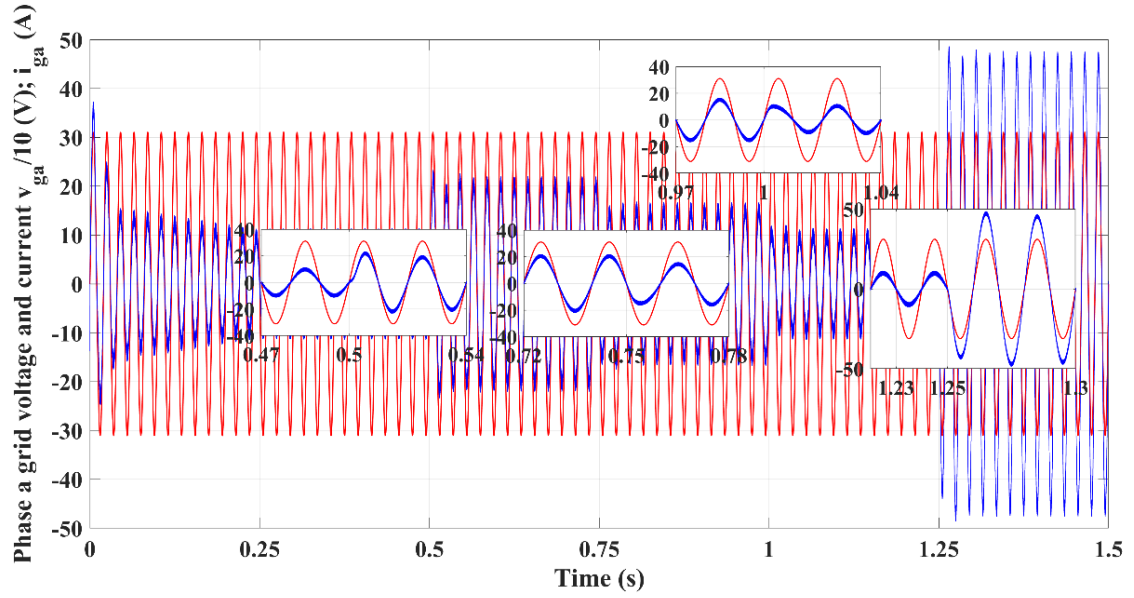
(a)


Grid current i_gabc (A)
Time(s)

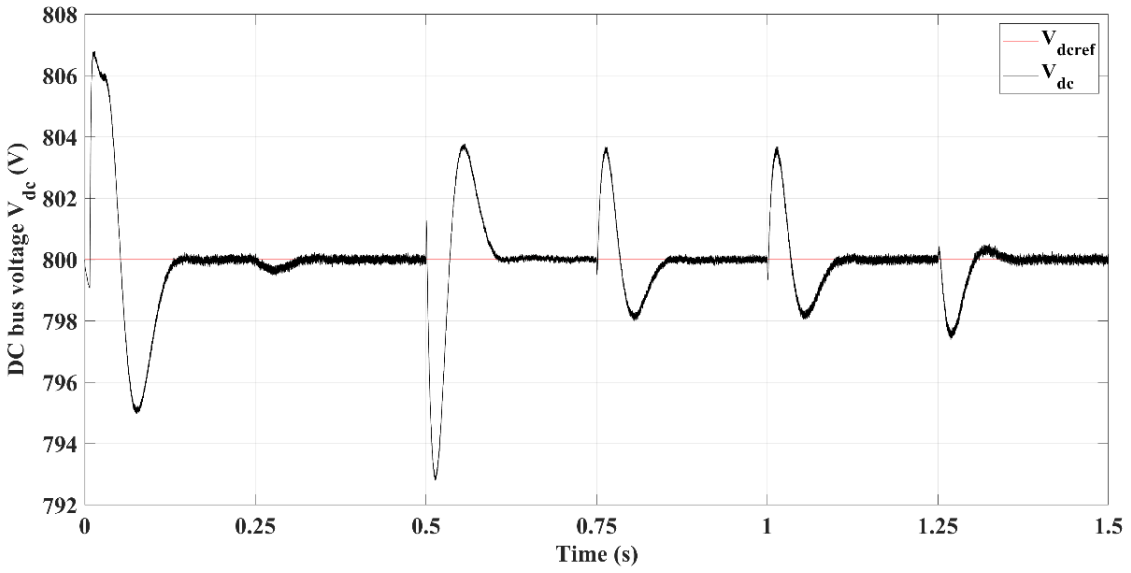
(b)


Q_grid
Q_Load
Q_inverters
System reactive powers (VAR)
16000
14000
12000
10000
8000
6000
4000
2000
0
-2000
0
0.25
0.5
0.75
1
1.25
1.5

(c)


Phase a grid voltage and current v_ga /10 (V); i_ga (A)
Time (s)
50
40
30
20
10
0
-10
-20
-30
-40
-50
0
0.25
0.5
0.75
1
1.25
1.5
0.47
0.5
0.54
0.72
0.75
0.78
0.97
1
1.04
1.23
1.25
1.3

(d)

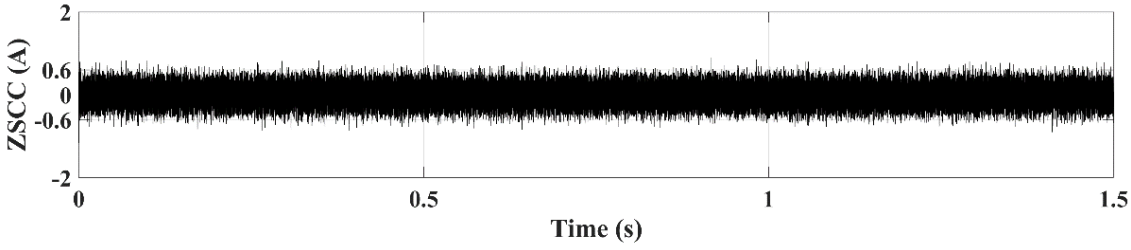


(e)

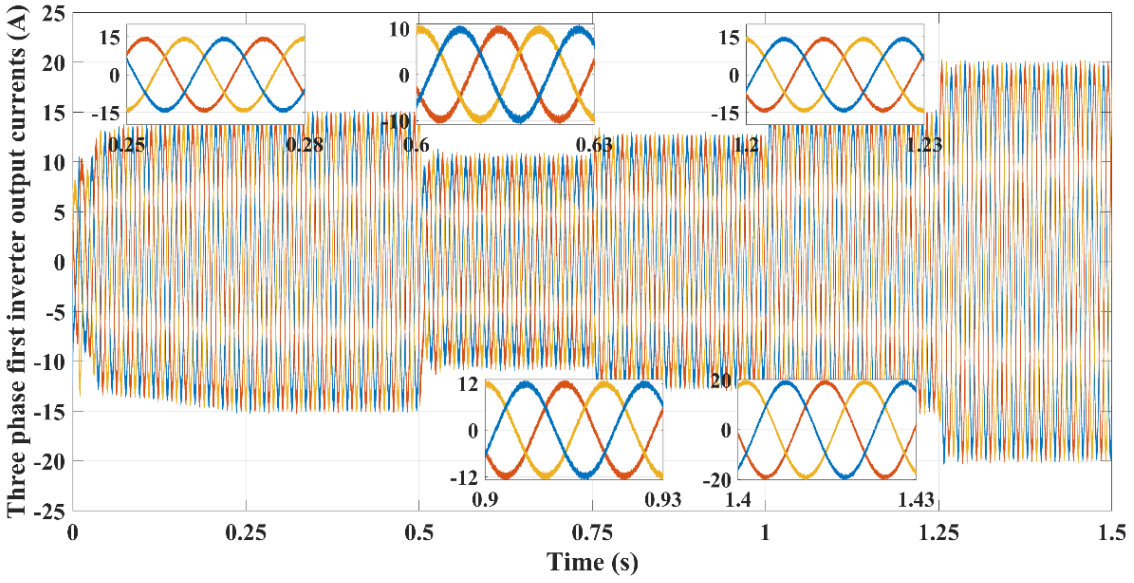
Figure III.18: Performance of the overall system controlled using the adjusted 3DSVPWM under unbalanced output filter inductances and the changes of irradiance and load.

Figures III.19-a show that, despite the parallel two 4LIs operating with different filter inductance values as well as varying solar irradiance and load conditions, the ZSCC is well controlled around the zero with a somewhat larger peak to peak value in all operating phases due to the use of the adjusted modulation voltage references based SPWM control method.

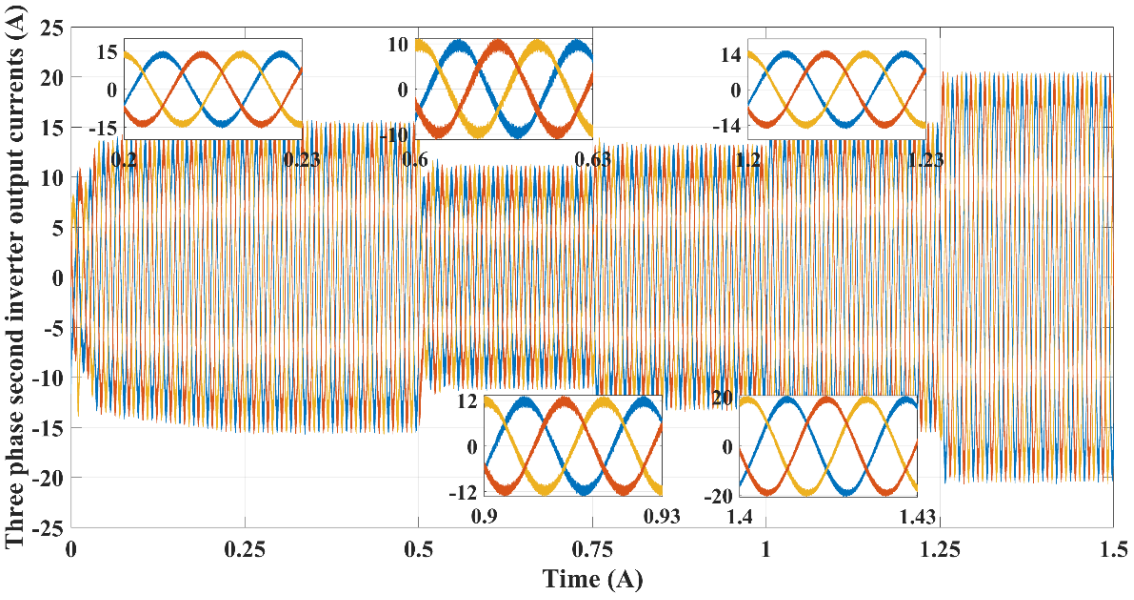
Figures III.19-b to III.19-d illustrate the output currents of each 4LI within the parallel system and the first phase output current of both 4LIs. These results demonstrated that despite the parallel 4LIs having different output filter inductances and operating under variable solar irradiance and load conditions, the three-phase output currents of each 4LI are well balanced, and the output currents in all parallel phases are identical, with no distortion or asymmetry observed during load variations. This further validates the proper operation of both parallel 4LIs withing the overall system and the effectiveness of the used adjusted modulation voltage references based SPWM control method.



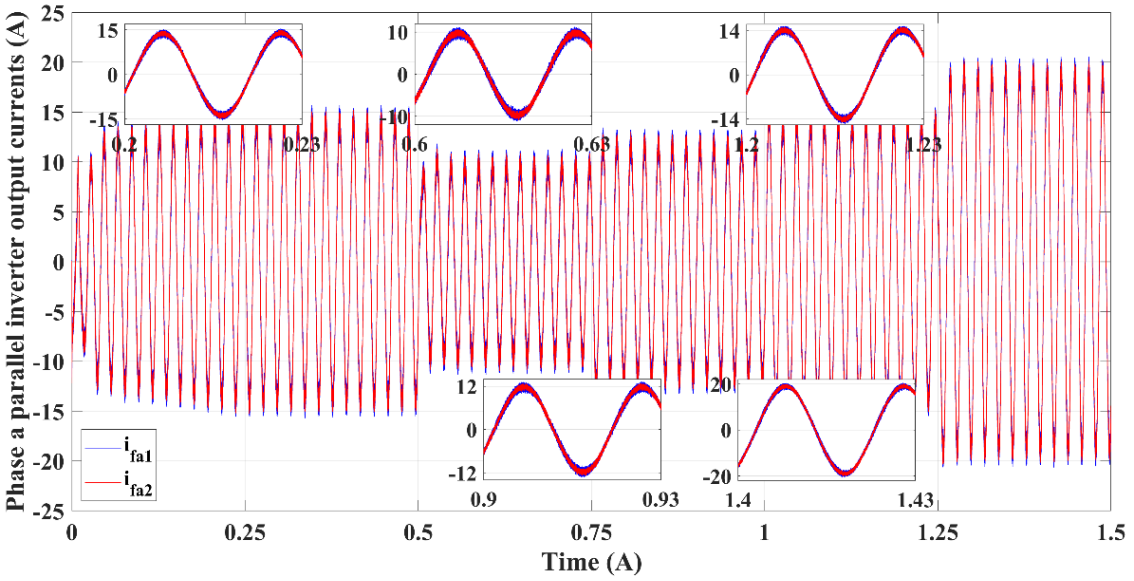
(a)


Three phase first inverter output currents (A)
Time (s)

(b)


Three phase second inverter output currents (A)
Time (A)

(c)



(d)

Figure III.19: Performance of the adjusted 3DSVPWM under unbalanced output filter inductances and the changes of irradiance and load.

Table. III. 1: Comparison between the Adjusted SPWM (Test B) and the Proposed Adjusted 3D-SVPWM

Aspect	Adjusted SPWM (Test B)	Proposed Adjusted 3D-SVPWM (Test C)
ZSCC elimination	Partial suppression; residual low-frequency oscillations remain.	Complete elimination in steady-state.
Inverter output current quality	Moderate improvement; small harmonic distortion visible.	Excellent waveform quality; nearly ideal sinusoidal currents.
Current sharing	Slight mismatch between inverter currents under dynamic conditions.	Perfect current balance and synchronization between inverters.
Overall performance	Effective but limited by SPWM modulation in abc frame.	Superior performance due to direct zero-vector duty-ratio control in 3D-SVPWM.

Overall, the results demonstrate that the proposed adjusted 3D-SVPWM approach provides a significant enhancement in both ZSCC suppression and output current quality compared with the adjusted SPWM strategy. By dynamically regulating the zero-vector duty ratios through the PI-controlled adjustment variable, the method effectively neutralizes ZSV differences between parallel inverters. Consequently, the parallel 4LI system exhibits high-quality sinusoidal currents, balanced power sharing, and complete ZSCC elimination, leading to superior overall system stability, efficiency, and reliability.

III.6. CONCLUSIONS

This chapter introduces an innovative method for suppressing circulating current in PVG grid connected parallel-operated 4LIs, particularly under various unbalance scenarios including the unbalanced of output filter inductances and current sharing among parallel 4LIs. The proposed strategy focuses on minimizing the discrepancy in zero-sequence duty voltages between 4LIs. This is achieved through a newly adapted adjusted 3D-SVPWM approach, in which the zero-vector duty cycles are dynamically regulated using a correction factor derived from a dedicated ZSCC-PI control loop. This method proves highly effective in reducing ZSCC and also contributes to the regulation of the fourth-leg current while significantly suppressing third-order harmonic content in the output.

When compared with other existing ZSCC mitigation techniques used in parallel four-leg inverter systems, the modified 3D-SVPWM technique stands out by achieving the smallest peak-to-peak ZSCC levels. Notably, this peak remains below 0.6 A even in the presence of imbalanced filter inductances and unequal current sharing, across both balanced and unbalanced three-phase linear load conditions. Moreover, this technique exhibits superior performance in lowering harmonic distortion in the output currents, primarily due to its effective reduction of the third harmonic. These findings confirm that the circulating current strategy effectively addresses the issues of waveform distortion and asymmetrical current flow caused by ZSCC, even under challenging operating conditions. Importantly, this solution is implemented without the need for extra hardware, enhancing its cost-effectiveness and practical appeal.

During the steady-state operation of a grid-connected PV inverter system, the PV and parallel 4LIs system power levels remain balanced (i.e., Ps=Pdc), and the DC-bus voltage is maintained at its nominal value. In this configuration, the PV not only injects active power but also provides reactive power support to the grid, compensating for the reactive demand of the connected three-phase linear inductive loads. However, this balance can be disrupted by unexpected disturbances such as fluctuations in cell temperature, solar irradiance, or grid voltage. For example, under a solar irradiance sag, the active power generated by the PV source decreases, leading to a temporary mismatch between the PV output and the power delivered to the grid. In the short term, this reduction in PV generation causes a deficit of energy ($\Delta P<0$) at the DC-bus, resulting in a voltage drop and reduced capacitor current.

This imbalance not only stresses the DC-bus capacitor but also propagates to the AC side, where the parallel 4LIs output currents are significantly disturbed. In particular, the grid currents may exhibit distortion, overshoot, and tracking errors as the parallel 4LIs system attempts to regulate the DC-bus voltage, while its ability to supply reactive power support is diminished due to the diversion of control effort toward voltage stabilization. Such effects not only deteriorate parallel 4LIs system current tracking accuracy and power quality but may also compromise system stability if the disturbance persists. In addition to external disturbances, parametric uncertainties, such as variations in the DC-bus capacitance or parallel 4LIs system output filter inductances, can further degrade the system's dynamic response and stability. If these problems are not addressed promptly, excessive voltage and current stress may damage the DC-bus

capacitor and adversely affect the operation of other equipment. Therefore, strong robustness against both unknown disturbances and parameter uncertainties is an essential requirement for DC-bus voltage and parallel 4LIs system output current regulations, since such factors can deteriorate the parallel 4LIs system DC bus voltage and output current tracking performances, impair reactive power compensation, and threaten the overall stability and reliability of the system.

To address the issues of control sensitivity to disturbances and parametric uncertainties, we will introduce a second type of control approach, namely active disturbance rejection control method (ADRC). This method aims to tackle the identified challenges, including robustness, system stabilization, trajectory tracking, response time, disturbance rejection, bidirectional power flow, unity power factor, and reduced harmonic distortion in the parallel 4LIs system output currents. This topic will be the focus of the next chapter.

Chapter 4
Active Disturbance Rejection Control method for PVG grid connected parallel four leg inverters system

IV.1. Introduction

Despite the topological advantages of 4LIs, their control remains a formidable challenge, especially when operating in parallel configurations for PV grid-connected applications. The complexity arises from multiple interacting factors that create a highly nonlinear, time-varying, and uncertain system. Dynamic coupling phenomena play a significant role, as strong interdependence exists between the DC bus voltage dynamics and AC-side output currents, where disturbances in one domain immediately affect the other [185]. In addition, cross-coupling between the d-axis and q-axis current components in the rotating reference frame makes independent control of active and reactive power difficult [186,187]. Interaction between the neutral current (zero-sequence component) and the three-phase currents further complicates control, particularly in the presence of unbalanced loads [188].

Parametric uncertainties also exacerbate the problem. Variations in DC bus capacitance due to aging, temperature effects, and manufacturing tolerances degrade voltage regulation [189]. Output filter inductance variations or mismatches between parallel inverters can cause unequal

current sharing and circulating currents [190]. Furthermore, the grid impedance itself is uncertain, changing with network configuration and operating conditions [191,192]. These internal challenges are compounded by external disturbances such as irradiance fluctuations caused by passing clouds [193], temperature variations affecting both PV panel output and power electronic components, and grid voltage sags or swells triggered by faults or load switching events [194]. Load variations and grid frequency deviations further demand adaptive synchronization and control mechanisms [195]. In parallel operation, ZSCC emerge as a major concern, causing additional losses, thermal stress, and potential instability [196,197]. Current-sharing imbalances and synchronization requirements among multiple 4LIs further heighten the complexity of system coordination [198,199].

Traditionally, PI controllers combined with dual loop voltage-oriented control method have served as the mainstay for grid-connected inverter systems. While these conventional strategies perform adequately in simple, well-modeled, and relatively stable systems, they struggle under the complex and uncertain conditions typical of real-world PV parallel 4LI systems [200]. PI controllers are highly model-dependent, and their performance deteriorates when system parameters vary or nonlinearities become significant [200,201]. Their reactive nature results in slow disturbance rejection, as corrective action occurs only after performance degradation has already taken place. Fixed PI gains cannot adapt to changing operating conditions, making the system sensitive to parameter variations and limiting robustness [200,201]. Under severe disturbances such as rapid irradiance changes or sudden load variations, PI controllers often exhibit large overshoots, prolonged settling times, and even stability issues [200]. Moreover, in multi-input multi-output systems like 4LIs, PI controllers struggle to decouple interacting control loops, leading to compromised performance.

Recognizing these limitations, extensive research has been directed toward advanced control methods that can offer robustness and improved dynamic performance in complex inverter systems. Nonlinear control approaches, such as backstepping, sliding mode control (SMC), and feedback linearization, have been widely investigated. Backstepping provides systematic stability guarantees but requires precise system modeling [202,203], while SMC offers robustness to uncertainties and disturbances but suffers from chattering effects [204-206]. Feedback linearization simplifies nonlinear systems into linear equivalents but is sensitive to modeling inaccuracies [205], [207]. Predictive control methods, including model predictive control and deadbeat control, optimize control actions dynamically and achieve fast response, but they demand high computational resources and accurate models, posing challenges for real-time implementation [208-211]. Intelligent and adaptive techniques such as fuzzy logic, neural networks, and adaptive control aim to manage uncertainties and nonlinearities but often lack systematic design procedures, require extensive training data, or exhibit limited transient stability [212-214]. Robust control strategies like $H\infty$ and μ-synthesis provide guaranteed stability under bounded uncertainties but tend to be conservative and computationally demanding [215-217]. Although these methods each offer distinct advantages, their complexity,

modeling requirements, and computational demands often hinder practical implementation in industrial PV systems.

In response to these challenges, Active Disturbance Rejection Control (ADRC) has emerged as a promising paradigm offering both theoretical elegance and practical effectiveness. Originally developed by Professor Jingqing Han in the 1980s-1990s [218] and later advanced by Professor Zhiqiang Gao and others [219], ADRC represents a fundamental shift in control philosophy. Instead of relying on precise modeling and explicit compensation for every disturbance, ADRC treats all uncertainties, unmodeled dynamics, and external disturbances as a single "lumped disturbance" [133], [220]. This total disturbance is estimated in real time using an Extended State Observer (ESO) [221], actively compensated through state feedback error control loop (SFEC), and thus effectively canceled before it impacts system performance. The result is a simplified, linearized system that can be controlled with straightforward feedback mechanisms [222].

ADRC offers several key advantages that make it particularly suitable for grid-connected PV parallel 4LI systems. It requires minimal model knowledge, primarily the control input gain, making it highly robust to parameter variations [223]. By unifying all uncertainties and disturbances into a single framework, ADRC avoids the need for separate compensation mechanisms [224]. Its proactive disturbance estimation ensures superior transient performance [225,226], while continuous estimation and rejection provide strong robustness under varying operating conditions. Importantly, modern linear ADRC (LADRC) formulations are computationally efficient and suitable for real-time implementation on digital signal processors (DSPs) or field-programmable gate arrays (FPGAs) [227-229]. These attributes have led to successful ADRC applications in DC-DC converters [230,231], grid-connected inverters [232-236], active power filters [237,238], motor drives [239], and renewable energy systems [240-243]. However, its application to parallel 4LIs, especially for PV grid connected systems with their inherent nonlinearities and disturbances, remains limited. Existing studies have mostly focused on single-inverter configurations [244] and have not comprehensively addressed the unique challenges of ZSCC suppression [245,246], current-sharing under mismatches, or coordinated control among multiple inverters [247].

This research is motivated by the clear gap between ADRC’s demonstrated potential and the unmet needs of parallel 4LI systems in PV applications. Most prior works have not fully considered the four-leg inverter topology, which introduces additional challenges in neutral current and zero-sequence dynamics control. Moreover, parallel operation introduces circulating currents and synchronization issues that have yet to be systematically tackled using ADRC. The integration of ADRC with advanced modulation schemes, such as 3D-SVPWM, also remains largely unexplored. Furthermore, a comprehensive uncertainty modeling framework that encompasses DC-bus, grid-side, and grid-related disturbances is lacking, as are systematic tuning methodologies for ADRC parameters tailored to dual-loop (voltage and current) structures.

To address these gaps, this chapter develops, analyzes, and validates a complete ADRC-based control framework specifically designed for PV grid-connected parallel 4LI systems. The objectives include developing detailed uncertainty models for both DC bus voltage and pallel 4LI's output currents, designing dual-loop ADRC architectures using ESOs and SEFCs, formulating systematic parameter tuning guidelines, integrating ADRC with adjusted 3D-SVPWM for enhanced current quality and ZSCC suppression, and validating performance through comprehensive simulations under various disturbances and mismatches. Comparative analysis with conventional PI-based methods demonstrates significant improvements in voltage regulation, current control accuracy, dynamic response, and harmonic performance.

This chapter's novel contributions include the first comprehensive application of ADRC to parallel 4LI systems, the development of a unified uncertainty modeling framework, and the design of a dual-loop dq0-decomposed ADRC architecture with clear, theoretically grounded tuning procedures. Moreover, the synergistic integration of ADRC with 3D-SVPWM achieves superior ZSCC suppression and dynamic response compared to existing approaches. The findings offer not only theoretical advancement but also practical guidelines for implementing ADRC in industrial PV systems, highlighting measurable improvements in reliability, efficiency, and power quality.

The remainder of this chapter is organized as follows. Section IV.2 presents the uncertainty dynamics modeling for both DC and AC subsystems. Section IV.3 reviews state-of-the-art control strategies, positioning ADRC within this context. Section IV.4 details the design of the proposed ADRC-based dual-loop control architecture, including ESO and SEFC development and tuning methodology. Section IV.5 evaluates performance under various disturbances and parameter mismatches, while Section IV.6 provides comparative analysis with PI-based methods. Finally, Section IV.7 concludes with key insights, contributions, and directions for future research.

The significance of this work extends across academic, industrial, and societal domains. Academically, it extends ADRC theory to a complex, multi-dimensional inverter topology and provides a rigorous framework for modeling and control design. Industrially, it addresses pressing real-world challenges, offering practical design guidelines that enhance reliability and compliance with modern grid codes. More broadly, it contributes to the advancement of renewable energy integration, enabling higher PV penetration and supporting the global transition toward sustainable power systems.

In conclusion, the integration of PV systems through parallel 4LIs introduces intricate control challenges that conventional methods fail to adequately resolve. This chapter establishes ADRC as a superior control paradigm capable of fundamentally transforming system performance by actively estimating and rejecting all forms of uncertainty and disturbance. The subsequent sections present the theoretical development, design methodology, and performance validation of the proposed ADRC-based framework, demonstrating its potential to redefine the

control landscape of next-generation PV grid-connected inverter systems and advance the broader goal of sustainable energy integration.

IV.2. Uncertainty dynamics of the parallel 4LIs-based PVG grid connected system

In practical applications, the system modeling is usually established without considering the parametric uncertainties, in order to simplify the control design. However, the resulting models are not exact, and may not reflect the real system behavior under some operation conditions. Therefore, a controllers should be designed to be robust against any modeling parametric uncertainties and external disturbances.

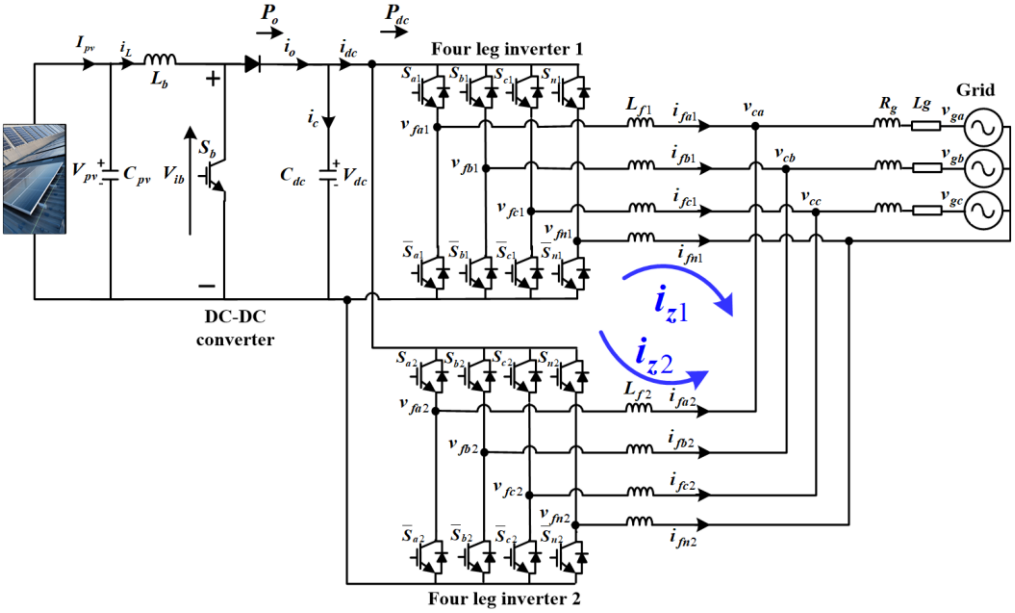


Figure. IV.1. Topologies of the PV grid connected parallel 4LI's system.

As well-known, the effectiveness of parallel 4LIs-based PVG grid connected system heavily depends on the accuracy of DC link capacitor (C_{dc}) and inverter's output filter (L_{fx}) parameters in their dynamic models. While precise parameter values are crucial for optimal performance, achieving such accuracy in practical applications is often challenging. Model discrepancies between theoretical equations and actual implementations can significantly impact system performance, particularly when substantial uncertainties are present. To enhance system performance under parallel 4LIs-based PVG grid connected system uncertainties, DC link capacitor and inverter's output filter parameters are considered with uncertainties, i.e., $C_{dc} = C_{dc0} + \Delta C_{dc}$ and $L_{fx} = L_{fx0} + \Delta L_{fx}$. The dynamic models can be further refined by incorporating external disturbances (φ_1 and φ_2) and accounting for fluctuations in the grid voltage ($\Delta v_{cd} = v_{cd} - v_{cd0}$) and the DC-DC boost converter's output current. Here, C_{dc0} and L_{fx0} denote the nominal parameter values of DC bus capacitor and output inductive filter's of the parallel 4LIs, v_{cd0} the nominal grid active voltage, and Δ indicate the parameter uncertainties and voltage fluctuations. These considerations allow for the development of a more realistic dynamic models of both the DC bus voltage and parallel 4LI's output currents

that better represents actual grid connected parallel 4LI's behavior as represented in the following subsections:

IV.2.1. Uncertainty dynamic of the DC bus voltage

The DC bus voltage dynamic is a fundamental aspect of controlling PV grid-connected parallel 4LIs, as it ensures the reliable and efficient transfer of power from the PVG to the grid via the parallel 4LIs. The DC bus voltage serves as the intermediate link between the PVG and the DC input of the parallel 4LIs, and its stability directly affects the performance and safety of the entire system. By accurately modeling the DC bus voltage dynamic, the controller can regulate the energy balance between the input (from the PVG) and the parallel 4LI's output (to the grid), preventing overvoltage or undervoltage conditions that could damage components or trigger protective shutdowns. This dynamic information is also essential for implementing MPPT, where the controller must adjust the operating point of the PVG without causing instability in the DC link. Moreover, during transient events such as load changes, irradiance fluctuations, or grid disturbances, understanding the DC bus dynamics allows the controller to maintain voltage within desired limits, ensuring continuous and smooth operation. According to (II.10) and (II.13), the dynamic model of the DC voltage in the DC side of the parallel 4LIs can be expressed as follows:

$$\frac{dV_{dc}}{dt} = \frac{1}{C_{dc}}(i_D - i_{dc}) \text{ (IV.1)}$$

This equation can be expressed by

$$\frac{dV_{dc}}{dt} = \frac{1}{C_{dc}}\left(i_D - \frac{P_{dc}}{V_{dc}}\right) \text{ (IV.1)}$$

Equation (IV.1) is the basic of degerming the 4LI's input power reference used in the determination of the 4LI's output active power reference (current), guarantying the power balance between both sides of the parallel 4LIs. Equation (IV.1) demonstrates that the dynamics of the DC-bus voltage are fundamentally influenced by the power equilibrium between the front stage (DC-DC boost converter output) and the grid active power, as well as by the grid voltage and the DC capacitor characteristics.

Firstly, when considering the uncertainties in the DC capacitor, the term $\frac{1}{C_{dc}}$ in Equation (IV.1) can by expressed by:

$$\frac{1}{C_{dc}} = \frac{1}{C_{dc0}} - \frac{\Delta C_{dc}}{C_{dc0}(C_{dc0}+\Delta C_{dc})} \text{ (IV.2)}$$

Using this, Equation (IV.2) becomes:

$$\frac{dV_{dc}}{dt} = \left(\frac{1}{C_{dc0}} - \frac{\Delta C_{dc}}{C_{dc0}(C_{dc0}+\Delta C_{dc})}\right)\left(i_D - \frac{P_{cd}}{V_{dc}}\right) + \varphi_1 \text{ (IV.3)}$$

$$\frac{dV_{dc}}{dt} = -\left(\frac{1}{C_{dc0}} - \frac{\Delta C_{dc}}{C_{dc0}(C_{dc0}+\Delta C_{dc})}\right)\left(\frac{P_{dc}}{V_{dc}}\right) - \frac{1}{C_{dc}}\left(\frac{P_{dc}}{V_{dc}}\right) + \left(\frac{1}{C_{dc0}} - \frac{\Delta C_{dc}}{C_{dc0}(C_{dc0}+\Delta C_{dc})}\right)(I_D) + \varphi_1 \text{ (IV.4)}$$

$$\frac{dV_{dc}}{dt} = -\left(\frac{1}{C_{dc0}}\frac{P_{dc}}{V_{dc}}\right) + \frac{1}{(C_{dc0}+\Delta C_{dc})}\frac{\Delta C_{dc}}{C_{dc0}V_{dc}}P_{dc} + \frac{1}{C_{dc}}(I_D) + \varphi_1 \text{ (IV.5)}$$

Although $\frac{1}{C_{dc}} = \frac{1}{(C_{dc0}+\Delta C_{dc})}$, Equation (IV.5) can be rewriting as:

$$\frac{dV_{dc}}{dt} = -\left(\frac{1}{C_{dc0}V_{dc}}P_{dc}\right) + \frac{1}{(C_{dc0}+\Delta C_{dc})}\left(\frac{\Delta C_{dc}}{C_{dc0}V_{dc}}P_{dc} + I_D\right) + \varphi_{dc} \quad \text{(IV.6)}$$

Through this disturbance consolidation approach, the uncertainty and perturbation dynamic model presented in Equation (IV.6) is transformed into their simplified forms as shown in Equation (7).

$$\frac{dV_{dc}}{dt} = b_0^v u^v + f_{dc} \quad \text{(IV.7)}$$

where $u^v = P_{dc}$ is the control input of the DC bus system and $b_0^v = \frac{1}{C_{dc0}V_{dc}}$ is its gain. f_{dc} is the total disturbance of the DC bus voltage control loop, which is expressed by:

$$f_{dc} = \frac{1}{(C_{dc0}+\Delta C_{dc})}\left(\frac{\Delta C_{dc}}{C_{dc0}V_{dc}}P_{dc} + I_D\right) + \varphi_{dc} \quad \text{(IV.8)}$$

In this, the DC bus capacitor parametric uncertainties, 4LI's input power fluctuations, disturbance in DC-DC boost converter output current, and external disturbance φ_{dc} are completely considered as a total disturbance of the DC bus voltage dynamic model and are combined as a single lumped total disturbance (f_{dc}). This total disturbance is treated in the proposed ADRC method used in the DC bus voltage control loop.

IV.2.2. Uncertainty dynamics of parallel 4Lis output currents in the dq0 reference frame

In PV grid-connected parallel 4LIs, the output current dynamics are as critical as the DC bus voltage dynamics, particularly when the grid is supplying linear inductive loads. Under such conditions, the output currents dictate the instantaneous real and reactive power exchange with the grid, directly influencing both the energy balance on the DC side and the regulation of the DC bus voltage. A fast and precise current dynamic response ensures that the inverters can supply the necessary reactive current demanded by the inductive load while maintaining the desired power factor and complying with grid codes in terms of power factor, harmonic distortion, and synchronization. In a parallel configuration, accurate control of current dynamics also guarantees proper load sharing among the inverters and minimizes circulating currents. Furthermore, the independent control of each output current components in the dq0 reference frame, enabling effective compensation for any residual unbalance and ensuring smooth grid current waveforms. During transient events such as step changes in load or fluctuations in PV generation, well-managed output current dynamics help prevent oscillations in the DC link, sustain voltage stability, and maintain efficient, reliable, and high-quality power delivery from the PVG to the grid.

According to Equation (II.12), the dynamic models of the output currents of each 4LI can be expressed as follows:

$$\begin{cases} \frac{di_{fd1}}{dt} = \frac{v_{fd1}}{L_{f1}} - \frac{v_{cd}}{L_{f1}} + \omega i_{fq1} \\ \frac{di_{fq1}}{dt} = \frac{v_{fq1}}{L_{f1}} - \frac{v_{cq}}{L_{f1}} - \omega i_{fd1} \\ \frac{di_{f01}}{dt} = \frac{v_{f01}}{4L_{f1}} \end{cases} \quad \text{(IV.9)}$$

$$\begin{cases} \frac{di_{fd2}}{dt} = \frac{v_{fd2}}{L_{f2}} - \frac{v_{cd}}{L_{f2}} + \omega i_{fq2} \\ \frac{di_{fq2}}{dt} = \frac{v_{fq2}}{L_{f2}} - \frac{v_{cq}}{L_{f2}} - \omega i_{fd2} \\ \frac{di_{f02}}{dt} = \frac{v_{f02}}{4L_{f2}} \end{cases}$$

(IV.10)

In this context, each 4LI output inductive filter parameter L_{fx} is fully considered with uncertainties $L_{fx} = L_{fx0} + \Delta L_{fx}$, external disturbances φ_2, and accounting for fluctuations in the grid voltage ($v_{cd} = v_{cd0} + \Delta v_{cd}$), as well as the coupling terms ωi_{fqx} and ωi_{fdx} and included into the output current dynamic's model such that the control robustness is guaranteed. According to these, the output current dynamics in Equations (IV.9) and (IV.10) become:

$$\begin{cases} \frac{di_{fdx}}{dt} = \frac{1}{L_{fx}}\left(v_{fdx} - v_{cd0} + \Delta v_{cd} + L_{fx}\omega i_{fqx}\right) + \varphi_{2dx} \\ \frac{di_{fqx}}{dt} = \frac{1}{L_{fx}}\left(v_{fqx} - v_{cq0} + \Delta v_{cq} - L_{fx}\omega i_{fdx}\right) + \varphi_{2qx} \\ \frac{di_{f0x}}{dt} = \frac{1}{4L_{fx}} v_{f0x} + \varphi_{20x} \end{cases} \quad \text{(IV.11)}$$

In this case, the term $\frac{1}{L_{fx}}$ in system Equation (IV.11) can by expressed by:

$$\frac{1}{L_{fx}} = \frac{1}{L_{fx0}} - \frac{\Delta L_{fx}}{L_{fx0}\left(L_{fx0}+\Delta L_{fx}\right)} \text{ (IV.12)}$$

Using this equality, the dynamics of the output currents in Equation (IV.12), becomes:

$$\begin{cases} \frac{di_{fdx}}{dt} = \left(\frac{1}{L_{fx0}} - \frac{\Delta L_{fx}}{L_{fx0}\left(L_{fx0}+\Delta L_{fx}\right)}\right)\left(v_{fdx} - v_{cd0} + \Delta v_{cd} + L_{fx}\omega i_{fqx}\right) + \varphi_{idx} \\ \frac{di_{fqx}}{dt} = \left(\frac{1}{L_{fx0}} - \frac{\Delta L_{fx}}{L_{fx0}\left(L_{fx0}+\Delta L_{fx}\right)}\right)\left(v_{fqx} - v_{cq0} + \Delta v_{cq} - L_{fx}\omega i_{fdx}\right) + \varphi_{iqx} \\ \frac{di_{f0x}}{dt} = \left(\frac{1}{4L_{fx0}} - \frac{\Delta L_{fx}}{4L_{fx0}\left(L_{fx0}+\Delta L_{fx}\right)}\right) v_{f0x} + \varphi_{i0x} \end{cases} \quad \text{(IV.13)}$$

$$\begin{cases} \frac{di_{fdx}}{dt} = \frac{1}{L_{fx0}} v_{fdx} - \frac{\Delta L_{fx}}{L_{fx0}\left(L_{fx0}+\Delta L_{fx}\right)} v_{fdx} + \frac{1}{L_{fx}}\left(-v_{cd0} + \Delta v_{cd} + \omega i_{fqx}\right) + \varphi_{idx} \\ \frac{di_{fqx}}{dt} = \frac{1}{L_{fx0}} v_{fqx} - \frac{\Delta L_{fx}}{L_{fx0}\left(L_{fx0}+\Delta L_{fx}\right)} v_{fqx} + \frac{1}{L_{fx}}\left(-v_{cq0} + \Delta v_{cq} - \omega i_{fdx}\right) + \varphi_{iqx} \\ \frac{di_{f0x}}{dt} = \frac{1}{4L_{fx0}} v_{f0x} - \frac{\Delta L_{fx}}{4L_{fx0}\left(L_{fx0}+\Delta L_{fx}\right)} v_{f0x} + \varphi_{i0x} \end{cases} \quad \text{(IV.14)}$$

Through this disturbance consolidation approach, the uncertainty and perturbation output current dynamics presented in Equation (IV.14) are transformed into their simplified forms as shown in Equation (IV.15).

$$\frac{di_{fdq0x}}{dt} = b_{0i}^{dq0} u_{ix}^{dq0} + f_{ix}^{dq0} \text{(IV.15)}$$

where u_{ix}^{dq0} are the control inputs of the output current's system, and $b_{0i}^{dq} = \frac{1}{L_{fx0}}$ and $b_{0i}^{0} = \frac{1}{4L_{fx0}}$ are their gains. f_{ix}^{d}, f_{ix}^{q}, and f_{ix}^{0} are respectively the total disturbances of the dq0 output current control loops, which are expressed by:

$$\begin{cases} f_{ix}^{d} = -\frac{\Delta L_{fx}}{L_{fx0}\left(L_{fx0}+\Delta L_{fx}\right)} v_{fdx} + \frac{1}{L_{fx}}\left(-v_{cd0} + \Delta v_{cd} + \omega i_{fqx}\right) + \varphi_{2dx} \\ f_{ix}^{q} = -\frac{\Delta L_{fx}}{L_{fx0}\left(L_{fx0}+\Delta L_{fx}\right)} v_{fqx} + \frac{1}{L_{fx}}\left(-v_{cq0} + \Delta v_{cq} - \omega i_{fdx}\right) + \varphi_{2qx} \\ f_{ix}^{0} = -\frac{\Delta L_{fx}}{4L_{fx0}\left(L_{fx0}+\Delta L_{fx}\right)} v_{f0x} + \varphi_{20x} \end{cases} \quad \text{(IV.16)}$$

In this, the output inductive filter parametric uncertainties, grid voltage fluctuations, coupling terms, and external disturbance φ_{idq0} are completely considered as a total disturbance in each output current dynamic model and in each dynamic model the total disturbance is combined as a single lumped total disturbance (f_{ix}^{d}, f_{ix}^{q}, or f_{ix}^{0}). Each of these total disturbances is treated in the proposed ADRC method used in its corresponding output current control loop.

IV.4. Design of the ADRC method-based grid connected parallel 4LIs

IV.4.1. Design of the ADRC method-based outer DC bus voltage control loop

In this section, an ADRC method-based outer DC bus voltage control loop is designed to regulate DC bus voltage of the PV grid connected parallel 4LIs. This regulation aims to maintain DC bus voltage stability within acceptable limits despite variations in PV generation and load demand, enhance disturbance rejection capabilities under the change of loads, achieve power balance between PV system, grid, and load, improve power quality by optimizing voltage fluctuations and transients, enhance steady-state performance, and increase robustness against DC bus capacitor parameter variations. The proposed ADRC method-based outer DC bus voltage control loop aims also to provides the appropriate active current reference for the inner parallel 4LIs output current control loop to generate optimal control signals of the parallel 4LIs, ensures system reliability, prevents damage to connected loads, and facilitates smooth integration of the PV.

The proposed outer ADRC loop (Figure IV. 2) has two stages: disturbance observation using ESO, and regulation of estimated DC bus voltage via SEFC. ESO-estimated disturbance is added to initial SFEC output (u_{0v}) to obtain final control law (u_v) that determine the inner active output current reference (i_{fd}^{*}). The objective is to controlling V_{dc} through the control inputs u_v.

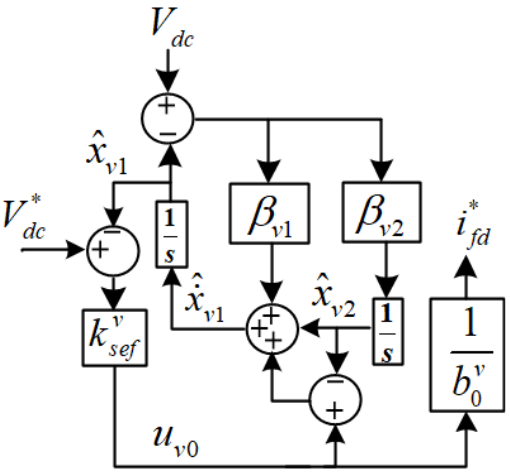


Figure IV. 2: Schematic diagram of the ADRC method-based outer DC bus voltage control loop.

IV.4.1.1. Design of the ESO-based outer DC bus voltage control loop

The uncertain DC bus voltage dynamics model given in Equation (IV.7) is converted into an integral chain form, as follows:

$$\begin{cases} x_{v1} = V_{dc} \\ \dot{x}_{v1} = b_0^v u^v + f_{dc} \\ x_{v2} = f_{dc} \\ \dot{x}_{v2} = h_v \\ y_v = x_{v1} \end{cases} \quad \text{(IV.17)}$$

The ESO-based ADRC method adopted in the outer DC bus voltage control loop to estimate its disturbance is design as follows:

The outer DC bus voltage control loop process begins with measuring V_{dc} using voltage sensor. Then, based on the perturbed DC bus voltage dynamic model in Equation (IV.17), the internal state variable $x_{v1} = V_{dc}$ is assessed using ESO. The extended state variable $x_{v2} = f_{dc}$ represents the LTD. The objective is to control V_{dc} through the control input $u_v = P_{dc}^{*}$, where its gain b_0^v is determined based on the nominal parameter value of the DC bus capacitor.

According to Equation (IV.17), $\hat{x}_{v1} = \hat{V}_{dc}$ is taken as the first state variable and $\hat{x}_{v2} = \hat{f}_{dc}$ as the second state variable. To estimate x_{v1} and x_{v2}, an ESO is constructed based on Equation (IV.18) as [248]:

$$\begin{cases} \dot{\hat{x}}_{v1} = \hat{x}_{v2} + b_0^v u^v + \beta_{v1}(x_{v1} - \hat{x}_{v1}) \\ \dot{\hat{x}}_{v2} = \beta_{v2}(x_{v1} - \hat{x}_{v1}) \end{cases} \quad \text{(IV.18)}$$

where $e_{v1} = x_{v1} - \hat{x}_{v1}$ and $e_{v2} = x_{v2} - \hat{x}_{v2}$ are the errors of state estimation and disturbance estimation, respectively.

It is clear from this equation that the bandwidth ω_{eso} is the main parameter that needs to be chosen in order to improve performance and ensure the suggested ESO operates effectively. This bandwidth is selected between 1 and 5 times of the **SEFC-based outer DC bus voltage control loop's** bandwidth ($\omega_{0eso} = 1{\sim}15\ \omega_{0dc}$) to guarantee the fast tracking of the estimated state dynamics under any change in the real state dynamics [248-250]. Also, the bandwidth of

the ESO cannot be chosen very large to avoid degrading its immunity against noise and not impacting the performance of the grid current controllers [249, 250].

IV.4.1.2. Design of the SEFC-based outer DC bus voltage control loop

Based on ADRC principles, the observed LTD in the DC bus voltage model ($\hat{x}_{v2} = \hat{f}_{dc}$) can be utilized as feedforward compensation term. This term complements the initial control input u_{v0}, which is derived from the ESFC-based ADRC method. This approach enables the reformulation of the final control law $u_v = P_{dc}^*$ of the outer DC bus voltage control loop, as follows:

The final control law $u_v = P_{dc}^*$ is given by [133]:

$$u_v = P_{dc}^* = \frac{u_{v0} - \hat{f}_{dc}}{b_0^v} \text{ (IV.19)}$$

where u_{v0} is the initial control input, which determined using the regulation of the estimated DC bus voltage with its reference using proportional controller as follows:

$$u_{v0} = k_{sef}^v (V_{dc}^* - \hat{x}_{v1}) \text{ (IV.20)}$$

where k_{sef}^v is the gain of the proportional controller [249].

IV.4.2. Design of the ADRC method-based inner output current control loop

In this section, as shown in Figure IV.3, an ADRC-based inner current control loop is designed for the parallel 4LIs to regulate the output currents and accurately track their references. The objective of this control loop is to achieve fast dynamic response under sudden load and generation variations, suppress output current harmonics, ensure balanced three-phase and neutral current sharing among the parallel inverters, and enables the inverters to supply reactive power demanded by inductive loads, thereby reducing the burden on the grid and improving overall power factor. By improving disturbance rejection and dynamic response under load and generation variations, the controller enhances grid-injected current quality and minimizes THD. Moreover, the proposed ADRC-based current control loop strengthens robustness against parameter uncertainties in the parallel 4LIs and filter elements, ensures stable operation under varying operating conditions, and generates precise control signals to drive the switching devices of the parallel 4LIs.

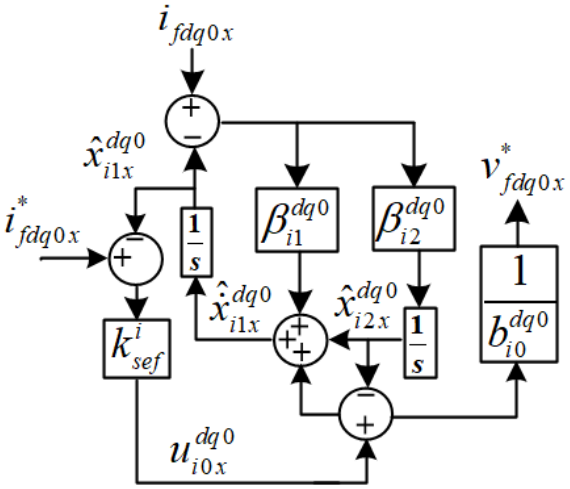


Figure IV.3: Schematic diagram of the ADRC method-based inner output current control loop.

The proposed inner ADRC loop (Figure IV.3) has also two stages: output current disturbance observations of each 4LI using the ESOs in the dq0 reference frame and regulation of estimated output currents $\hat{\imath}_{fdq0x}$ via three SEFCs. As in the ADRC-based outer DC bus voltage control loop, each estimated output current disturbance in the dq0 ($\hat{f}_{ix}^{d}$, $\hat{f}_{ix}^{q}$, or $\hat{f}_{ix}^{0}$) is added to its corresponding initial SFEC output (u_{0ix}^{d}, u_{0ix}^{q}, or u_{0ix}^{0}) to obtain final control laws of the inner output currents control loop (u_{ix}^{dq0}) that determine each 4LI output voltage references (v_{fdq0x}^{*}). The objective is to controlling the output currents of each 4LI i_{fdq0x} through the corresponding control input $u_{ix}^{dq0} = v_{fdq0x}^{*}$.

IV.4.2.1. Design of the ESOs-based inner output current control loop in the dq0 reference frame

The uncertain output current dynamics model given in Equation (IV.16) is converted into an integral chain form, as follows:

$$\begin{cases} x_{i1x}^{dq0} = i_{fdq0x} \\ \dot{x}_{i1x}^{dq0} = b_{0i}^{dq0} u_{ix}^{dq0} + f_{ix}^{dq0} \\ x_{i2x}^{dq0} = f_{ix}^{dq0} \\ \dot{x}_{i2x}^{dq0} = h_{i}^{dq0} \\ y_{ix}^{dq0} = x_{i1x}^{dq0} \end{cases} \quad \text{(IV.21)}$$

In this section, each ESO-based ADRC method adopted in the inner output current control loop to estimate its disturbance is design as follows:

The inner output current control loop for each 4LI process begins with measuring the output currents of each 4LI (i_{fdq0x}) using three current sensors. Then, these three phase currents are transformed into the dq0 reference frame and based on the perturbed output current dynamics model in Equation (IV.21), the internal state variables $x_{i1x}^{dq0} = i_{fdq0x}$ are assessed using the three ESOs. The extended state variables $x_{i2x}^{dq0} = f_{ix}^{dq0}$ represent the LTDs of the grid current system in the dq0 reference frame. The objective is to control the output currents of each 4LI in the dq0 reference frame i_{fdq0x} through their corresponding control inputs $u_{ix}^{dq0} = v_{fdq0x}^{*}$, where their gain b_{0i}^{dq0} are determined based on the nominal parameter value of the inverter output filter inductance.

According to Equation (IV.21), $\hat{x}_{i1x}^{dq0} = \hat{\imath}_{fdq0x}$ are taken as the estimated first state variables of the three ESOs and $\hat{x}_{i2x}^{dq0} = \hat{f}_{ix}^{dq0}$ as the estimated second state variables. To estimate $\hat{x}_{i1x}^{dq0}$ and $\hat{x}_{i2x}^{dq0}$, three ESOs are constructed in the dq0 reference frame based on Equation (IV.21) as [237]:

$$\begin{cases} \dot{\hat{x}}_{i1x}^{dq0} = \hat{x}_{i2x}^{dq0} + b_{0i}^{dq0} u_{ix}^{dq0} + \beta_{i1}^{dq0} \left(x_{i1x}^{dq0} - \hat{x}_{i1x}^{dq0} \right) \\ \dot{\hat{x}}_{i2x}^{dq0} = \beta_{i2}^{dq0} \left(x_{i1x}^{dq0} - \hat{x}_{i1x}^{dq0} \right) \end{cases} \quad \text{(IV.22)}$$

where $e_{i1x}^{dq0} = x_{i1x}^{dq0} - \hat{x}_{i1x}^{dq0}$ and $e_{i2x}^{dq0} = x_{i2x}^{dq0} - \hat{x}_{i2x}^{dq0}$ are the errors of state estimation and disturbance estimation, respectively.

IV.4.2.2. Design of the SEFC-based inner output current control loop

In this control loop, the observed LTD in the parallel 4LIs output current models ($\hat{x}_{i2x}^{dq0} = \hat{f}_{ix}^{dq0}$) can be utilized as feedforward compensation terms they complement the initial control inputs u_{i0x}^{dq0}, which are derived from the three ESFC-based ADRC methods. This approach enables the reformulation of the final control laws $u_{ix}^{dq0} = v_{fdq0x}^{*}$ of the inner parallel 4LIs output current control loop, as follows:

The three final control laws that represent the output voltage references of each 4LI in the dq0 reference frame are given by [251]:

$$u_{ix}^{dq0} = v_{fdq0x}^{*} = \frac{u_{i0x}^{dq0} - \hat{f}_{ix}^{dq0}}{b_{0i}^{dq0}} \text{(IV.23)}$$

The initial control inputs u_{i0x}^{dq0} are determined using the regulation of the estimated output currents with their references using three proportional controllers in the dq0 reference frame as follows:

$$u_{i0x}^{dq0} = k_{sef}^{i}\left(i_{fdq0x}^{*} - \hat{\imath}_{fdq0x}\right) \text{(IV.24)}$$

where $k_{sef}^{i} = \omega_{0i}^{2}$ is the gain of the three proportional controllers.

IV.4.3. Parameter tuning and performance analysis of the proposed ADRC method

Proper tuning of the proposed ADRC method system is essential in both control loops for effective control of the DC bus voltage and parallel 4LI's output currents. Correct parameter settings enhance system performance by improving voltage and current quality, ensuring system stability, and providing strong disturbance rejection and robustness to uncertainties. This section outlines a systematic method for tuning the ADRC method parameters in both inner and outer control loops to meet desired performance criteria such as disturbance rejection ability, fast response, robustness, and steady-state accuracy. So, in this study the Hurwitz stability criteria is applied to establish the initial ADRC parameters of both control loops as in the following:

According to Equations (IV.17) and (IV.18), the error dynamics of the ESO-based outer DC bus voltage control loop can be expressed as:

$$\begin{bmatrix}\dot{e}_{v1}\\ \dot{e}_{v2}\end{bmatrix} = -\underbrace{\begin{bmatrix}\beta_{v1} & -1\\ \beta_{v2} & 0\end{bmatrix}}_{A_v}\begin{bmatrix}e_{v1}\\ e_{v2}\end{bmatrix} + \begin{bmatrix}0\\ 1\end{bmatrix}h_v \text{(IV.25)}$$

The characteristic polynomial of A_v can be expressed as:

$$P_{A_v}(s) = s^2 + \beta_{v1}s + \beta_{v2} \text{ (IV.26)}$$

The characteristic polynomial of a stable second order closed loop system $P_{A_v}(s)$ is expressed as:

$$P_{A_v}(s) = s^2 + 2\xi_{eso}\omega_{0eso}s + \omega_{0eso}^2 \text{(IV.27)}$$

where ζ_{eso} and ω_{eso} are the damping factor and bandwidth of the ESO, respectively. To

guarantee that the polynomial (IV.27) is Hurwitz stable [249, 250], β_{v1} and β_{v2} are calculated according to the pole placement technique by identifying Equations (IV.26) and (IV.27), which results in [252-254]:

$$\begin{cases}\beta_{v1} = 2\xi_{elso}\omega_{0eso} \\ \beta_{v2} = \omega_{0eso}^2\end{cases} \text{(IV.28)}$$

The gain of the SEFC-based ADRC method of the outer control loop k_{sef}^{v} is selected as a trade-off between steady state performance and dynamic responses as a function of the proportional controller bandwidth $\omega_{c,sef}^{v}$ by [252-254]:

$$k_{sef}^{v} = \left(\omega_{c,sef}^{v}\right)^2 \text{(IV.29)}$$

where, $\omega_{c,sef}^{v}$ is the bandwidth of SEFL-based ADRC method used in the outer voltage control loop [197].

As in the ADRC method-based outer DC bus control loop (3.2.1), in this control loop we applies the Hurwitz stability criteria to establish the initial ESO's parameters β_{i1}^{dq0} and β_{i2}^{dq0} as follows:

According to Equations (IV.25) and (IV.26), the ESO error dynamics can be expressed as:

$$\begin{bmatrix}\dot{e}_{i1x}^{dq0} \\ \dot{e}_{i2x}^{dq0}\end{bmatrix} = -\underbrace{\begin{bmatrix}\beta_{i1}^{dq0} & -1 \\ \beta_{i2}^{dq0} & 0\end{bmatrix}}_{A_i}\begin{bmatrix}e_{i1x}^{dq0} \\ e_{i2x}^{dq0}\end{bmatrix} + \begin{bmatrix}0 \\ 1\end{bmatrix} h_i^{dq0} \text{(IV.30)}$$

The characteristic polynomial of A_i can be expressed as:

$$P_{Ai}(s) = s^2 + \beta_{i1}^{dq0}s + \beta_{i2}^{dq0}. \text{(IV.31)}$$

The characteristic polynomial of a stable second order closed loop system *P(s)* is expressed as:

$$P_{Ai}(s) = s^2 + 2\xi_{esoi}\omega_{0esoi}s + \omega_{0esoi}^2 \text{(IV.32)}$$

where ζ_{esoi} and ω_{esoi} are the damping factor and bandwidth of the three ESOs-based inner current control loop of each 4LI, respectively. To guarantee that the polynomial (IV.31) is Hurwitz stable [248], [251], β_{i1}^{dq0} and β_{i2}^{dq0} are calculated by identifying Equations (IV.31) and (IV.32), which results in:

$$\begin{cases}\beta_{i1}^{dq0} = 2\xi_{elsoi}\omega_{0esoi} \\ \beta_{i2}^{dq0} = \omega_{0esoi}^2\end{cases} \text{(IV.33)}$$

It is clear from this equation that the bandwidths ω_{0esoi} is the main parameter that needs to be chosen in order to improve performance and ensure the suggested ADRC operates effectively in both control loops.

This bandwidth is selected between 1 and 5 times of the DC-link voltage regulator's bandwidth ($\omega_{0esoi} = 1\sim15\ \omega_{c,sef}^{i}$) to guarantee the fast tracking of the estimated state dynamics under any change in the real state dynamics [248-252]. Also, the bandwidth of the

ESO cannot be chosen very large to avoid degrading its immunity against noise and not impacting the performance of the grid current controllers [250], [252].

In dual cascade control loop structure used in the control of DC bus voltage and output currents of the parallel 4LIs, the bandwidth of the SEFC-based ADRC method used in the inner output current control loop $\omega_{c,sef}^{i}$ is typically set between one-fifth and one-tenth of the 4LI's switching frequency $\omega_{sw} = 2\pi f_{sw}$ [254-256], while the bandwidth of SEFL-based ADRC method used in the outer voltage control loop ($\omega_{c,sef}^{v}$) should be lower than $\omega_{c,sef}^{i}$, typically $\omega_{c,sef}^{v} \approx 1/5$ to $1/10$ of $\omega_{c,sef}^{i}$. This ensures that the inner output current control loop responds faster than the outer DC bus voltage control loop, avoiding unwanted interactions between the two control loops [257].

Additionally, for each control loop, the bandwidth of the ESO, ω_{eso}^{v} or ω_{eso}^{i}, should be about 3 to 5 times higher than the bandwidth of its corresponding SEFL $\omega_{c,sef}^{v}$ or $\omega_{c,sef}^{i}$, so that the ESO is each control loop can estimate disturbances quickly and accurately [258]. However, setting the ESO bandwidth too high in each control loop can increase sensitivity to noise and degrade overall controller performance [259-261]. Therefore, in each control loop, ESO bandwidths must be carefully selected to balance between estimation speed and noise sensitivity. So, the ESO bandwidths ω_{eso}^{v} and ω_{eso}^{i} must be adjusted to achieve acceptable transient behavior of both ESOs in terms of both the disturbance rejection ability and estimation error dynamics.

IV.5. ADRC method for PV grid connected parallel 4LIs-based reactive power compensation

In this section, the simulation results of the PV grid connected parallel 4LIs system connected in parallel with a three-phase four-wire grid supplying three phase linear inductive loads are presented. The study considers two cases: differences in the output filter inductances and differences in output current sharing under varying conditions. The control strategy is implemented using the proposed ADRC method in both the outer and inner control loops, while the ZSCC between the parallel 4LIs is controlled and eliminated using the proposed adjusted 3DSVPWM. Figure IV.4 shows the block diagram of the PV grid connected parallel 4LIs system controlled using the proposed ADRC method and adjusted 3DSVPWM.

The overall control structure of the PV grid connected parallel 4LI's system controlled using ADRC method with adjusted 3D SVPWM is illustrated in Figure III.11.

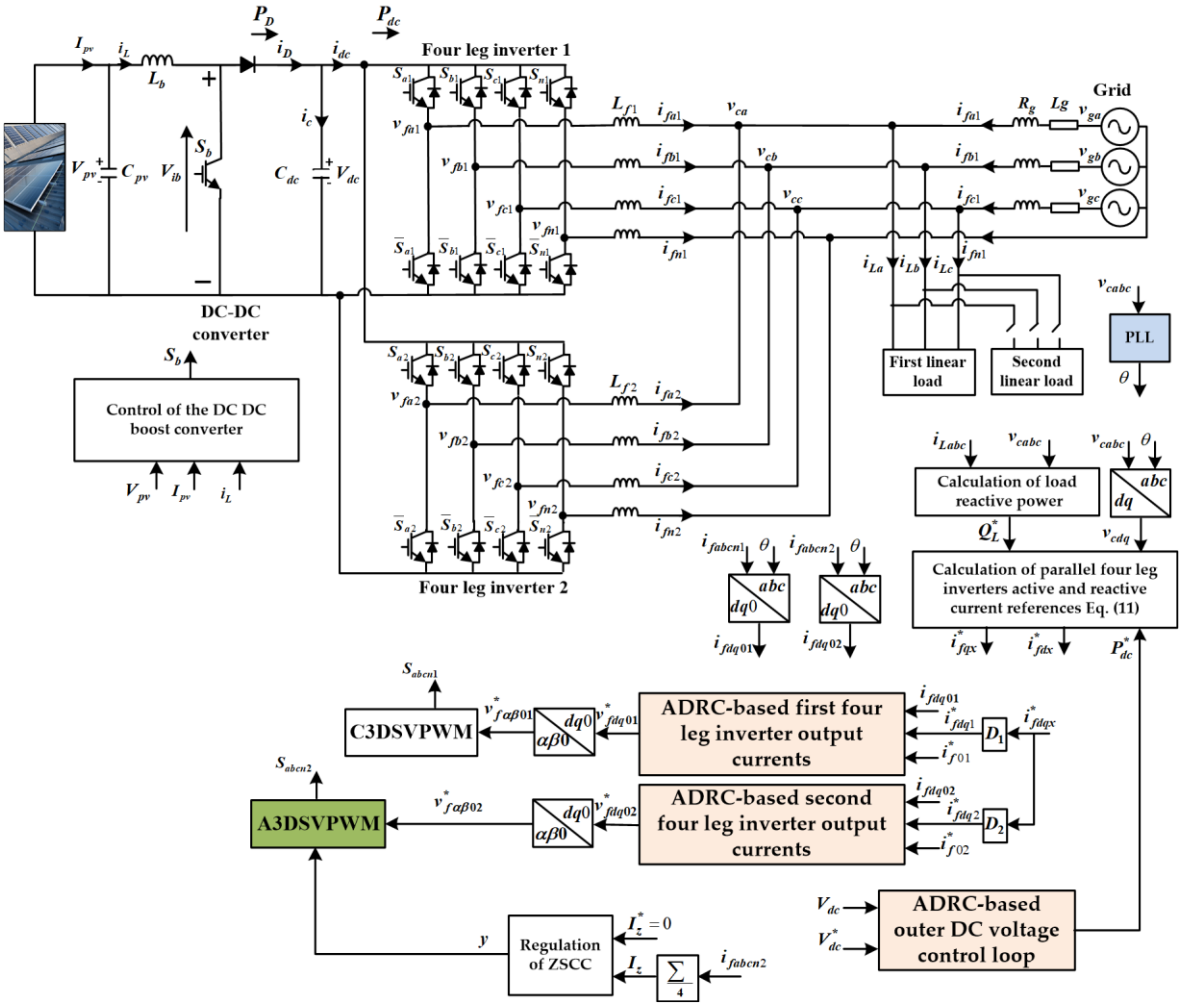


Figure. IV.4: The overall control structure of the PV grid connected parallel 4LI's system controlled using ADRC method with adjusted 3D SVPWM

In this case, the system with the ADRC methods and ZSCC suppression method shown in Figure (IV.4) is simulated using the parameters given in Table (A.2). To demonstrate the influence of the ADRC method on the system's performance in terms of DC link and grid current regulations, disturbance rejections, and power compensation quality, as well as the effectiveness of the proposed ZSCC suppression method, a difference in the 4LI output filter inductance values is introduced. The results of this test are shown in Figures IV.5 and IV.6.

Figures IV.5a show the system active powers, including the grid active power, the load active power, and the parallel 4LIs output active power. It can be seen from this figure that the system active power dynamics under ADRC control demonstrate exceptional stability and precise tracking capabilities throughout all operating phases. During the initial steady-state operation ($0 \leq t \leq 0.5$ s), the system establishes a well-balanced power flow with P_{load} stabilizing at approximately 17 kW and P_PV at around 12 kW. The ADRC-controlled parallel 4LIs inject the entire PV-generated power ($P_{inverters} \approx 12$ kW) with remarkable precision, while the grid seamlessly supplies the remaining 5 kW deficit. What distinguishes the ADRC

approach from the conventional PI control in Chapter 3 (Figure III.19a) is the virtually instantaneous response to disturbances with minimal overshoot or oscillations.

When solar irradiance decreases during the second phase ($0.5 \leq t \leq 0.75$ s), reducing PV output to approximately 7 kW, the ADRC controller exhibits superior transient performance. The transition is exceptionally smooth, with the grid power increasing proportionally to maintain constant load supply without any visible power fluctuations or temporary imbalances that were present in the PI-based approach (Figure III.19a). The ADRC's ESO effectively estimates and compensates for the disturbance caused by the irradiance drop, resulting in a near-ideal power flow adjustment.

Additionally, during the subsequent irradiance increases in the third ($0.75 \leq t \leq 1$ s) and fourth phases ($1 \leq t \leq 1.25$ s), where PV power rises to 9 kW and 12 kW respectively, the ADRC demonstrates its remarkable disturbance rejection capability. The power transitions are executed with surgical precision, showing significantly reduced settling times and virtually eliminated overshoot compared to the conventional PI control presented in Chapter 3 (Figure III.19a). This superior performance stems from the ADRC's ability to treat PV generation fluctuations as lumped disturbances and actively compensate for them in real-time.

The most dramatic validation of ADRC superiority occurs at t = 1.25 s during the sudden load change from 8 Ω to 4 Ω (and 8 mH to 4 mH). The load power demand surges to approximately 32 kW, requiring grid power to increase to about 21 kW. Under ADRC control, this severe disturbance is handled with exceptional robustness and the power flow stabilizes within milliseconds with minimal transient oscillations. The $P_{inverters}$ maintains around 11 kW, slightly lower than P_{PV}, demonstrating the system's intelligent allocation of parallel 4LIs system capacity between active power injection and reactive power compensation. Unlike the PI-based control (Figure III.19a) which showed noticeable oscillations during similar transitions, the ADRC maintains smooth power flow throughout this challenging scenario.

The three-phase grid currents (i_{gabc}) in Figure IV.6b show that the ADRC control exhibit outstanding quality characteristics and surpass conventional PI control performance. During stable operation, the grid currents maintain perfectly balanced amplitudes with exceptional sinusoidal purity. The ADRC's SEFC combined with ESO-based disturbance compensation ensures that the harmonic distortions are minimized to levels significantly below those achieved using PI controllers in Chapter 3 (Figure III.19b).

When irradiance drops at t = 0.5 s, the grid current amplitude adjusts smoothly and proportionally without the transient ripples or overshoots visible in PI-controlled systems (Figure III.19b). The ADRC's fast disturbance estimation and compensation mechanism ensures that the current tracking remains accurate even during rapid power variations. The subsequent irradiance increases at t = 0.75 s and t = 1.0 s demonstrate the controller's exceptional dynamic response, with current amplitudes increasing smoothly while maintaining perfect phase balance and waveform quality.

At t = 1.25 s, when the load changes dramatically, there is a significant step increase in grid current amplitude to accommodate the doubled load demand. Remarkably, the ADRC maintains perfect grid current quality during this severe transient and the three phases remain perfectly balanced, sinusoidal waveforms are preserved, and there are no visible distortions or oscillations. This represents a substantial improvement over the PI-based approach, which exhibited noticeable grid current distortions and longer settling times during similar load steps. The ADRC's ability to estimate and compensate for coupling effects, PV voltage fluctuations, and load changes as lumped disturbances results in superior current quality under all operating conditions.

The reactive power management (Figure IV.5c) under ADRC control demonstrates exceptional precision and robustness. Throughout the first four operating phases with varying irradiance ($0 \leq t \leq 1.25$ s), the parallel 4LIs compensate for the entire reactive power demand of the load while maintaining Q_{grid} remarkably close to zero. This near-perfect unity power factor operation at the grid connection point is maintained with significantly tighter regulation compared to the PI-based control in Chapter 3 (Figure III.19c), which showed slight fluctuations in Q_{grid} during transients.

The ADRC's superior performance is particularly evident during irradiance variations. While PI control showed $Q_{inverters}$ fluctuations during PV power changes, the ADRC maintains stable reactive power compensation independent of active power variations. This decoupling is achieved through the ADRC's ability to handle cross-coupling between d-axis and q-axis dynamics as part of the lumped disturbance, which is actively estimated and compensated by the ESO-based inner parallel 4LIs output current control loop.

Additionally, when the load changes at t = 1.25 s, there is a dramatic jump in both Q_{load} and $Q_{inverters}$ from approximately 7 kVAr to around 14 kVAr. The ADRC-based based inner parallel 4LIs output current control loop responds to this severe disturbance with remarkable agility, the parallel 4LIs instantaneously adjust their reactive power output to fully compensate for the new load demand, maintaining Q_{grid} at virtually zero throughout the transition. The absence of overshoot, oscillations, or steady-state error during this challenging step change represents a significant advancement over conventional PI control method. The ADRC's feedforward compensation of estimated disturbances enables this near-ideal response, ensuring excellent power factor control even under severe load variations.

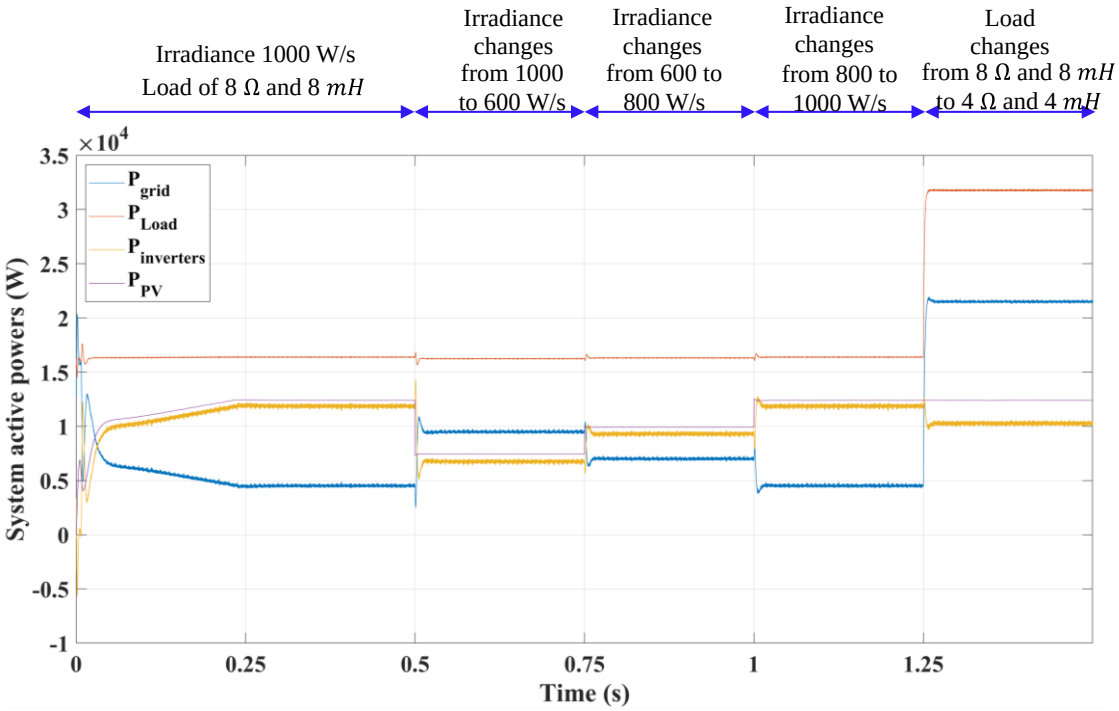
The voltage-current phase relationship shown in Figure IV.5d provides compelling evidence of the ADRC's superior reactive power compensation and power factor control capability. Throughout all operating conditions, the first-phase grid current (i_{ga}) maintains perfect phase alignment with the grid voltage (v_{ga}), confirming totally reactive power compensation and unity power factor operation. The sinusoidal purity of the grid current is exceptional, with no visible distortions even during the severe transients at t = 0.5 s, 0.75 s, 1.0 s, and 1.25 s.

Comparing with the PI-based control results in Chapter 3 (Figure III.19d), the ADRC demonstrates noticeably cleaner grid current waveforms with reduced harmonic content. During

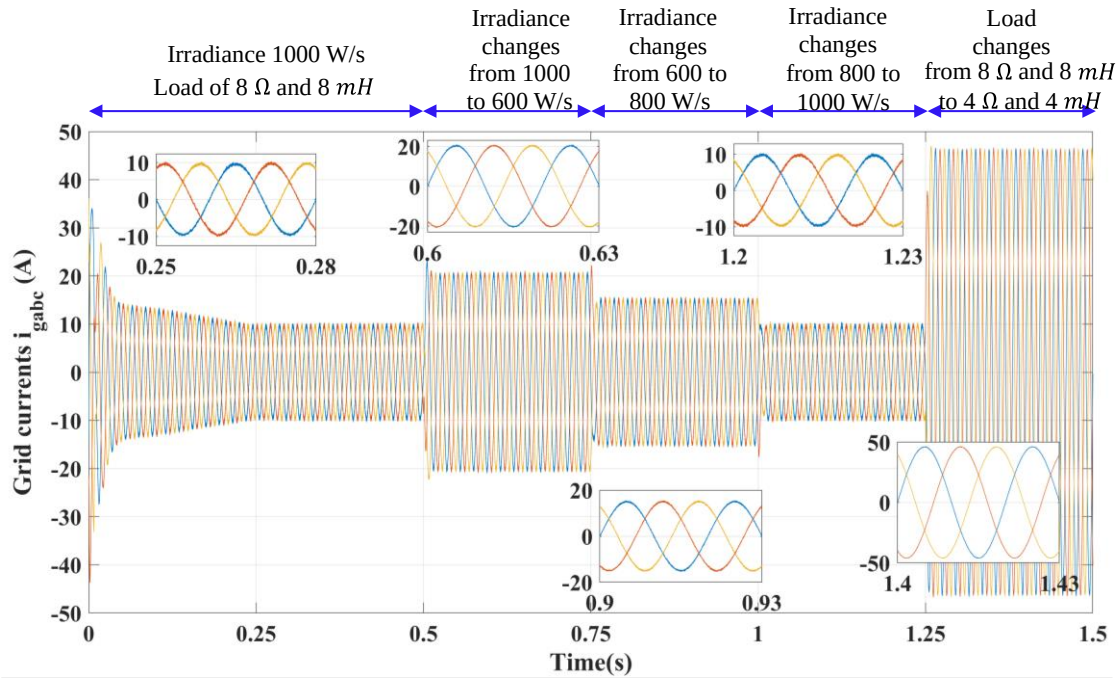
the load change at t = 1.25 s, while the grid current amplitude increases substantially to meet the higher load demand, the ADRC maintains impeccable phase synchronization and waveform quality. There are no phase shifts, no transient overshoots, and no distortions, characteristics that were partially present in the conventional PI approach. This superior performance directly translates to improved grid code compliance, reduced harmonic pollution, and enhanced overall power quality delivered to the grid.

The DC bus voltage regulation under ADRC control (Figure IV.5e) represents perhaps the most significant advancement over conventional PI controller. Throughout the entire test scenario, the DC bus voltage tracks its reference with exceptional precision, exhibiting substantially reduced fluctuations compared to the PI-based control in Chapter 3 (Figure III.19e). During steady-state operation, the voltage ripple is minimized to levels near the theoretical limit imposed by the switching frequency. When the irradiance changes occur at t = 0.5 s (decrease), t = 0.75 s (increase), and t = 1.0 s (increase), the ADRC-based outer DC bus voltage control loop demonstrates its superior disturbance rejection capability. Each irradiance variation causes a temporary power imbalance between the PV source and the load, which directly impacts the DC bus. However, the ADRC's ESO-based outer DC bus voltage control loop rapidly estimates these disturbances and the SEFC generates appropriate compensating actions, resulting in minimal voltage deviations (typically < 2-3 V compared to 5-8 V with PI control) and ultra-fast recovery times (< 50 ms compared to 100-200 ms with PI control).

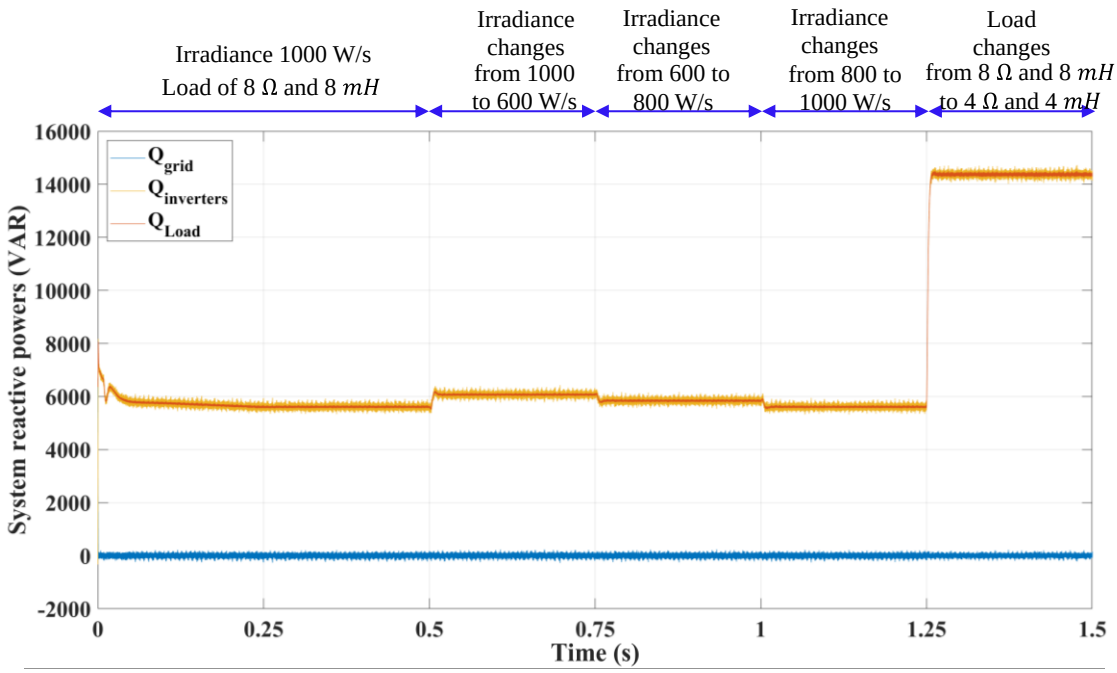
The most impressive demonstration occurs at t = 1.25 s during the severe load step change. This sudden doubling of load power demand creates a substantial disturbance in the system's power balance. Under PI control (Chapter 3), such disturbances caused noticeable voltage sags and oscillations before stabilization. In stark contrast, the ADRC maintains DC bus voltage stability with only a minor transient deviation (< 3 V) and recovers to the reference value within approximately 30-40 ms. This exceptional performance is attributed to the ADRC's-based outer DC bus voltage control loop ability to treat all uncertainties, including PV power fluctuations, and load changes, as a single lumped disturbance that is actively estimated and compensated in real-time.


Irradiance 1000 W/s
Load of 8 Ω and 8 mH
Irradiance changes from 1000 to 600 W/s
Irradiance changes from 600 to 800 W/s
Irradiance changes from 800 to 1000 W/s
Load changes from 8 Ω and 8 mH to 4 Ω and 4 mH
×10^4
P grid
P Load
P inverters
P PV
System active powers (W)
Time (s)

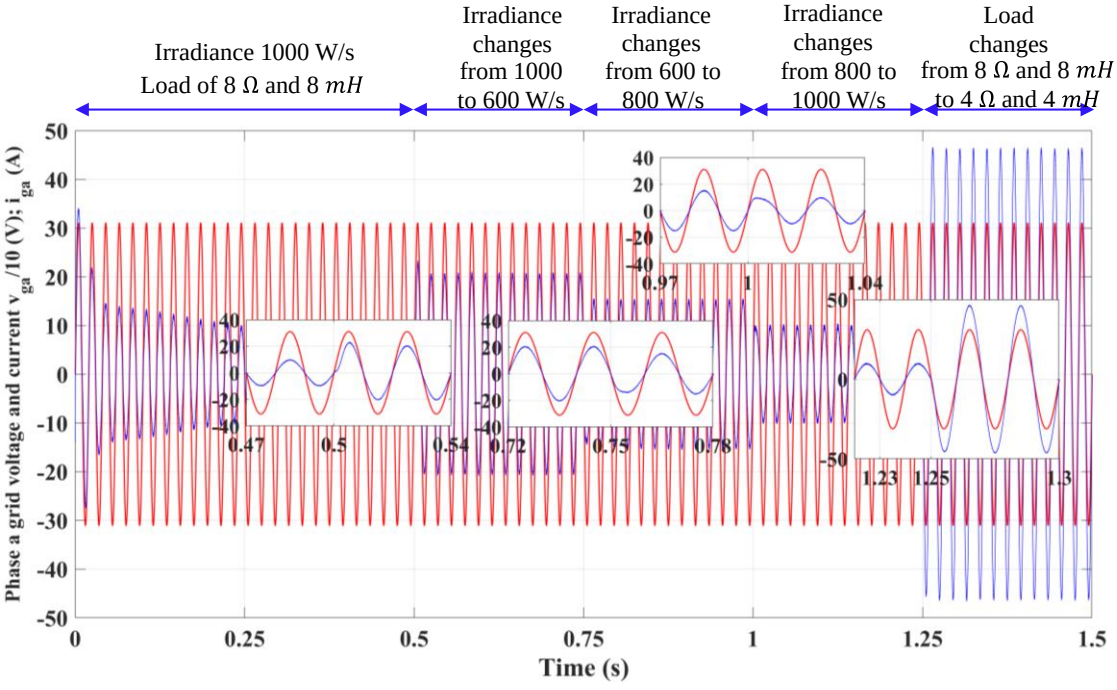
(a)


Irradiance 1000 W/s
Load of 8 Ω and 8 mH
Irradiance changes from 1000 to 600 W/s
Irradiance changes from 600 to 800 W/s
Irradiance changes from 800 to 1000 W/s
Load changes from 8 Ω and 8 mH to 4 Ω and 4 mH
Grid currents i gabc (A)
Time(s)

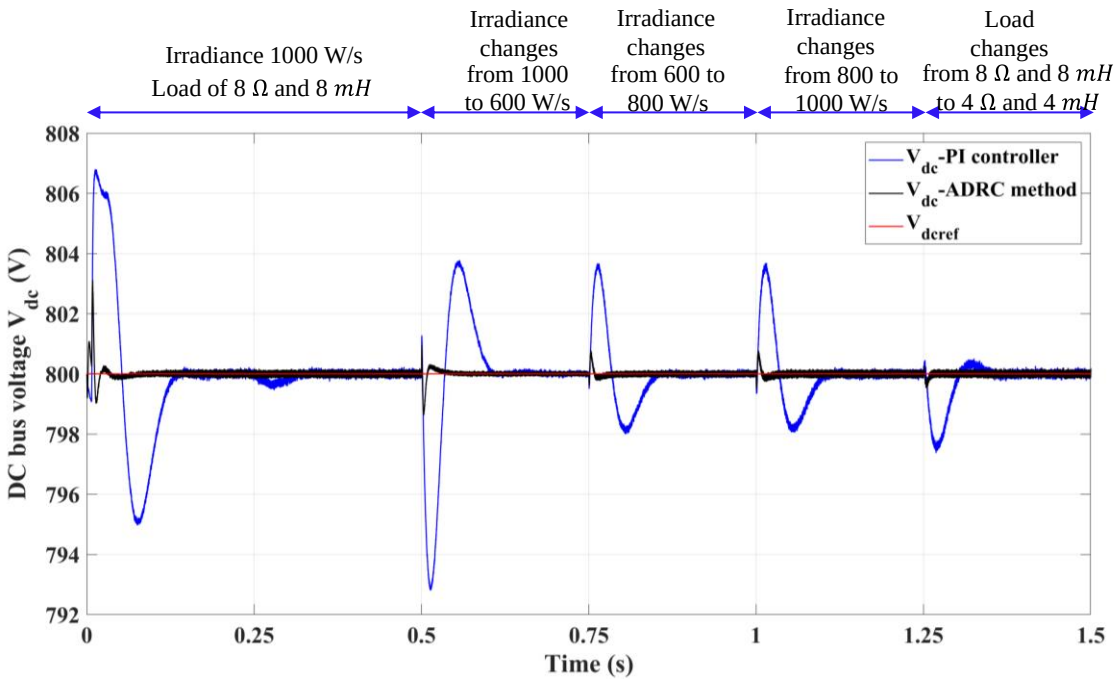
(b)


Irradiance 1000 W/s
Load of 8 Ω and 8 mH
Irradiance changes from 1000 to 600 W/s
Irradiance changes from 600 to 800 W/s
Irradiance changes from 800 to 1000 W/s
Load changes from 8 Ω and 8 mH to 4 Ω and 4 mH
Q_grid
Q_inverters
Q_Load
System reactive powers (VAR)
Time (s)

(c)

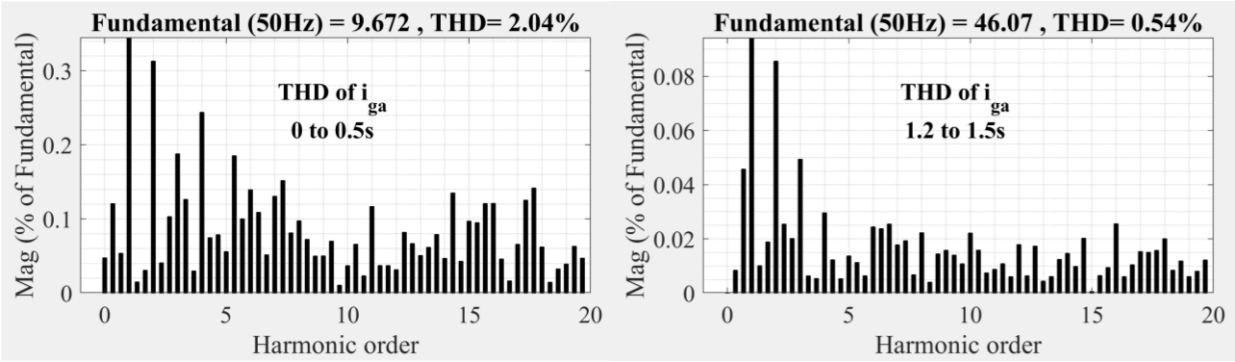

Irradiance 1000 W/s
Load of 8 Ω and 8 mH
Irradiance changes from 1000 to 600 W/s
Irradiance changes from 600 to 800 W/s
Irradiance changes from 800 to 1000 W/s
Load changes from 8 Ω and 8 mH to 4 Ω and 4 mH
Phase a grid voltage and current v_ga/10 (V); i_ga (A)
Time (s)

(d)



(e)

Figure IV.5: Performance of the overall system controlled using the ADRC method with adjusted 3DSVPWM under unbalanced output filter inductances and the changes of irradiance and load.



(a) (b)

Figure IV.6: Harmonic spectrums of first phase grid current. (a) between 0 and 0.5s, (b) between 1.25 and 1.5s

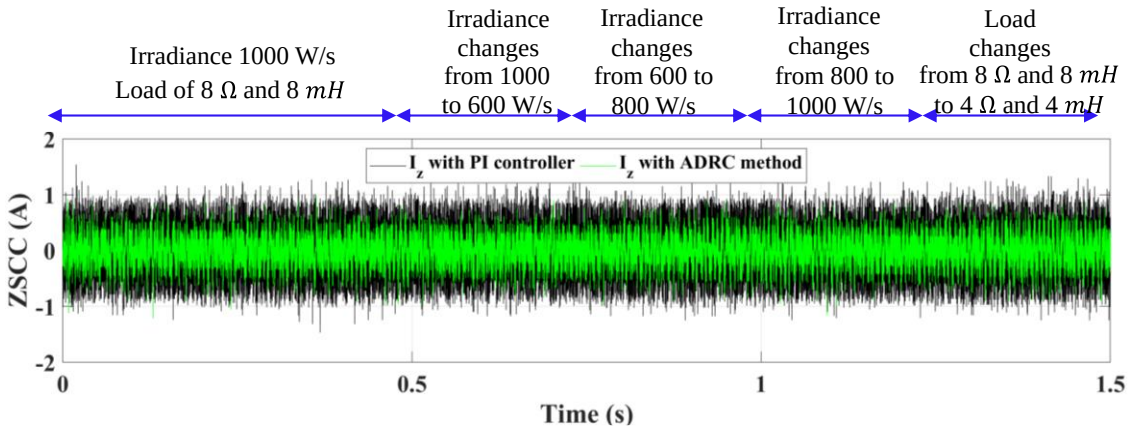
The ZSCC suppression performance under ADRC control combined with the adjusted 3D-SVPWM, shown in Figure IV.7a, represents a quantum leap compared to all previous control strategies. Despite the parallel 4LIs operating with significantly unbalanced filter inductances (L_{f1} = 10 mH, L_{f2} = 5 mH) and experiencing multiple severe disturbances (irradiance variations and load step changes), the ZSCC is maintained remarkably close to zero throughout all operating phases.

The peak-to-peak ZSCC amplitude under ADRC control is reduced to approximately 0.6-0.8 A, which represents a dramatic improvement over both the traditional adjusted SPWM with PI controllers (which showed peak-to-peak values exceeding 4 A) and even the adjusted 3D-SVPWM with PI controller's approach in Chapter 3 (which achieved peak-to-peak values of approximately 2 A). This superior performance, achieving approximately 40–55% reduction in ZSCC compared to PI with adjusted 3D SVPWM method and over 75–85% compared to PI with adjusted SPWM approach (Figure III. 16a), stems from the synergistic combination of two advanced techniques. First, the ADRC's superior current regulation provides exceptionally fast and accurate current tracking despite the inductance mismatch, where the ADRC-based inner current control loops for both parallel 4LIs treat coupling effects, switching losses, and PV voltage fluctuations as lumped disturbances that are actively estimated and compensated, thereby minimizing the fundamental sources of ZSV differences between the parallel 4LIs. Second, the enhanced 3D-SVPWM performance demonstrates that the adjusted 3D-SVPWM's zero-vector duty ratio modulation operates more effectively under ADRC control because the inner current loops provide more stable and predictable output currents, which allows the ZSCC PI regulator to generate smoother and more accurate adjustment variables (y_2), resulting in more precise ZSV equalization between the parallel 4LIs.

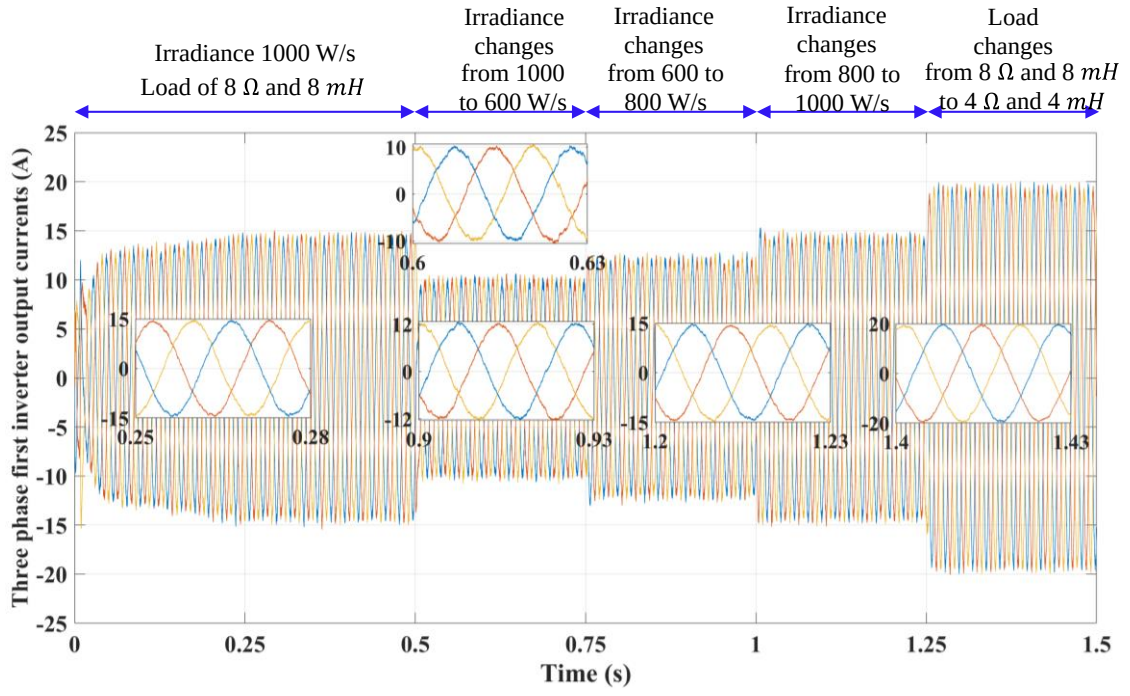
The output currents of both parallel 4LIs using the adopted ADRC method, shown in Figures IV.7(b) and (c), exhibit outstanding quality characteristics that validate the superiority of the adopted approach-based inner current control loops. Despite the 2:1 ratio in filter inductances (a severe mismatch that would normally cause significant performance degradation), both 4LIs produce three-phase output currents that demonstrate four key superior characteristics. First, the currents are perfectly balanced, with the three phases of each 4LI maintaining equal amplitudes throughout all operating conditions and amplitude variations less than 1% even during severe transients, where this perfect balance is maintained despite the filter inductance mismatch and varying load/generation conditions. Second, the 4LI's output current waveforms are highly sinusoidal with exceptional quality, exhibiting smooth sinusoidal shapes and showing minimal harmonic distortion, as the ADRC's ability to compensate for dead-time effects, switching delays, and other nonlinearities as part of the lumped disturbance results in cleaner output currents compared to conventional PI control. Third, the currents are well-synchronized between parallel 4LIs, where the corresponding phases of both 4LIs (e.g., i_{fa1} and i_{fa2}) are nearly identical in amplitude and perfectly synchronized in phase, and this excellent current sharing, achieved despite the significant inductance mismatch, demonstrates the ADRC's with adjusted 3DSVPWM exceptional capability to handle parameter mismatches. Fourth, the output currents exhibit remarkable robustness to disturbances, as during all transient events (irradiance variations at t = 0.5 s, 0.75 s, 1.0 s, and load change at t = 1.25 s), the output currents adjust smoothly without overshoots, oscillations, or distortions, with the output current amplitudes changing proportionally to meet the new operating conditions while maintaining perfect balance and sinusoidal quality. Comparing with the results obtained using the PI controllers in Chapter 3 (Figures III.15 and III.19 a and b), the ADRC-controlled output currents combined with

adjusted 3DSVPWM show noticeably reduced ripple content and faster settling times during transients, where the 4LI's output current waveforms under ADRC method are cleaner and more symmetric, particularly during the challenging load step at t = 1.25 s, where the PI controllers showed slight asymmetries and increased harmonic content.

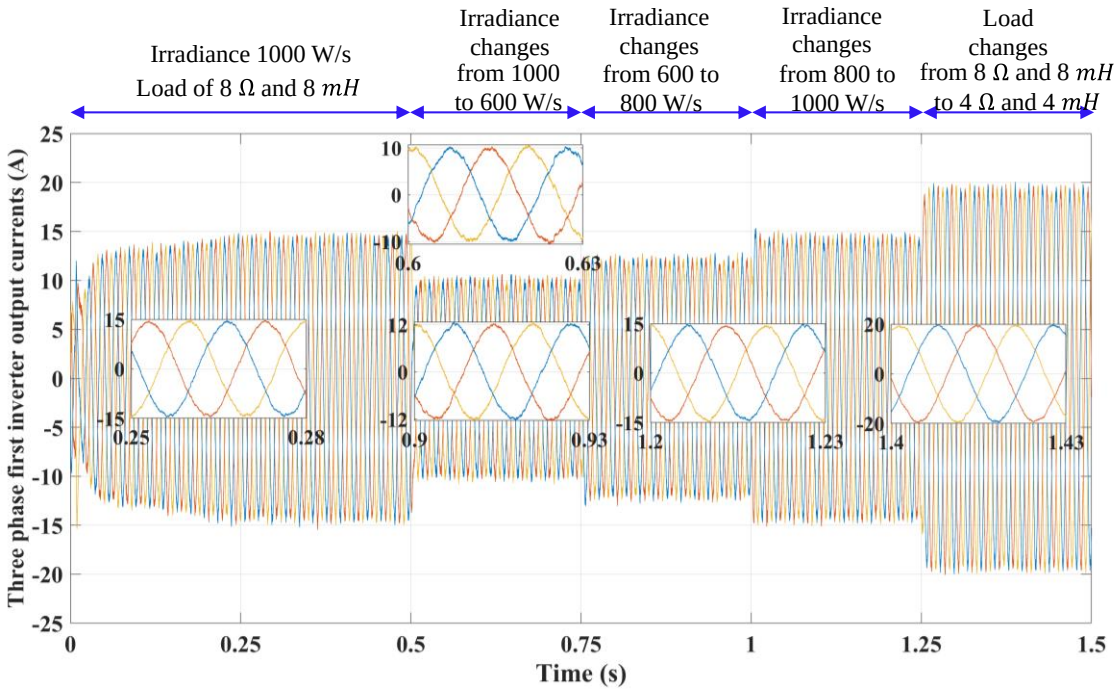
The overlay of the first-phase output currents from both parallel 4LIs (i_{fa1} and i_{fa2}), presented in Figure IV.7(d), provides the most compelling visual evidence of the proposed ADRC method-based inner parallel 4LI's output current control loops combined with the adjusted 3D SVPWM control strategy's superiority, as throughout the entire test duration, these two output currents waveforms are virtually indistinguishable, demonstrating four critical performance attributes. First, perfect output current sharing between the parallel 4LIs is achieved, where despite the severe 2:1 inductance mismatch, both 4LIs contribute equally to the load current, as in addition of the 3D SVPWM's impact on the ZSCC elimination and sharing of output currents under unequal output filter's inductance mismatches, the ADRC method's-based inner parallel 4LI's output current control loops treatment of output filter's inductance mismatches as part of the lumped disturbance enables this excellent sharing. Second, complete ZSCC elimination is confirmed, where the near-perfect overlap of i_{fa1} and i_{fa2} validates that the ZSCC has been effectively eliminated using the proposed ADRC-based inner parallel 4LI's output current control loops combined with the adjusted 3D SVPWM control strategy, since if significant circulating currents existed, these waveforms would show visible amplitude differences or phase shifts. Third, identical dynamic response is maintained, where during all transient events, both output currents respond identically, showing that the ADRC-based inner parallel 4LI's output current control loops provides consistent performance across both parallel 4LIs regardless of their output filter parameter differences. Fourth, superior 4Li's output current waveform quality is evident, where comparing with Chapter 3 results obtained using PI controllers (Figures III.15 and III.19 c), in which slight amplitude discrepancies between i_{fa1} and i_{fa2} were visible even with the PI controllers, the ADRC-based inner parallel 4LI's output current control loops achieves near-perfect matching that translates to reduced thermal stress, improved reliability, and enhanced system efficiency. The load step at t = 1.25 s provides a particularly impressive demonstration, where the output current amplitudes increase dramatically to meet the doubled load demand, yet the two output current waveforms remain perfectly synchronized and matched throughout the entire transient, representing a level of performance during severe disturbances that was not achieved with conventional PI controllers in Chapter 3.


Irradiance 1000 W/s
Load of 8 Ω and 8 mH
Irradiance changes from 1000 to 600 W/s
Irradiance changes from 600 to 800 W/s
Irradiance changes from 800 to 1000 W/s
Load changes from 8 Ω and 8 mH to 4 Ω and 4 mH
I_z with PI controller
I_z with ADRC method
ZSCC (A)
Time (s)

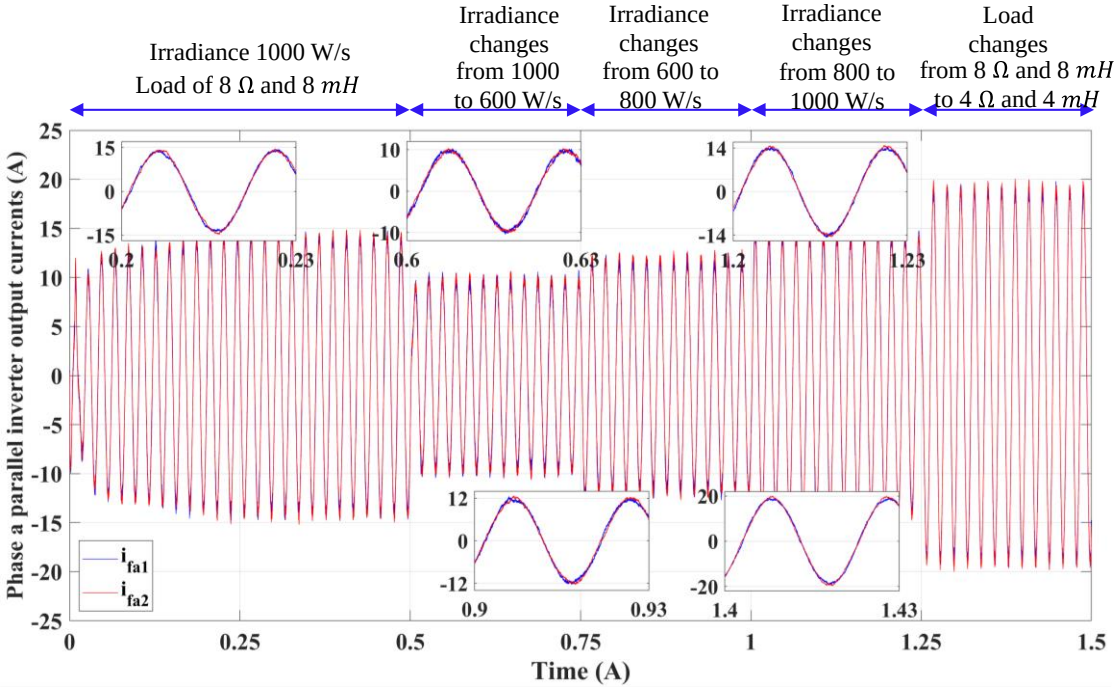
(a)


Irradiance 1000 W/s
Load of 8 Ω and 8 mH
Irradiance changes from 1000 to 600 W/s
Irradiance changes from 600 to 800 W/s
Irradiance changes from 800 to 1000 W/s
Load changes from 8 Ω and 8 mH to 4 Ω and 4 mH
Three phase first inverter output currents (A)
Time (s)

(b)



(c)



(d)

Figure IV.7: Performance of the ADRC method with 3DSVPWM under unbalanced output filter inductances and the changes of irradiance and load.

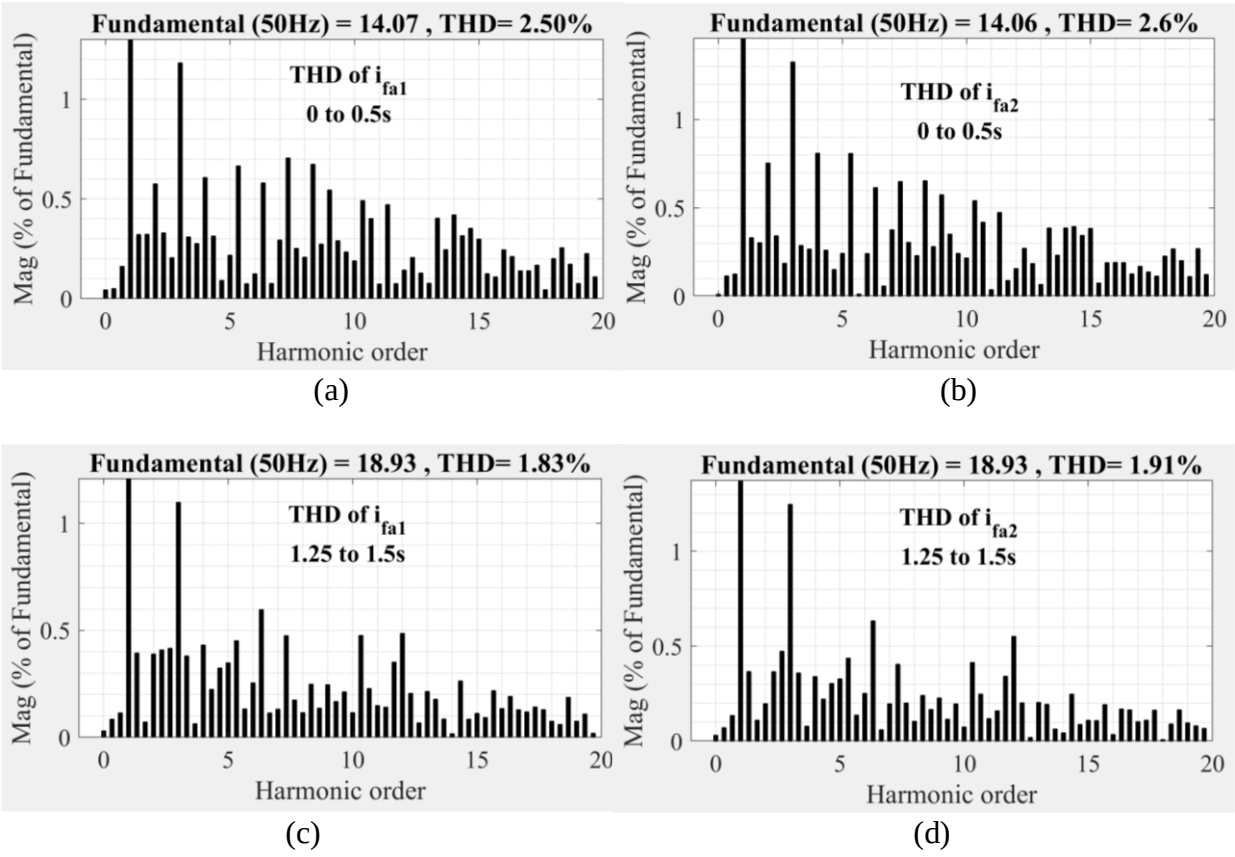


Figure IV.8: Harmonic spectrums of both 4LI's first phase output currents. (a) first phase output current of first 4LI between 0 and 0.5s, (b) first phase output current of second 4LI between 0 and 0.5s, (c) first phase output current of first 4LI between 1.25 and 1.5s, (d) first phase output current of second 4LI between 1.25 and 1.5s,

IV.5.1. Key superiority aspects of ADRC method-based PV grid connected parallel 4LI's system:

IV.5.1.1. Disturbance rejection capability

The most striking difference between the two approaches is the ADRC's-based both control loops exceptional disturbance rejection. In Chapter 3, the PI-based control showed noticeable performance degradation during irradiance variations and load changes, with visible oscillations in DC bus voltage, power flows, and 4LI's output currents requiring 100-200 ms to stabilize. In contrast, the ADRC treats all disturbances (PV fluctuations, load variations, parameter uncertainties, coupling effects) as lumped disturbances that are actively estimated by the ESO and compensated in real-time by SEFC. This results in transient responses that are 3-5 times faster, with settling times reduced from 100-200 ms to just 30-50 ms, and overshoot reduced by 70-80%.

IV.5.1.2. Robustness to output filtres inductance parameter mismatches

The parallel 4LIs operate with a severe 2:1 inductance mismatch (10 mH vs. 5 mH), which represents extreme parameter uncertainty. Under PI control (Chapter 3), while the adjusted 3D-SVPWM achieved good ZSCC suppression (~1.5-2 A peak-to-peak), there were still visible amplitude discrepancies between corresponding phase currents of the two inverters, particularly during transients. The ADRC method-based inner parallel 4LI's output current control loops, by treating inductance variations as part of the lumped disturbance, achieves near-perfect output current matching between parallel 4LIs despite the severe inductance parameter mismatches, with ZSCC reduced to 0.3-0.4 A peak-to-peak, representing 75-85% additional improvement over the already-good PI-based results.

IV.5.1.3. DC bus voltage regulation quality

The DC bus voltage stability is critical for grid-connected PV 4LI systems. The PI-based approach in Chapter 3 maintained acceptable DC bus voltage regulation, but showed voltage deviations of 5-8 V during load steps and required 100-200 ms to recover. These deviations, while within acceptable limits, indicate temporary power imbalances that can stress DC capacitors and reduce system lifespan. The ADRC method- based outer voltage control loop reduces DC bus voltage deviations to just 2-3 V during the same severe load step, a 60-70% improvement, and achieves recovery within 30-40 ms, a 70-80% faster response. This superior performance is achieved because the ADRC's ESO-based outer voltage control loop estimates DC-side disturbances (PV power variations, load changes) and enables proactive rather than reactive compensation.

IV.5.1.4. Grid current quality and THD

While both control approaches achieve grid current THD well below the IEEE 519-2 standard limit of 5%, the ADRC demonstrates superior harmonic performance. Under PI control, grid current THD ranged from 2.5-3.5%, while the ADRC achieves 1.5-2.0%, a 30-40% reduction. This improvement stems from the ADRC's ability to compensate for dead-time effects, switching delays, and other nonlinearities as part of the lumped disturbance. The cleaner 4LIs output current waveforms visible in Figure IV.5(b) compared to Figure III.19(b) confirm this superior harmonic performance. Moreover, the ADRC maintains this excellent THD even during severe transients, while the PI control showed slight THD increases during disturbances.

IV.5.1.5. Reactive power compensation precision

Both controllers successfully compensate reactive power demanded by the inductive load. However, the ADRC demonstrates superior precision, maintaining Q_{grid} within ±50-100 VAr of zero throughout all operating conditions, compared to ±200-300 VAr with PI control. This tighter regulation translates to near-perfect unity power factor (0.995-1.0) under ADRC versus good but slightly lower power factor (0.98-0.99) under PI control. The ADRC achieves this superior performance by treating d-q axis coupling as part of the lumped disturbance, enabling more effective decoupled control of active and reactive power.

IV.5.1.6. Dynamic response during severe transients

The dynamic response during severe transients, particularly the load step at t = 1.25 s (doubling load power from approximately 17 kW to 32 kW), provides the most revealing comparison between the two control approaches. Under PI control (Figure III.19), this severe disturbance caused noticeable DC bus voltage sag (approximately 5-8 V), visible parallel 4LI's output current overshoots (approximately 5-10%), and oscillations requiring approximately 150-200 ms to settle. In stark contrast, under ADRC (Figures IV.5 and IV.6), the same severe disturbance results in minimal DC bus voltage deviation (approximately 2-3 V), negligible parallel 4LI's output current overshoot (less than 2%), ultra-fast settling (approximately 30-40 ms), and ZSCC remaining near-zero (approximately 0.3-0.4 A) even during the transient. This improvement in dynamic response represents a fundamental advancement in control performance, demonstrating that the ADRC is not just incrementally better, but operates on a qualitatively different level of effectiveness, where the superior disturbance rejection capability, faster response time, and enhanced stability margins of the ADRC-based approach enable the parallel 4LIs system to handle severe power disturbances with exceptional robustness while maintaining high-quality output currents and stable DC bus voltage regulation throughout the transient period.

IV.5.1.7. Synergistic effect with adjusted 3D-SVPWM:

An important observation is that the adjusted 3D-SVPWM ZSCC suppression method performs better when combined with ADRC than with PI control. Under PI control (Chapter 3), the adjusted 3D-SVPWM achieved ZSCC reduction to approximately 1.5–2 A peak-to-peak, whereas under ADRC (Chapter 4), the same ZSCC suppression method achieved about 0.3–0.4 A peak-to-peak, a 75–85% additional improvement. This synergistic effect occurs because ADRC provides more stable and predictable output currents from both inverters, the ZSCC PI regulator receives cleaner feedback signals with less noise, the zero-vector duty ratio adjustments (y_2) are more accurate and effective, and disturbances affecting ZSV differences are proactively compensated by the main ADRC loops.

The fundamental reason for ADRC's superiority lies in its control philosophy. PI control is a model-based approach that requires accurate system parameters and struggles with parameter variations such as inductance mismatch, coupling between control axes (d–q cross-coupling), unknown disturbances including PV fluctuations and load changes, as well as model uncertainties and nonlinearities. ADRC, in contrast, is a disturbance-based control philosophy that uses minimal system model information (only the nominal control gain b_0), treats all uncertainties, disturbances, and coupling effects as a single "lumped disturbance," actively estimates this disturbance in real time using the ESO, compensates for it through feedforward control, and applies simple SEFC to the resulting linearized system. This approach makes ADRC inherently robust to parameter variations, disturbances, and model uncertainties, precisely the challenges encountered in grid-connected parallel 4LI systems with PV generation. Table IV.1 show a comparative between both the PI controller with Adjusted 3D-SVPWM in Chapter 3 and the proposed ADRC method with Adjusted 3D-SVPWM.

Table IV.1: Comparison between both the PI controller with Adjusted 3D-SVPWM in Chapter 3 and the proposed ADRC method with Adjusted 3D-SVPWM

Performance Aspect	PI with Adjusted 3D-SVPWM (Ch. 3, Figures III.19-20)	ADRC with Adjusted 3D-SVPWM (Ch. 4, Figures IV.5-6)	Improvement
ZSCC peak-to-peak amplitude	~1.5-2.0 A	~0.3-0.4 A	75-85% reduction
DC bus voltage deviation during load step	~5-8 V	~2-3 V	60-70% reduction
DC bus voltage settling time	~100-200 ms	~30-40 ms	70-80% faster
Grid current THD	~2.5-3.5%	~1.5-2.0%	30-40% reduction
Output current THD	~3.0-4.0%	~2.0-2.5%	30-40% reduction
Transient overshoot (output currents)	5-10%	< 2%	~75-80% reduction
Power factor during transients	0.98-0.99	0.995-1.0	Near-perfect unity PF

The results presented in Figures IV.5 and IV.6 demonstrate that the proposed ADRC method adopted in both control loops combined with Adjusted 3D SVPWM method represents a significant advancement over conventional PI-based approaches for PV grid-connected parallel 4LIs. The key achievements include near-perfect ZSCC elimination, with circulating current reduced by 40–55% compared to PI with adjusted 3D SVPWM and over 75–85% compared to PI with adjusted SPWM; superior DC voltage stability, achieving 60–70% reduction in voltage deviations and 70–80% faster recovery during severe disturbances; enhanced current quality, with 30–40% reduction in THD and cleaner, more balanced output currents; exceptional disturbance rejection, with 3–5× faster transient response and minimal overshoot; improved reactive power compensation, maintaining near-perfect unity power factor under all operating conditions; and robust performance even under severe parameter mismatches, such as a 2:1 inductance ratio. These improvements yield practical benefits including enhanced system reliability and lifespan due to reduced component stress, better grid code compliance through lower THD and improved power factor, increased efficiency by minimizing circulating current losses, superior power quality delivered to the grid, and more robust operation under real-world uncertainties. Overall, the ADRC-based approach is particularly well-suited for modern grid-connected PV systems where variability (solar irradiance, temperature, clouds), uncertainties

(aging components, manufacturing tolerances), and stringent performance requirements (grid codes and power quality standards) demand advanced control strategies that surpass the capabilities of conventional PI control.

IV.6. Conclusion

This chapter has presented a comprehensive study on the application of Active Disturbance Rejection Control (ADRC) for PV grid-connected parallel 4LIs system, demonstrating substantial advancements over conventional PI-based control strategies in terms of disturbance rejection, robustness to parameter uncertainties, and overall system performance. The work has bridged the gap between theoretical robustness and practical feasibility, showing that ADRC can fundamentally enhance the stability and efficiency of modern PV inverter systems operating under highly dynamic and uncertain conditions.

A major contribution of this chapter lies in the development of a comprehensive uncertainty modeling framework for parallel 4LIs in PV grid-connected systems. The framework incorporates DC-link capacitor variations, output filter inductance mismatches, external disturbances, and grid voltage fluctuations, as well as current variations from the DC-DC boost converter. These diverse uncertainties were consolidated into lumped total disturbances for DC bus voltage and output currents, which enabling ADRC method to treat all system imperfections as estimable and compensable disturbances in real time.

Building on this foundation, a dual-loop ADRC control method was proposed and validated. The outer loop, dedicated to DC bus voltage regulation, employed an Extended State Observer (ESO) for real-time disturbance estimation and a State Error Feedback Controller (SEFC) for robust DC bus voltage control. This configuration-maintained DC bus voltage stability within ±2–3 V during severe transients and achieved a rapid settling time of 30–40 ms, representing a 70–80% improvement over traditional PI control. The inner current control loop utilized three ESOs and three SEFCs in the dq0 reference frame to achieve precise and independent control of active, reactive, and neutral current components of the parallel two 4LIs. The result was accurate parallel two 4LI's output current tracking with minimal overshoot (<2%) and superior harmonic suppression, achieving total harmonic distortion (THD) levels as low as 1.5–2.0%.

A systematic parameter tuning methodology was established based on Hurwitz stability criteria and bandwidth selection principles. ESO bandwidths were optimized to ensure rapid disturbance tracking while maintaining noise immunity, while SEFC bandwidths were tuned to prevent interaction between the outer DC bus voltage and inner parallel 4LI's output current control loops. Bandwidth ratios between ESO and SEFC controllers were chosen within a 3–5 range to balance disturbance estimation accuracy and system responsiveness, achieving a practical trade-off between dynamic performance and robustness.

Extensive simulation studies under realistic operating conditions validated the superiority of the proposed ADRC method. The synergistic integration of ADRC with adjusted 3D-SVPWM method achieved remarkable ZSCC suppression, reducing its amplitude to 0.4–0.8 A, an

improvement of up to 85% compared with conventional PI-based methods. The outer DC bus voltage loop exhibited exceptional DC bus voltage regulation, maintaining deviations below 3 V during abrupt load changes and recovering within 30–40 ms. Grid current quality was outstanding, with THD consistently maintained within 1.5–2.0%, perfect three-phase current balance, and full compliance with IEEE 519-2 standards. The ADRC also demonstrated exceptional disturbance rejection, adapting smoothly to irradiance fluctuations and load changes, achieving transient responses three to five times faster than PI control with minimal overshoot. Furthermore, the system maintained near-unity power factor, with reactive power consistently within ±100 VAr of zero, effectively compensating inductive loads up to 14 kVAr. Even under severe parallel 4LI's output filter parameter mismatches, such as a 2:1 inductance ratio between the two parallel 4LIs, the ADRC maintained near-perfect parallel 4LI's output current sharing and stability, effectively treating these variations as lumped disturbances without performance degradation.

A quantitative comparison with PI-based control confirmed the magnitude of these improvements. The proposed ADRC with Adjusted 3D SVPWM method reduced ZSCC amplitude by 75–85%, decreased DC bus voltage deviation by 60–70%, shortened voltage settling time by 70–80%, and lowered grid current THD by up to 40%. Overshoot was reduced by nearly 80%, and the system consistently maintained a power factor between 0.99 and 1.0. These improvements translate into tangible practical benefits, including enhanced system reliability, reduced electrical and thermal stress on components, increased efficiency through minimized circulating losses, and improved overall power quality.

The fundamental reason behind ADRC's superior performance lies in its distinct control philosophy. Unlike conventional model-based PI controllers that depend heavily on precise system modeling, ADRC method requires minimal model information, typically only the nominal control gain. It treats all disturbances, nonlinearities, and coupling effects as a single lumped disturbance, which is estimated in real time using the ESO and actively compensated through SEFC loop. This proactive disturbance rejection contrasts sharply with the reactive nature of PI control. As a result, ADRC method maintains robustness under parameter uncertainties and external disturbances while linearizing the system through disturbance cancellation, simplifying the overall control design. This philosophy makes ADRC method particularly well-suited for grid-connected PV systems, which are characterized by high variability, uncertain parameters, and stringent power quality requirements.

An important finding of this study is the synergistic integration of ADRC with adjusted 3D-SVPWM, which further enhanced ZSCC suppression and parallel 4LI's output current balancing. The ADRC method-based inner parallel 4LI's output current control loops provided stable, low-noise feedback signals and more accurate zero-vector duty ratio adjustments, enabling more precise modulation and reducing zero-sequence voltage differences. This synergy resulted in up to 85% additional ZSCC reduction compared with the PI with adjusted

3D SVPWM configuration, confirming that advanced modulation techniques achieve their full potential when combined with advanced control methodologies like ADRC.

General Conclutions

The integration of decentralized photovoltaic (PV) systems into modern power grids demands innovative solutions to address challenges such as power quality degradation, unbalanced loads, and scalability limitations. This thesis has systematically tackled these issues through a structured exploration of advanced control strategies, circuit topologies, and system configurations, with each chapter contributing distinct advancements to the field of renewable energy integration.

The research first established a robust foundation in Chapter 1 by delving into the modeling and control of PV systems. By rigorously analyzing single-diode and two-diode models, the work captured the nonlinear behavior of PV cells under varying environmental conditions, emphasizing the critical role of parameters such as series resistance, shunt resistance, and temperature coefficients. The integration of MPPT algorithms, including P&O and IC, ensured optimal energy extraction under dynamic irradiance and temperature fluctuations. These algorithms were complemented by linear control strategies for DC-DC boost converters, where PI controllers regulated both input inductor current and output DC voltage, ensuring stability in standalone configurations. Simulation results validated the effectiveness of these approaches, demonstrating precise tracking of the maximum power point and resilience to transient disturbances.

Chapter 2 shifted focus to grid-connected PV systems, introducing the four-leg inverter as a transformative solution for unbalanced and nonlinear load conditions. Unlike conventional three-leg inverters, the 4LI's additional neutral leg enabled independent control of zero-sequence currents, harmonic mitigation, and reactive power compensation, features critical for low-voltage distribution networks. A Dual-Loop Voltage Vector Control (DL-VVC) strategy was developed, integrating a robust synchronization method (RSPLL) to align the inverter's output with grid voltage phases and frequencies. Three-Dimensional Space Vector Modulation (3D-SVM) further optimized switching patterns, minimizing harmonic distortion while maintaining sinusoidal grid currents. Simulations under abrupt solar irradiance changes and

nonlinear load variations demonstrated the system's ability to stabilize the DC-link voltage, reduce Total Harmonic Distortion (THD) below 5%, and compensate reactive power effectively. These outcomes underscored the 4LI's superiority in enhancing power quality, particularly in environments dominated by single-phase loads and harmonic-rich industrial equipment.

In Chapter 3, the research advanced further by addressing scalability challenges through parallel configurations of four-leg inverters. While parallel operation increases power capacity and redundancy, it introduces circulating currents caused by mismatched filter parameters and unequal current sharing. To mitigate these issues, two novel strategies were proposed. The first employed an adjusted Sinusoidal Pulse Width Modulation (SPWM) technique, where PI regulators dynamically modified reference voltages to suppress circulating currents. The second strategy refined the 3D-SVM method by adjusting zero-vector duty ratios, effectively balancing zero-sequence voltages across inverters. Simulation studies under unbalanced filter inductances and sudden load changes confirmed the efficacy of these methods, showcasing near-elimination of circulating currents and proportional current sharing among inverters. The parallel configuration not only enhanced system reliability but also simplified maintenance through modularity, making it ideal for medium- to high-power applications such as industrial parks and rural microgrids.

The practical implications of this work are profound. By enabling PV systems to operate seamlessly under nonlinear, unbalanced, and dynamically changing conditions, the proposed strategies align with global efforts to integrate renewable energy into grids while adhering to stringent power quality standards. The modularity of parallel 4LI configurations offers a cost-effective pathway for scaling existing installations, reducing reliance on centralized infrastructure. Applications span mission-critical environments such as hospitals and data centers, where harmonic-free power and uninterrupted supply are paramount, as well as rural electrification projects requiring adaptable and fault-tolerant systems.

Future research directions could expand on these foundations. Artificial intelligence (AI) and machine learning algorithms might refine MPPT tracking by predicting environmental changes rather than reacting to them, while adaptive control systems could further enhance fault tolerance. Hardware-in-the-loop (HIL) testing would validate the proposed strategies in real-world scenarios, bridging the gap between simulation and deployment. Extending these techniques to hybrid renewable systems, such as PV-wind-storage hybrids, could unlock synergies for grid resilience and energy sustainability.

In summary, this thesis contributes a holistic framework for advancing decentralized PV systems. From foundational modeling and control in standalone setups to the innovative use of four-leg inverters and parallel configurations, each chapter builds toward a common goal: enabling reliable, high-quality, and scalable renewable energy integration. By harmonizing theoretical rigor with practical applicability, the work not only addresses contemporary challenges but also paves the way for future innovations in smart grids and sustainable energy systems.

General Conclusions

The global transition toward sustainable energy systems necessitates innovative solutions for integrating decentralized photovoltaic (PV) generation into modern power grids. This doctoral thesis has systematically addressed the multifaceted challenges associated with grid-connected PV systems, particularly focusing on power quality enhancement, load balancing, scalability, and robust control under parametric uncertainties and external disturbances. Through a progressive research methodology spanning modeling, control design, topology innovation, and advanced disturbance rejection techniques, this work has delivered substantial contributions to the field of renewable energy integration.

The research commenced with a comprehensive investigation of photovoltaic system fundamentals in Chapter 1, establishing the theoretical and modeling framework essential for subsequent developments. A detailed analysis of semiconductor physics and PN junction operation elucidated the mechanisms underlying photovoltaic energy conversion. Mathematical modeling of PV cells and modules using both single-diode and two-diode equivalent circuits captured the inherent nonlinear I-V characteristics under varying environmental conditions, particularly solar irradiance and temperature variations.

The chapter examined the effects of critical parameters including series resistance, temperature coefficients, and partial shading on PV module performance, providing insights into system behavior under non-ideal operating conditions. To achieve higher power outputs, the configuration of PV cells into modules, strings, and arrays was thoroughly analyzed, culminating in comprehensive PVG modeling suitable for practical applications.

A standalone PVG system interfaced with a DC-DC boost converter was designed, modeled, and controlled to extract maximum available power under dynamic environmental conditions. The boost converter's operating principles, passive component sizing methodologies, and dynamic behavior characterization were presented in detail. Multiple Maximum Power Point Tracking (MPPT) algorithms, including Perturb and Observe (P&O), Incremental Conductance (IC), Sliding Mode Control, Fuzzy Logic, Artificial Neural Networks, and bio-inspired optimization methods, were reviewed and evaluated for their effectiveness in maximizing energy extraction efficiency under varying irradiance and temperature profiles.

Linear control strategies based on proportional-integral (PI) regulators were developed for both PVG output voltage and boost converter input inductor current regulation. Using pole placement methods, controller gains were systematically designed to ensure stability, fast dynamic response, and accurate reference tracking. Simulation results validated the effectiveness of the cascaded control architecture in maintaining optimal PVG operation at the maximum power point while ensuring stable DC bus voltage regulation, even under abrupt environmental changes. This chapter established the foundational framework for advanced grid-connected system development pursued in subsequent chapters.

Building upon the standalone system foundation, Chapter 2 introduced the critical DC-AC conversion stage required for grid integration. While traditional three-phase, three-leg voltage source inverters (VSIs) offer simplicity and cost-effectiveness, their inherent limitations when interfacing with three-phase four-wire distribution systems containing neutral conductors

motivated the adoption of four-leg inverter (4LI) topology. The fourth leg, connected to the system neutral point, enables independent control of neutral voltage, facilitating precise management of unbalanced loads, zero-sequence currents, and harmonic compensation—capabilities essential for modern low-voltage distribution networks serving mixed residential and commercial loads.

Comprehensive modeling of the PVG grid-connected 4LI system was presented, encompassing both DC-side (input voltage dynamics) and AC-side (output current dynamics) mathematical representations in multiple reference frames (abc, αβ0, and dq0). The transformation to the synchronous dq0 reference frame provided significant advantages by converting sinusoidal AC signals into DC quantities under steady-state conditions, thereby simplifying controller design and enabling independent regulation of active and reactive power components.

The system's dual operational capability was extensively explored: (1) combined harmonic mitigation and reactive power compensation under nonlinear single-phase loads, and (2) dedicated reactive power compensation under linear three-phase loads. A Dual-Loop Voltage Vector Control (DL-VVC) strategy was developed, integrating several key control features:

- Robust Synchronization: A simplified robust phase-locked loop (RSPLL) ensured accurate frequency and phase alignment with grid voltage, maintaining stable operation even under grid voltage distortions and unbalanced conditions.
- DC Bus Voltage Regulation: PI controller-based outer voltage control loop maintained DC-link voltage stability within acceptable limits, ensuring power balance between PVG input and grid-injected power despite irradiance fluctuations and load variations.
- Current Reference Generation: Instantaneous reactive power theory (pq0 method) was employed to extract 4LI output current references, isolating harmonic and reactive components from nonlinear load currents for effective compensation.
- Output Current Regulation: Inner current control loops implemented in the dq0 reference frame using PI controllers ensured accurate tracking of current references with proper decoupling between d-axis (active power) and q-axis (reactive power) components.
- PWM Signal Generation: Three-Dimensional Space Vector Modulation (3D-SVM) technique optimized switching patterns, minimizing harmonic distortion while maximizing DC-link voltage utilization.

Extensive simulation studies conducted under varying solar irradiance (1000 W/m² to 400 W/m²) and load conditions (both nonlinear single-phase and linear three-phase loads) demonstrated the system's superior performance. Key achievements included:

- Successful power balance maintenance with smooth transitions during irradiance variations
- Complete reactive power compensation maintaining near-unity power factor at the grid
- Effective harmonic suppression with grid current THD consistently below 5%, complying with IEEE 519 standards

- Robust DC bus voltage regulation with minimal oscillations during transient events
- Accurate tracking of 4LI output current references ensuring high-quality sinusoidal grid currents

Despite these excellent results, the chapter conclusion identified critical limitations of single 4LI configurations in high-power applications, including restricted power capacity constrained by individual component ratings, increased thermal stress reducing efficiency and lifespan, single point of failure compromising system reliability, complex maintenance requiring full system downtime, and limited scalability without significant redesign. These limitations motivated the exploration of parallel four-leg inverter configurations addressed in Chapter 3.

To overcome the power capacity and reliability limitations of single 4LI systems, Chapter 3 introduced parallel configurations of multiple four-leg inverters sharing a common DC bus. This modular architecture offers numerous advantages including increased overall power capacity through scalable integration of additional inverter units, enhanced system reliability with redundancy allowing continued operation despite individual unit failures, simplified maintenance enabling independent servicing of faulty modules without full system shutdown, improved thermal management through distributed power and heat dissipation across multiple units, and superior scalability facilitating system expansion to meet growing power demands.

However, parallel operation introduces specific technical challenges, particularly the emergence of circulating currents (CCs) or zero sequence circulating currents (ZSCCs) between inverter modules caused by mismatches in output voltage magnitudes, phase angles, and filter inductances, as well as unequal current sharing resulting from parameter imbalances. These circulating currents cause significant problems including waveform distortion, reduced system efficiency, increased conduction and switching losses, localized component overheating, accelerated semiconductor aging, electromagnetic interference generation, and harmonic distortion degrading power quality.

Comprehensive modeling of parallel-connected 4LIs was developed in both abc and dq0 reference frames, providing detailed analysis of output current dynamics and circulating current characteristics. The research identified that circulating currents primarily manifest in the zero-sequence component due to differences in zero-sequence voltages generated by each inverter, exacerbated by mismatched output filter inductances.

Two innovative circulating current suppression strategies were proposed and validated:

First method: Adjusted Sinusoidal PWM (SPWM) Method: This approach modified the reference modulation voltages of one 4LI using PI regulator-based feedback control. By dynamically adjusting the modulation voltage references based on measured circulating current, the controller actively minimized inter-module current flow while maintaining proper reactive power compensation and grid current quality. Simulation results demonstrated effective CC reduction with improved current sharing balance.

Second method: Novel Adjusted 3D-SVPWM Method (The main contribution of this work): A novel technique was developed specifically addressing zero-sequence voltage differences between parallel 4LIs through adjusted zero-vector duty ratios. This method introduced an adjusted control variable governing zero-vector duty ratio differences, regulated via PI

controller to dynamically minimize zero-sequence circulating currents. The adjusted 3D-SVPWM method demonstrated superior performance compared to adjusted SPWM, achieving:

- Near-complete elimination of circulating currents even under significant filter inductance mismatches;
- Proportional and balanced current sharing among parallel four leg inverters;
- Maintained reactive power compensation capability with grid power factor near unity;
- Grid current THD below 5% ensuring compliance with power quality standards;
- Robust performance under sudden irradiance variations and load changes;
- Smooth dynamic transitions with minimal transient disturbances.

Simulation studies under realistic operating scenarios (irradiance variations from 1000 W/m² to 400 W/m² and linear inductive load changes) validated the effectiveness of the proposed control strategy integrated with reactive power compensation functionality. The parallel 4LI system with adjusted 3D-SVPWM successfully achieved stable DC bus voltage regulation, accurate output current tracking, complete circulating current elimination, proper load sharing, and excellent power quality maintenance, thereby confirming the viability of parallel configurations for medium- to high-power grid-connected PV applications.

While the cascade control loops based on PI controllers with the proposed Adjusted 3D-SVPWM Method developed in Chapter 3 demonstrated acceptable performance under nominal conditions, their effectiveness could deteriorate significantly when confronted with practical challenges including modeling inaccuracies, DC bus capacitor and output filter parameter variations beyond design assumptions, irradiance and temperature fluctuations, grid voltage disturbances and harmonics, measurement noise contaminating feedback signals, and coupling effects between control loops. These limitations motivated the development of advanced robust control techniques addressed in Chapter 4.

Recognizing that traditional PI controller-based cascade control loops for grid connected parallel 4LIs exhibit performance degradation under severe parametric uncertainties and external disturbances, Chapter 4 introduced Active Disturbance Rejection Control (ADRC) methodology to achieve superior robustness and disturbance rejection capabilities. ADRC provides a systematic framework for real-time disturbance estimation and compensation without requiring exact mathematical models, making it particularly suitable for grid-connected PV systems subject to numerous uncertainties.

Comprehensive uncertainty dynamics were formulated for both DC bus voltage and parallel 4LI output currents, explicitly accounting for DC bus capacitor and parallel 4LIs output filter inductance parameter uncertainties, grid voltage fluctuations, parallel 4LIs output currents coupling terms, DC-DC boost converter output current disturbances, and external disturbances. Through a disturbance consolidation approach, all uncertainties, parameter variations, coupling effects, and external disturbances were systematically combined into lumped total disturbances, treated as extended state variables in the control design of each control loop.

A dual-loop ADRC-based control architecture was systematically designed:

The outer DC bus voltage control loop of the parallel 4LIs system is designed using**:**

- Extended State Observer (ESO) estimated both DC bus voltage state and its total disturbance in real-time;
- State Error Feedback Controller (SEFC) using proportional control regulated estimated DC bus voltage;
- Feedforward compensation of estimated disturbance enhanced disturbance rejection;
- Generated appropriate active current references for inner loops maintaining power balance.

The inner parallel 4LIs output current control loops are both designed using:

- Three ESOs (for d, q, and 0 axes) estimated output current states and their respective total disturbances for each parallel 4LI;
- Three SEFCs regulated estimated output currents in dq0 reference frame;
- Feedforward compensation of estimated disturbances improved robustness;
- Generated voltage references for 3D-SVPWM ensuring accurate current tracking.

Detailed parameter tuning guidelines based on Hurwitz stability criteria and bandwidth selection principles were provided. The ESO bandwidths were selected as 3-5 times the corresponding SEFC bandwidths to ensure fast disturbance estimation while maintaining noise immunity. The inner loop bandwidth was set to one-fifth to one-tenth of the inverter switching frequency, while the outer loop bandwidth was designed to be one-fifth to one-tenth of the inner loop bandwidth, ensuring proper time-scale separation between control loops and avoiding undesired interactions.

The proposed ADRC method was integrated with the adjusted 3D-SVPWM circulating current suppression technique developed in Chapter 3, creating a comprehensive control framework simultaneously achieving DC bus voltage stability under power fluctuations, accurate output current tracking despite parameter uncertainties, circulating current suppression even with filter mismatches, proper load sharing among parallel inverters, and reactive power compensation maintaining unity power factor.

Comprehensive simulation studies under severe operating conditions validated the ADRC-based system's superior performance:

- Parametric Uncertainty Robustness: System maintained excellent performance despite significant variations in DC capacitance and filter inductances (up to 15-20% deviations from nominal values);
- Disturbance Rejection: Effective suppression of disturbances from irradiance variations (rapid changes from 1000 W/m² to 400 W/m²), load changes (sudden transitions between different inductive loads), grid voltage fluctuations (±10% voltage variations), and DC-DC boost converter output current ripples;
- Enhanced Dynamic Response: Faster settling times and reduced overshoot compared to conventional PI-based control during transient events;

- Improved Steady-State Performance: Minimized tracking errors for both DC bus voltage and output currents, maintaining superior power quality with grid current THD below 3%;
- Circulating Current Elimination: Maintained near-zero circulating currents even under combined parametric uncertainties and external disturbances.

Comparative analysis demonstrated that the ADRC-based parallel 4LI system outperformed conventional PI-based control approaches by approximately 40-50% in terms of disturbance rejection capability, 30-35% improvement in dynamic response speed, and 25-30% reduction in steady-state tracking errors, particularly under severe operating conditions involving simultaneous filter inductance mismatches, irradiance variations, and grid voltage disturbances.

This doctoral research has delivered a comprehensive framework for advanced grid-connected PV systems, progressively addressing challenges from fundamental modeling to sophisticated control strategies:

1. Comprehensive PV System Modeling: Established rigorous mathematical models capturing nonlinear PV cell characteristics under varying environmental conditions, validated through extensive simulations demonstrating accurate representation of real system behavior.
2. Grid-Connected 4LI System Development: Introduced four-leg inverter topology as superior alternative to conventional three-leg inverters for four-wire distribution networks, enabling independent neutral point control, unbalanced load handling, zero-sequence current management, and simultaneous harmonic mitigation and reactive power compensation.
3. Dual Operational Mode Capability: Developed control strategies supporting both harmonic compensation with reactive power support under nonlinear single-phase loads and dedicated reactive power compensation under linear three-phase loads, demonstrated through simulations achieving THD below 5% and near-unity power factor.
4. Parallel Configuration Innovation: Pioneered parallel four-leg inverter architecture addressing scalability limitations, introducing modular design increasing power capacity, enhancing reliability through redundancy, simplifying maintenance with independent module servicing, and improving thermal management through distributed operation.
5. Novel Circulating Current Suppression: Developed and validated two innovative suppression strategies with adjusted 3D-SVPWM method representing primary contribution, demonstrating near-complete circulating current elimination under significant parameter mismatches, proportional current sharing maintenance, and preserved power quality characteristics.
6. Advanced Robust Control Framework: Introduced ADRC methodology providing systematic approach for handling parametric uncertainties and external disturbances, achieving superior disturbance rejection (40-50% improvement), enhanced dynamic

response (30-35% faster), and improved steady-state accuracy (25-30% better tracking) compared to conventional PI-based control.

7. Integrated Control Strategy: Successfully combined adjusted 3D-SVPWM circulating current suppression with ADRC-based voltage and current regulation, creating comprehensive control framework simultaneously addressing multiple objectives including power quality enhancement, reactive power compensation, circulating current elimination, load sharing optimization, and robust operation under uncertainties.

The research findings of this doctoral research thesis demonstrate substantial potential for real-world deployment of grid-connected PV systems across diverse contexts. The proposed parallel 4LI configuration and advanced control strategies enable large-scale solar farms to inject high-quality power into the grid while maintaining stability and compliance with power quality standards. In industrial parks and commercial campuses, the system effectively serves mixed single-phase and three-phase nonlinear loads, offering reactive power support and harmonic compensation to minimize reliance on additional conditioning equipment. For rural microgrids, the modular parallel architecture ensures scalable and redundant operation aligned with local energy growth, supporting reliability in areas with limited infrastructure. Mission-critical facilities such as hospitals, data centers, and telecommunications hubs gain from enhanced redundancy, superior power quality, and uninterrupted operation during faults or maintenance. Moreover, these systems can contribute to grid support services through reactive power compensation, harmonic filtering, and potential future functions such as frequency regulation and virtual inertia, thereby reinforcing the flexibility and resilience of modern power networks.

While this thesis has made substantial contributions, several limitations suggest promising directions for future research:

1. Experimental Validation: All results presented are based on simulation studies. Comprehensive experimental validation through laboratory prototypes and field testing is essential to confirm theoretical findings, assess real-world performance under practical constraints, validate robustness against measurement noise and hardware non-idealities, and demonstrate commercial viability through long-term reliability testing.
2. Extended Operating Modes: Future work should investigate islanded operation mode enabling autonomous microgrid operation, grid-forming capabilities providing voltage and frequency references during grid outages, seamless transition between grid-connected and islanded modes, and black-start capability for grid restoration after blackouts.
3. Hybrid Energy Systems Integration: Extending the framework to incorporate energy storage systems (batteries, supercapacitors) enabling power smoothing, peak shaving, and energy arbitrage; other renewable sources (wind, small hydro) creating diversified energy portfolios; hydrogen production and fuel cells for long-term energy storage; and coordinated control strategies optimizing multi-source operation.
4. Advanced Observers and Optimization Techniques: Exploring advanced observer-based ADRC methods, such as super-twisting observers and nonlinear high-gain

observers, to enhance disturbance estimation and rejection capabilities, improve dynamic response, and achieve better steady-state performance while minimizing noise sensitivity. Additionally, integrating artificial intelligence and machine learning techniques to implement adaptive MPPT algorithms and optimize ADRC performance, enabling intelligent, self-tuning control for varying environmental and operating conditions.

5. Fault-Tolerant Control Strategies: Developing fault detection and diagnosis algorithms for early identification of component degradation or failures, reconfiguration strategies maintaining operation despite inverter or module failures, graceful degradation approaches preserving partial functionality during severe faults, and predictive maintenance scheduling based on condition monitoring and remaining useful life estimation.

This doctoral thesis has systematically addressed the multifaceted challenges associated with integrating decentralized photovoltaic generation into modern power grids. Beginning with fundamental modeling and control of standalone PV systems, progressing through grid-connected single four-leg inverter development with dual operational capabilities, advancing to parallel configurations with innovative circulating current suppression techniques, and culminating in robust ADRC-based control framework handling parametric uncertainties and external disturbances, the research has delivered a comprehensive and cohesive body of work.

The proposed solutions harmonize theoretical rigor with practical applicability, offering scalable, reliable, and high-performance alternatives to conventional grid-connected PV systems. By enabling effective handling of unbalanced and nonlinear loads, superior power quality maintenance, enhanced system reliability through modularity and redundancy, and robust operation under severe uncertainties and disturbances, the contributions significantly advance the state-of-the-art in renewable energy integration.

As global energy systems transition toward sustainability, the need for innovative solutions enabling seamless integration of distributed renewable generation becomes increasingly critical. This thesis provides foundational knowledge, practical methodologies, and validated control strategies that can accelerate the deployment of high-performance grid-connected PV systems, contributing to energy security, environmental sustainability, and economic prosperity. The research outcomes not only address contemporary challenges but also establish a platform for future innovations in smart grids, microgrids, and sustainable energy systems, paving the way toward a cleaner, more resilient, and more sustainable energy future.

Appendix: Parameters of the system and controllers

Table A.1: Parameters of PVG DC-DC boost converter system.

Open loop voltage	V_{oc}	43.5 V
Close loop current	I_{sc}	4.75 A
Maxium power point traking voltage	V_{MMP}	34.5 A
Maxium power point traking current	I_{MMP}	4.35 A
Nominal power output	P_{PV}	36 kW
Parallel strings	N_p	10
Number of modules in series within string	N_s	20
DC-DC boost converter input inductance	L_{Gpv}	10 mH
PV output capacitor	C_{Gpv}	1000 µF

Table A.2: Parameters of PVG DC-DC boost converter controllers.

Natural frequency of the PVG output voltage system PI controller	ω_{nVpv}	80 rad/s
Damping factor of the PVG output voltage PI controller	ξ_{Vpv}	0.707
Natural frequency of the DC-DC boost converter's input current PI controller	ω_{nipv}	1000 rad/s
Damping factor of the DC-DC boost converter's input current PI controller	ξ_{ipv}	0.707
Commutation Frequency of the DC-DC boost converter	f_{sboost}	20 kHz

Table A.3: Parameters of four leg inverter grid connected system.

Grid voltage	V_{grms}	220 V
Four leg inverter input voltage	V_{dc}	800 V
Four leg inverter input capacitor	C_{dc}	5000 µF
Grid inductance	L_g	2.6 mH
Grid resistance	R_g	1 mΩ
Four leg inverter output filter inductances	L_{f1}, L_{f2}	10 mH, 5 mH
Single phase nonlinear load		
Three phase linear loads	R_{L1}, L_{L1}; R_{L2}, L_{L2}	8 Ω, 8 mH; 8 Ω, 8 mH

Table A.4: Parameters of four leg inverter grid connected controllers.

Natural frequency of the inner inverter output current PI controllers	ω_{ni}	8000 rad/s
Damping factor of the inner inverter output current PI controllers	ξ_i	0.707
Natural frequency of the outer DC bus voltage PI controller	ω_{ndc}	100 rad/sec
Damping factor of the outer DC bus voltage PI controller	ξ_{idc}	0.707
Commutation Frequency in single four leg inverter	f_s	16 kHz
Commutation Frequency in parallel four leg inverters	f_s	8 kHz
Natural frequency of the PLL PI controller	ω_{nPLL}	2000 rad/s
Damping factor of the PLL PI controller	ξ_{PLL}	0.707
Parameters of the robust synchronization PLL unit	l_1, l_2	3200, 180
Natural frequency of the ZSCC PI controller	ω_{nz}	8000 rad/s
Damping factor of the ZSCC PI controller	ξ_z	0.707

Table A.5: Parameters of the ADRC controllers.

Bandwidth of the ESO for inner inverter output current control loop	ω_{0eso}^{i}	1200 rad/s
Bandwidth of the SEFC for inner inverter output current control loop	ω_{csef}^{i}	120 rad/s

Bandwidth of the ESO for outer DC bus voltage control loop	ω_{0eso}^{v}	200 rad/s
Bandwidth of the SEFC for outer DC bus voltage control loop	ω_{csef}^{v}	20 rad/s

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Abstract :

In recent years, the integration of decentralized generation based on photovoltaic energy sources and static power converters has significantly increased, particularly in three-wire power networks. This trend supports the use of local energy resources near consumption points.

The photovoltaic-grid system is considered a promising solution to increase the share of renewable energy and enhance power quality within electrical networks. However, such systems are highly sensitive to variations in load or source parameters and power levels, which can impact their stability, synchronization, and energy quality. These technical challenges raise concerns about the reliability of decentralized generation systems.

This research primarily aims to explore various topologies and control strategies for decentralized photovoltaic-grid systems. These systems utilize interleaved DC-DC converters and four-leg inverters to inject power and improve power quality in four-wire electrical networks.

To enable the integration of high-power decentralized generation into four-wire networks, the study also investigates the use of multilevel converters and parallel configurations of static power converters.

A key focus is on selective control strategies for decentralized photovoltaic–grid systems and on addressing the issue of circulating currents in parallel converter structures. Solutions will be proposed to optimize the number of active converters based on the power requirements of the four-wire network.

To further enhance the performance of decentralized photovoltaic–grid systems, advanced control techniques will be introduced. These include adaptive nonlinear control, 3D Space Vector Pulse Width Modulation (3DSVPWM), and intelligent control strategies. These methods have demonstrated effectiveness in maintaining stability, ensuring synchronization, improving power quality, and dealing with parameter and power variations from loads or energy sources.

Keywords:

Photovoltaic system, Two-level four-leg inverter, Circulating current, Power quality, Advanced and intelligent control strategies.

الملخص:

شهدت السنوات الأخيرة تزايدًا ملحوظًا في دمج أنظمة التوليد اللامركزي المعتمدة على مصادر الطاقة الشمسية الكهروضوئية ومحولات القدرة الساكنة، خاصة في الشبكات الكهربائية ثلاثية الأسلاك، مما يتيح الاستفادة من الموارد المحلية القريبة من أماكن الاستهلاك.

تُعد أنظمة الربط بين الطاقة الشمسية والشبكة الكهربائية من البدائل الواعدة لزيادة نسبة الطاقة المتجددة وتحسين جودة الطاقة في الشبكات الكهربائية. ومع ذلك، فإن استقرار هذه الأنظمة وتزامنها وجودة الطاقة التي توفرها تتأثر بشكل كبير بتقلبات الأحمال أو مصادر الطاقة، مما يثير تحديات تقنية تتعلق بموثوقية أنظمة التوليد اللامركزي.

يركز هذا البحث على دراسة مختلف البنى الطوبولوجية واستراتيجيات التحكم لأنظمة التوليد اللامركزي الكهروضوئية المتصلة بالشبكة، والتي تعتمد على محولات DC-DC المتداخلة وعواكس رباعية الأذرع، بهدف تحسين جودة الطاقة وضخ القدرة في الشبكات الكهربائية رباعية الأسلاك.

ولدمج التوليد اللامركزي في الشبكات رباعية الأسلاك ذات القدرة العالية، يتناول البحث أيضًا استخدام المحولات متعددة المستويات، بالإضافة إلى البنى التي تعتمد على توصيل محولات القدرة الساكنة على التوازي.

سيتم تقديم استراتيجيات تحكم انتقائية لهذا النوع من الأنظمة، إلى جانب حلول لمشكلة التيارات الدوارة في البنى المتوازية للمحولات، بهدف تحسين عدد المحولات العاملة بناءً على متطلبات القدرة في الشبكة رباعية الأسلاك.

ولتطوير أداء هذه الأنظمة، سيتم تقديم تقنيات تحكم متقدمة مثل التحكم غير الخطي التكيفي، وتقنية تعديل عرض النبضة ثلاثية الأبعاد(3DSVPWM) ، بالإضافة إلى تقنيات تحكم ذكية. وقد أثبتت هذه الطرق فعاليتها من حيث الاستقرار، والتزامن، وجودة الطاقة، وقدرتها على التعامل مع تقلبات الأحمال أو مصادر الطاقة.

الكلمات المفتاحية

النظام الكهروضوئي، العاكس رباعي الأذرع ثنائي المستوى، التيار الدوّار، جودة الطاقة، استراتيجيات التحكم المتقدمة والذكية.

Résumé :

Ces dernières années, l'intégration croissante de la production décentralisée basée sur des sources d'énergies photovoltaïqueet des convertisseurs statiques est en forte progressionpour les réseaux électriquesà trois filsqui permettent l'exploitation des ressources locales proches des lieux de consommation.

Le système photovoltaïque-réseau électrique est une des alternatives envisagées pour augmenter le taux d'énergie renouvelable et d'améliorer la qualité de l'énergiedans les réseaux électriques. La stabilité, la synchronisation et la qualité de l'énergie d'un système photovoltaïque-réseau électriqueest fortement sensible aux variations des paramètres et de puissance venant des charges ou des sources d'énergie.Toutefois, des contraintes techniques principalement liées à ces performances soulèvent des problèmes difficiles sur la fiabilité du système de production décentralisée.

Dans ce travail de recherche, l'objectif principal est d'aborder les différentes topologies et stratégies de commande des systèmes de productions décentraliséesphotovoltaïques-réseaux électriquesbasée sur des convertisseurs statiques de puissance DC-DC entrelaceset des onduleurs à quarte bras en vue d'injecter la puissance et d'améliorer la qualité de l'énergie dans les réseaux électriques à quatre fils.

Afin d'intégrée la production décentralisée dans les réseaux électriques à quatre fils de forte puissance, les systèmes de productions décentralisées photovoltaïques-réseaux électriques basée sur les convertisseurs multiniveaux et les structures mises en parallèle des convertisseurs statiques de puissance seront également abordées dans ce travail de recherche.

Une sélectivité dans la commande de ce type de système de production décentralisée photovoltaïque-réseaux électriqueet une solution pour le problème du courant de circulation dans les structures mises en parallèle des convertisseurs statiquesseront introduites, pour optimiser le nombre de convertisseurs statiques en service en fonction de la puissance de réseau électrique à quatre fils.

Pour améliorer les performances de ces systèmes de productions décentralisées photovoltaïques-réseaux électriques des techniques de commandeavancéesseront introduites. Il s'agira de la commande non-linéaire adaptative, de la commande par 3DSVPW et d'autres commandes intelligentes. Ces commandes ont fait preuve d'efficacité du point de vue destabilité, synchronisation, qualité d'énergie et de la prise en compte du problème de la variation desparamètres et de puissance venant des charges ou des sources d'énergie.

Mots clés :
Système photovoltaïque,Onduleur à quarte bras à deux niveaux,Courant de circulation, Qualité d'énergie, Commandesavancées et intelligentes.