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# Procesor in-the-Loop (PIL) Validation of Single-Phase Inverter Deadbeat Control with Disturbance Rejection

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*Abstract*—**In islanded mode and UPS applications, nonlinear loads cause significant distortion of the inverter output voltage due to the charging current of the capacitor at the parallel RC nonlinear load side. To mitigate this phenomenon, this paper presents a disturbance rejection-based deadbeat control strategy for single-phase voltage-controlled inverters, aiming to improve power quality under nonlinear loads. The controller-based deadbeat ensures fast and reliable reference tracking, while the DOB provides a lumped disturbance to actively compensate it by a subtractive mechanism. Co-simulation with processor-in-the-loop demonstrates the feasibility of this combined strategy in mitigating harmonic distortion. The method also achieves high-quality sinusoidal output under nonlinear load.**

***Keywords—Disturbance Observer (DOB), Power Quality, Harmonic Compensation, Nonlinear Loads, Islanded Mode.***

## I. INTRODUCTION

Voltage-controlled inverter plays an important role in islanded microgrid and uninterruptible power supplies (UPS) applications. It should produce a clean and pure sine waveform output voltages with guarantying high quality regardless of the load type [1-2]. However, under nonlinear loads, the output voltage of the inverter might be distorted with harmonic distortion leading to power quality degradation; Employing conventional state feedback or linear PI-based control to suppress this problem will definitely fail. This reason has motivated to the development of new control strategies based on advanced techniques such as deadbeat and model predictive based control (MPC).

Deadbeat based control has been widely used in power electronic converters because its main advantage is a fast transient response which enables the system reaching the desired output reference within one sampling period [2-6]. For instance, it is reported in [4], [6] improved dynamic performance deadbeat control has been successfully applied to distributed generation inverters DG and UPS. However, deadbeat control is too sensitive to parameter mismatch and dependent to the system model, which might not guarantee high performance and high quality of the output voltage in the presence of nonlinear loads [5-6].

To overcome this issue, a DOB-based compensation strategy is incorporated with deadbeat control as a systematic solution [7-17]. This DOB is incorporated to estimate and reject lumped disturbances comprising nonlinear load current and unmolded. The estimated disturbance signal can then be fed into the control loop to actively compensate for it; While deadbeat based control ensures fast reference tracking of the output voltage. This way guarantees the robustness and high power quality of the system.

Motivated by this concept, the paper proposes a deadbeat-based control strategy integrated with disturbance observer DOB for a single-phase voltage-controlled inverter feeding nonlinear load. The

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proposed control scheme preserves the fast dynamic response of deadbeat control while linking it with DOB which shows the ability of the method in disturbance rejection and harmonic suppression. The DOB estimates the disturbance induced by the load then compensated in real time which contributes in ensuring pure sinewave voltage with high quality. Co-simulation PIL with STM32F407 shows the feasibility of the approach in suppressing the disturbance and enhancing the THD of the output voltage.

## II. CONTROL METHOD

### *1- System Modeling*

The studied system as shown in Figure.1 is a single-phase H-bridge inverter, it is feeding a load through an LC output filter.

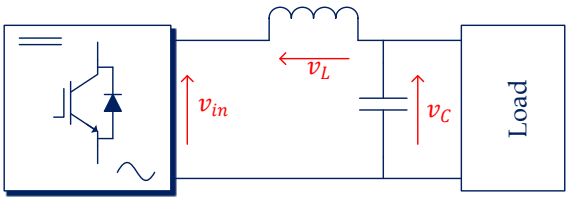


Fig. 1. Single-phase voltage controlled inverter with LC filter

The continuous time model of LC filter feeding the load can be expressed as

$$\begin{cases} \dot{x}(t) = Ax(t) + Bu(t) + Ei_{out}(t) \\ y(t) = Cx(t) \end{cases} \quad (1)$$

Where $x(t) = [v_C(t)\ i_L(t)\ ]^T$ is the state vector, $v_{in}(t) = v_{dc}u(t)$is the output voltage of the inverter and this should be normalized, $i_{out}(t)$ is the load current and this should be the unknown load current d(t);

And:

$$\begin{cases} A = \begin{bmatrix} 0 & \frac{1}{C_f} \\ -\frac{1}{L} & 0 \end{bmatrix} \\ B = \begin{bmatrix} 0 \\ \frac{v_{dc}}{L} \end{bmatrix} \\ E = \begin{bmatrix} -\frac{1}{C_f} \\ 0 \end{bmatrix} \\ C = [1 \quad 0] \end{cases}$$

### *2- Deadbeat control law*

To formulate the deadbeat control law, the system should be firstly discretized as follows:

$$\begin{cases} x(k+1) = A_d x(k) + B_d u(k) + E_d d(k) \\ y(k) = Cx(k) \end{cases} \quad (2)$$

where the system parameters become

$$\begin{cases} A_d = \begin{bmatrix} 1 & \frac{T_s}{C_f} \\ -\frac{T_s}{L} & 1 \end{bmatrix} \\ B_d = \begin{bmatrix} 0 \\ T_s.\frac{v_{dc}}{L} \end{bmatrix} \\ E_d = \begin{bmatrix} -\frac{T_s}{C_f} \\ 0 \end{bmatrix} \\ C = [1 \quad 0] \end{cases}$$

To build the deadbeat objective, we discretize it two steps of prediction for a natural horizon, the system becomes:

$$x(k+2) = A_d A_d x(k) + (A_d B_d + B_d)u(k) \quad (3)$$

Hence, the output voltage can be written as:

$$\begin{aligned} v_C(k+2) &= Cx(k+2) \\ &= C[A_d A_d x(k) + (A_d B_d + B_d)u(k)] \end{aligned} \quad (4)$$

We put $v_C(k+2) = v_{C,ref}(k+2)$ then we obtain the deadbeat law $u(k)$:

$$u(k) = \frac{v_{C,ref}(k+2) - C[A_d A_d x(k)]}{C[(A_d B_d + B_d)]} \quad (5)$$

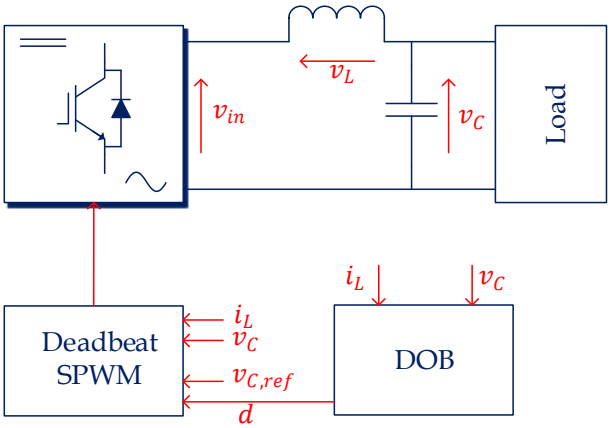


Fig. 2. Proposed control scheme for voltage controlled inverter with LC filter

### *3- Disturbance Observer*

The disturbance observer DOB is employed to estimate the load current, the estimation mechanism is based on using capacitor current equation and we obtain the raw estimate as follows:

$$d(k) = i_L(k) - C_f \frac{v_c(k) - v_c(k-1)}{T_s} \quad (6)$$

As it is indicated in equation (6), the estimation law is too sensitive to measurement noise; however, we can use simple first order low pass filter to remove the large noise and smooth it while preserving the real disturbance dynamic. After filtering it with first order $Q(s) = \frac{\omega_c}{s+\omega_c}$ we obtain the disturbance estimate $\hat{d}(k)$as:

$$\hat{d}(k) = (1-\alpha)\hat{d}(k-1) + \alpha d(k) \qquad (7)$$

with

$$\alpha = \frac{\omega_c T_s}{1+\omega_c T_s}, \omega_c = 2\pi f_c$$

The Q-filter cut-off frequency $f_c$ should be chosen below switching frequency.

It is noticed, from state model, that the disturbance gets in as an additive uncertainty in the state-space model where it is canceled in the deadbeat control law and compensate the term $E_d d(k)$ in the control law. Hence, the state model becomes:

$$x(k+2) = A_d A_d x(k) + (A_d B_d + B_d)u(k) + (A_d E_d + E_d)d(k) \qquad (8)$$

This allows us to write the output voltage as:

$$v_C(k+2) = Cx(k+2) = C[A_d A_d x(k) + (A_d B_d + B_d)u(k) + (A_d E_d + E_d)d(k)]$$

Finally, the control law $u(k)$ now is incorporating the lumped disturbance and can compensate for it

$$u(k) = \frac{v_{C,ref}(k+2) - C[A_d A_d x(k) + (A_d E_d + E_d)d(k)]}{C[(A_d B_d + B_d)]} \qquad (9)$$

## III. Simulation Results

The proposed deadbeat control with disturbance observer (DOB) has been assessed on a single-phase full bridge voltage-controlled inverter with an LC filter, the algorithm is implemented on STM32f407 and the system of power electronics is modeled in MATLAB/Simulink. The inverter parameters are: $v_{dc} = 400V$ , the system will be firstly tested under no load and then under nonlinear load with a diode H-bridge rectifier and a parallel RC load like it is shown in Figure.3.

Table. 1. Design parameters of the system.

| Parameters | Symbol (Unit) | Values |
|---|---|---|
| Filter inductance | $L(mH)$ | 1 |
| Filter capacitance | $C_f(\mu F)$ | 15 |
| Sampling time | $T_s(\mu s)$ | 10 |
| Switching frequency | $f_{sw}(Hz)$ | $10kHz$ |
| R rectifier load | $R(\Omega)$ | 20 |
| C rectifier load | $C(\mu F)$ | 400 |

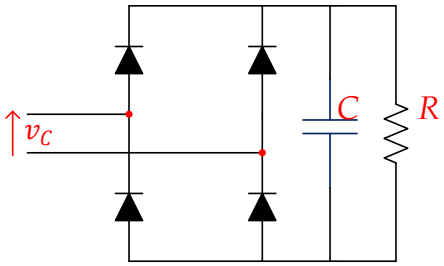


Fig. 3. Nonlinear-load.

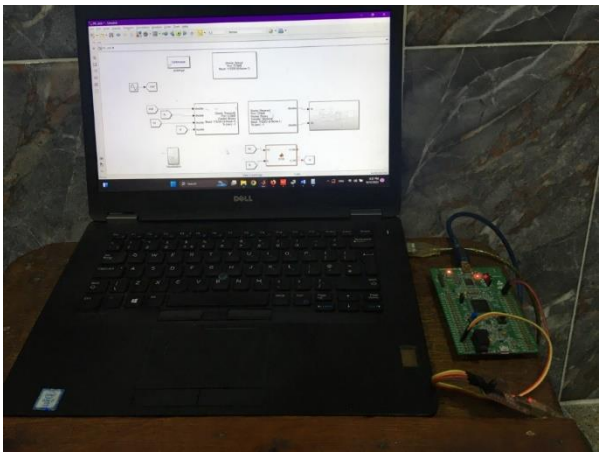

Fig. 4. PIL with STM32f407 of single-phase voltage controlled inverter.

*1- under no-load test*

Firstly, Figure.5 shows the output voltage of the inverter under no load. It is noticed that the voltage is properly regulated with low harmonics which its value is approximately THD=0.22%.

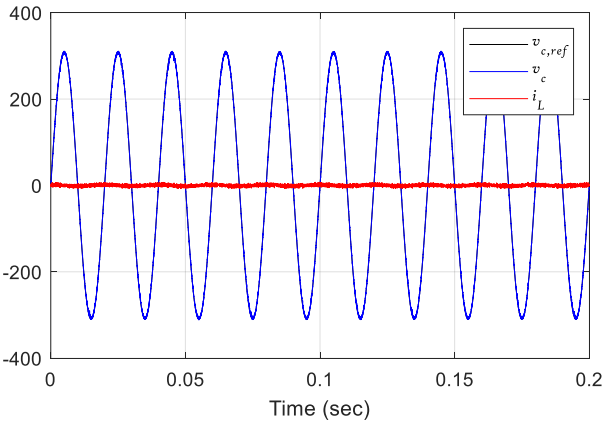


Fig. 5. Controlled-voltage in no-load test.

*2- under nonlinear-load without DOB test*

Now the proposed method should be tested in the presence of nonlinear load without DOB compensation.

As shown in Figure.6, despite the fast voltage reference tracking of the deadbeat based control, the output voltage is distorted and lost its sinusoidal form. Also as it is depicted in Figure.7, the value of total harmonic distortion (THD) is 5.9 % which is out of international standards.

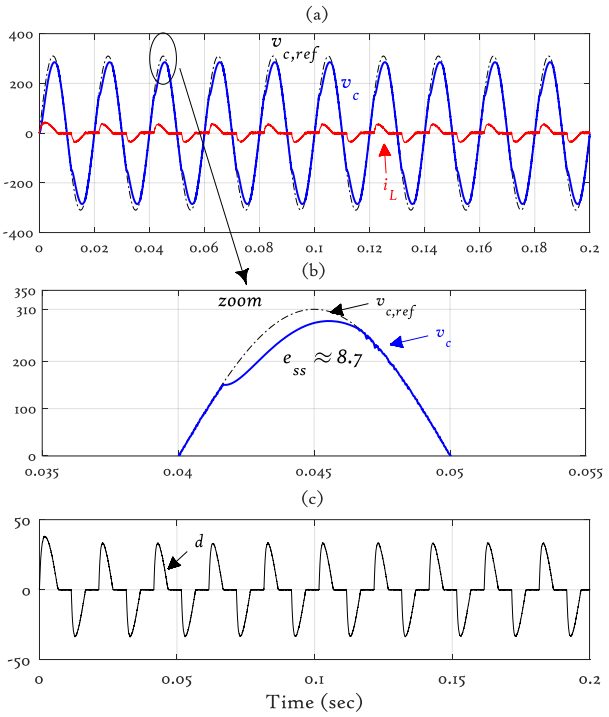


Fig. 6. (a) Controlled-voltage and load current under nonlinear-load test when employing only deadbeat control; (b) voltage zoom; (c) estimated disturbance.

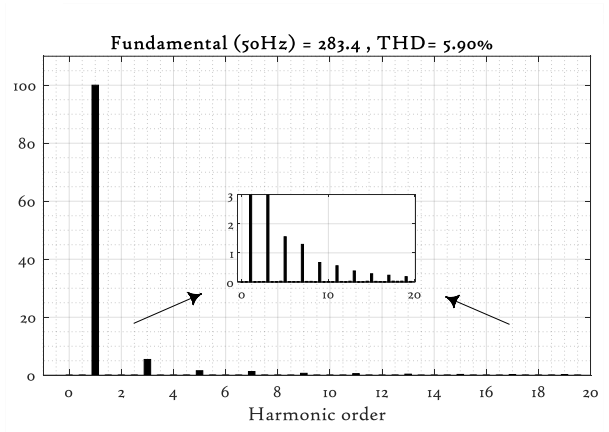


Fig. 7. Harmonic spectrum of the output voltage when only Deadbeat applied.

*3- under nonlinear-load with DOB test*

To make the system control more robust against disturbances, the proposed control scheme is incorporated with DOB (Figure.8) enabling the active compensation for disturbances into the deadbeat predictive law. The inverter output voltage is perfectly tracking the sinusoidal reference showing reduced distortion. Graphical THD analysis affirms that the DOB helps in reducing the distortion to 1.29% and this complies with IEEE-519 power quality standards, see Figure.9.

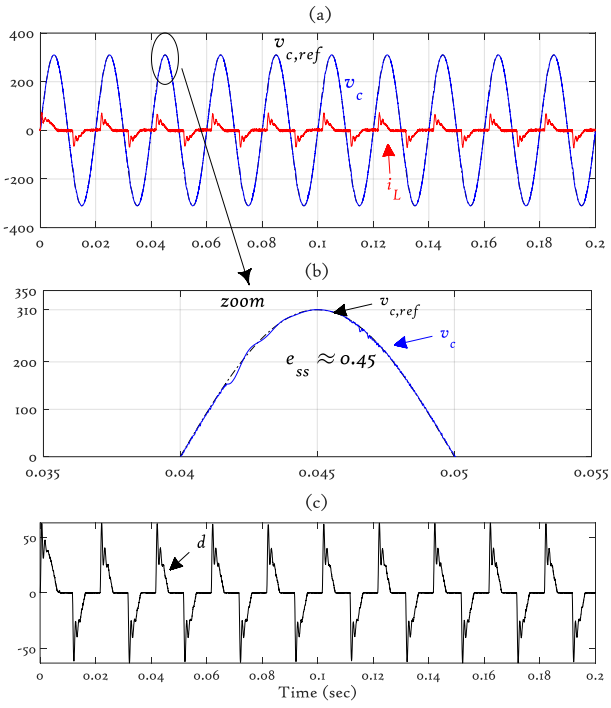


Fig. 8. (a) Controlled-voltage and load current in nonlinear-load test when the proposed deadbeat-based DOB is applied; (b) voltage zoom; (c) estimated disturbance. .

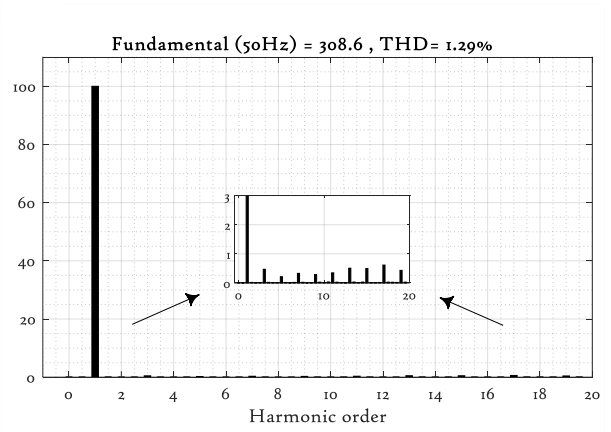


Fig. 9. Harmonic spectrum of the voltage when Deadbeat-DOB is applied.

Moreover, the performance of the proposed scheme is also assessed in terms of static error compensation; where the deadbeat-based DOB controller achieves to actively cancel the static error caused by the nonlinear

load. The steady state error of the voltage is reduced from 8.7% (without DOB) to 0.45% (with DOB)

Therefore, we can say that the proposed deadbeat-based DOB control is an alternative solution for single-phase voltage-controlled inverters whether in microgrid or UPS applications.

## IV. CONCLUSION

In this paper, it is presented a deadbeat control improved with a disturbance observer for single-phase voltage controlled inverter. Deadbeat control presents an advantage in ensuring fast reference and accurate voltage tracking. However, the control law is constructed with help of system model which makes it sensitive to model uncertainties and load disturbances. Because that the proposed method is based on deadbeat with incorporating disturbance observer DOB, the deadbeat keeps rapid reference tracking while DOB guarantees the robust compensation for disturbances which ensures pure sinewave voltage and high power quality.

The feasibility of the control method is validated through processor-in-the loop PIL with Simulink and STM32f407. The results showed that the proposed scheme maintain, in real time, a pure sinusoidal output voltage with reduced harmonics THD.

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